

Name: _____ EE224 Last 4 SSN _____

Answer sheet. Place all answers on this page. ***If the answers are not on this sheet, you will receive a score of zero.*** You may attach work to this sheet if you desire. Precedence matters $A+BC+D$ is $A+(BC)+D$, not $(A+B)(C+D)$.

1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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A

A

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A

A

Name: _____ EE224 Last 4 SSN _____

- 1 Design a Rising edge TSPC Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A*B+C*D$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 150ps for Pre-charge 80ps for N tree evaluate time. The inverter low to high time is 40ps. The inverter high to low time is 100ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 38ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 2.359u and W_{pi} is 6.328u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a clock tree to drive 32 loads assuming each driver can drive at most 4 loads. (10 points)
- 4 Design a P Tree Domino logic $A*B+C$ gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 Why is the weak keeper used in Domino logic. (10 points)
- 6 Design a static CMOS function implementing $Z=(A+B+C)(D+EF)$ matching the standard inverter with $W_n=2.5/0.18$ and $W_p=4/0.18$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 Design a 4 input DCVSL(dynamic) mux. Assume both input phases are available. Show transistor schematics. (10 points)
- 8 Show the clocking relationships for a 3 phase N Tree dynamic logic architecture. (10 points)

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1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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B

B

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B

B

Name: _____ EE224 Last 4 SSN _____

- 1 Design a falling edge Mux based Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A+B \cdot C \cdot D$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 70ps for Pre-charge 30ps for N tree evaluate time. The inverter low to high time is 30ps. The inverter high to low time is 60ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 39ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 3.908u and W_{pi} is 8.386u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a 3 input CPL Mux. Show schematics. (No transistor sizes required) (10 points)
- 4 Design a Static CMOS $A \cdot B + C \cdot D$ gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 What is the miller effect? How does it relate to capacitance in high speed logic design?.. (10 points)
- 6 Design a static CMOS function implementing $Z=(A \cdot B + C \cdot D)(E + F)$ matching the standard inverter with $W_n=3/0.18$ and $W_p=8/0.18$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 Design a 6 input dynamic logic AND function in a single block with no transistor tree over 3 high. Show transistor schematics and clock waveform(s). (10 points)
- 8 What is the relationship between the clocks in a two phase NORA/Zipper domino logic architecture. (10 points)

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1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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C

C

Name: _____ EE224 Last 4 SSN _____

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C

C

Name: _____ EE224 Last 4 SSN _____

- 1 Design a Rising edge TSPC Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A+B \cdot C+D$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 85ps for Pre-charge 50ps for N tree evaluate time. The inverter low to high time is 45ps. The inverter high to low time is 45ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 100ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 12.723u and W_{pi} is 13.652u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a 2 input CVSL XNOR gate. Assume both phase are available. Show transistor schematics. (10 points)
- 4 Design a N Tree Domino Logic C (B+A) gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 Draw the side view of a N and P transistor labeling all parts. (10 points)
- 6 Design a static CMOS function implementing $Z=(AB+C)(DE+F)$ matching the standard inverter with $W_n=3/0.18$ and $W_p=5/0.18$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 How can very wide AND functions be performed in NORA logic? Show a block diagram for a 12 input example with no gate having more than 4 inputs. (10 points)
- 8 Show the clocks for a 5 phase P tree dynamic logic architecture. (10 points)

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1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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D

D

Name: _____ EE224 Last 4 SSN _____

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Name: _____ EE224 Last 4 SSN _____

- 1 Design a Falling edge Mux based Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A*B*C*D$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 55ps for Pre-charge 30ps for N tree evaluate time. The inverter low to high time is 25ps. The inverter high to low time is 35ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 110ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 12.414u and W_{pi} is 18.65u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a clock distribution network driving 25 loads assuming each driver can drive at most 5 loads. (10 points)
- 4 Design a Static CMOS $(A*B) + C$ gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 Why is dynamic logic faster than static CMOS? Give at least 3 reasons. (10 points)
- 6 Design a static CMOS function implementing $Z=(A+B+C)(D+EF)$ matching the standard inverter with $W_n=1/0.24$ and $W_p=3/0.24$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 Design a 3 input DCVSL and function. Assume both phases are available. Show transistor schematics. (10 points)
- 8 What is the clock relationship between sections of NORA or zipper logic. Show in a block diagram. (10 points)

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1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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6

E

E

Name: _____ EE224 Last 4 SSN _____

7

8

E

E

Name: _____ EE224 Last 4 SSN _____

- 1 Design a Falling edge Pass gate Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A*B*C+D$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 85ps for Pre-charge 50ps for N tree evaluate time. The inverter low to high time is 45ps. The inverter high to low time is 85ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 80ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 3.128u and W_{pi} is 6.34u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a CPL function implementing $A \text{ xor } B \text{ xor } C$. Draw transistor schematics. (10 points)
- 4 Design a N Tree Domino Logic $(A+B) * (C+D)$ gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 How can charge sharing be mitigated? (10 points)
- 6 Design a static CMOS function implementing $Z=(AB+C)(D+EF)$ matching the standard inverter with $W_n=2/0.18$ and $W_p=3/0.18$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 How can very wide OR functions be performed in NORA logic? Show a block diagram for a 10 input example with no gate having more than 5 inputs. (10 points)
- 8 Show the clocks for a two phase N Tree dynamic logic architecture (10 points)

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1

2 Dynamic Cl _____ ff + _____ ff* Wnt + _____ ff * Wpi
Capacitance seen by previous stage from A input _____ ff
Labeled Schematic:

3

Name: _____ EE224 Last 4 SSN _____

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F

F

Name: _____ EE224 Last 4 SSN _____

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F

Name: _____ EE224 Last 4 SSN _____

- 1 Design a Rising edge Mux based Flip Flop. Show schematics using basic gates or transistors. No transistor sizes (10 points)
- 2 Design a N tree Dynamic latch. Perform the $A+B+CD$ logic function in the Dynamic Logic Element. Assume that both phases of the input are available if needed. Size all transistors. Allocate 66ps for Pre-charge 44ps for N tree evaluate time. The inverter low to high time is 33ps. The inverter high to low time is 55ps. Hint: divide all delays associated with pre-charge by 2. Assume the inverter is driving 105ff of external capacitance. Assume the metal within the dynamic logic block has 3ff of additional capacitance. $V_{dd}=1.2V$. A_i is 5. Assume all transistors in the N switch tree are the same W/L. Make the top of the tree as small as possible without sharing source drains. Consider overlap capacitances. (Calculate all transistor sizes to 3 significant digits. Do not round any transistor sizes to the grid for this problem. Draw and label schematics with transistor sizes. Calculate the capacitance seen by the previous stage. The size of the inverter has already been calculated. Assume W_{ni} is 6.352u and W_{pi} is 11.36u. (You don't have to calculate the inverter sizes) (25 points)
- 3 Design a DCVSL(dynamic) function implementing $A+B+CD$. Draw transistor schematics. (10 points)
- 4 Design a Static CMOS $A+B+CD$ gate showing transistor schematics, and perform a Sticks drawing representing a possible layout. Assume both phases of the input are available if required. (No device sizes) (15 points)
- 5 What type of weak keeper is used in P tree domino logic. Show a schematic representing it's use. (10 points)
- 6 Design a static CMOS function implementing $Z=(ABC)(D+E+F)$ matching the standard inverter with $W_n=3/0.18$ and $W_p=4/0.18$. Draw and label schematics with device sizes. Use a minimum number of transistors (10 points)
- 7 Draw schematics for a NORA/Zipper function implementing $(ABC+DEF)*(GHI+JKL)$ in two levels. Assume no transistor tree is higher than 4 levels. (10 points)
- 8 What are the clock relationships if N Tree dynamic logic is to be used as logic with static FFs? Illustrate with a block diagram. (10 points)