Photolithography

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Photolithography I

- Without photolithography there would be no integrated circuits because every process done to a wafer to fabricate diodes and transistors (implantation, oxidation, diffusion, and etching), would be done to the whole surface of the wafer. We would be limited to diodes and MOS capacitors the size of the wafer (Yes we could cut the wafer up into parts, but this is quite limited.)

Photolithography

- Our Process:
  - Singe
  - Spin on photoresist
  - Pre-Bake
  - Expose
  - Develop
  - Post-Bake
  - Etch
  - Remove photoresist

Singe

- What is it?
  - Heat wafers to about 800 ^{o}C for five minutes in.
- Why do we do it?
  - SiO_2 and Si attract water and absorb it.
  - Photoresist repels water, thus if the SiO_2 or Si have absorbed water, the photoresist will not stick.
  - We can also ash particles on the wafers.

Spin on photoresist

- What is it?
  - Photoresist is a photosensitive film that can be selectively patterned, and can protect the underlying structures from your etch process. It is a polymer that contains a interlocking mechanism, photosensitive chemicals, and solvents.
- Why do we spin it on?
  - Spinning it on is the quickest way to uniformly coat the wafer with photoresist.
  - It also drys out the solvent from the PR.

Spin on photoresist

- Problems?
  - Most of the PR is spun off the wafer. PR is about $900 per gallon.

Pre-Bake

- What is it?
  - Bake the wafers for 90 ^{o}C for 30 minutes.
- Why do we do it?
  - Drive out solvent
    - Convert liquid to solid
  - Relieve stress during spin on step
- It needs to be carefully optimized with exposure time. Too much softbake and the film will not be very sensitive to the developer. Too little and the film will be too sensitive.

Expose

- What is it?
  - Selectively expose the PR coated wafers with UV light with a predetermined amount of energy.
- Why do we use UV light?
  - We can resolve features down to about $\lambda/2$.

Develop

- What is it?
  - Mechanically agitate the exposed wafers in a developer solution.
- Why do we do it?
  - This removes the PR that we do not want. We have a selective pattern on the sample that will protect features from etching.

Post-Bake

- What is it?
  - We post-bake at 120^{o}C for 20 minutes
- Why do we do it?
  - This drives out all the elements that would allow the PR to be attacked by the etch.

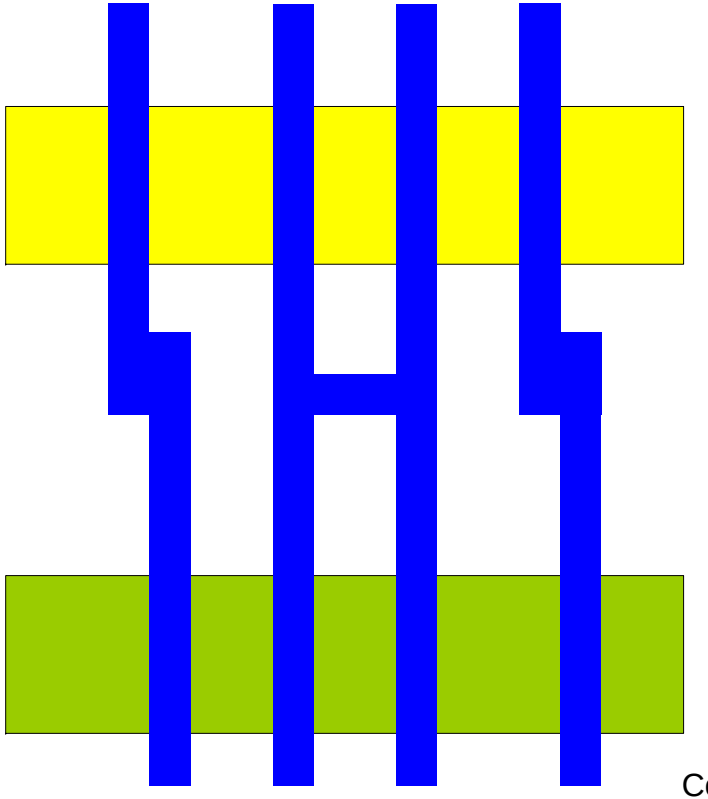
Etch or Process

- Once we have completed these step we have to remove oxide so that we can diffuse n or p, implant or grow a different quality oxide on the wafer.
- Note: We are not able to diffuse or oxidize until we have removed the patterning PR.

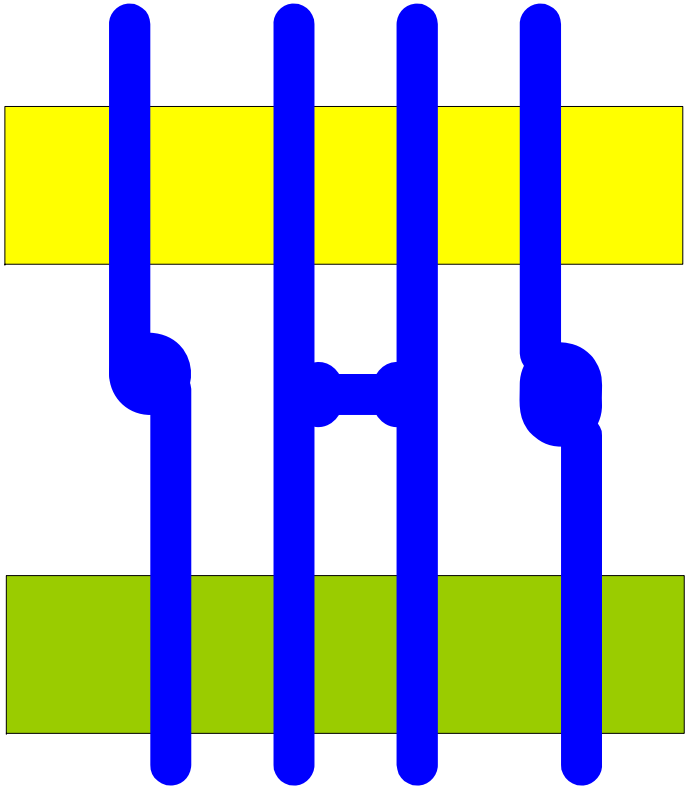
Survey of 90nm transistor issues

- **Poly Flare**
  - Changes Resistance and Capacitance makes hard to Model in standard Design Kit

Drawn Data

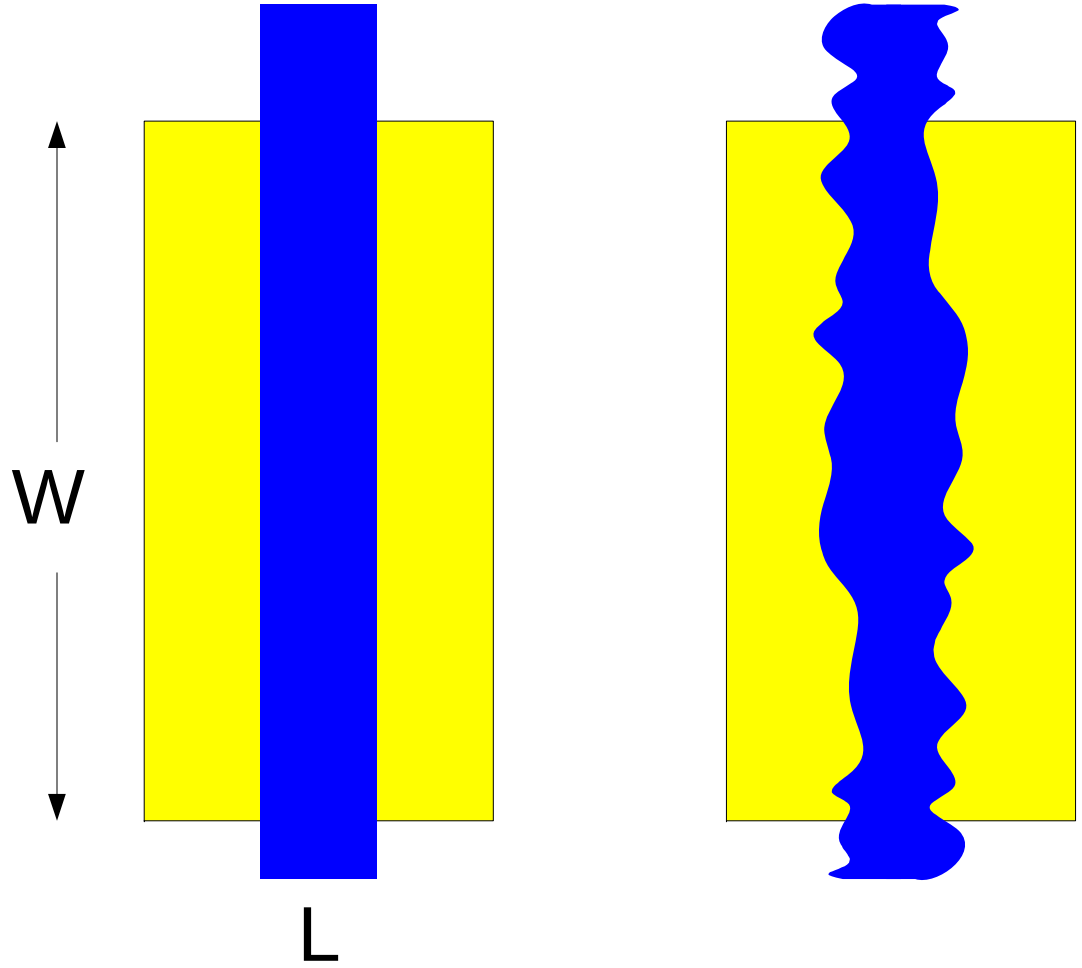


Poly Flare



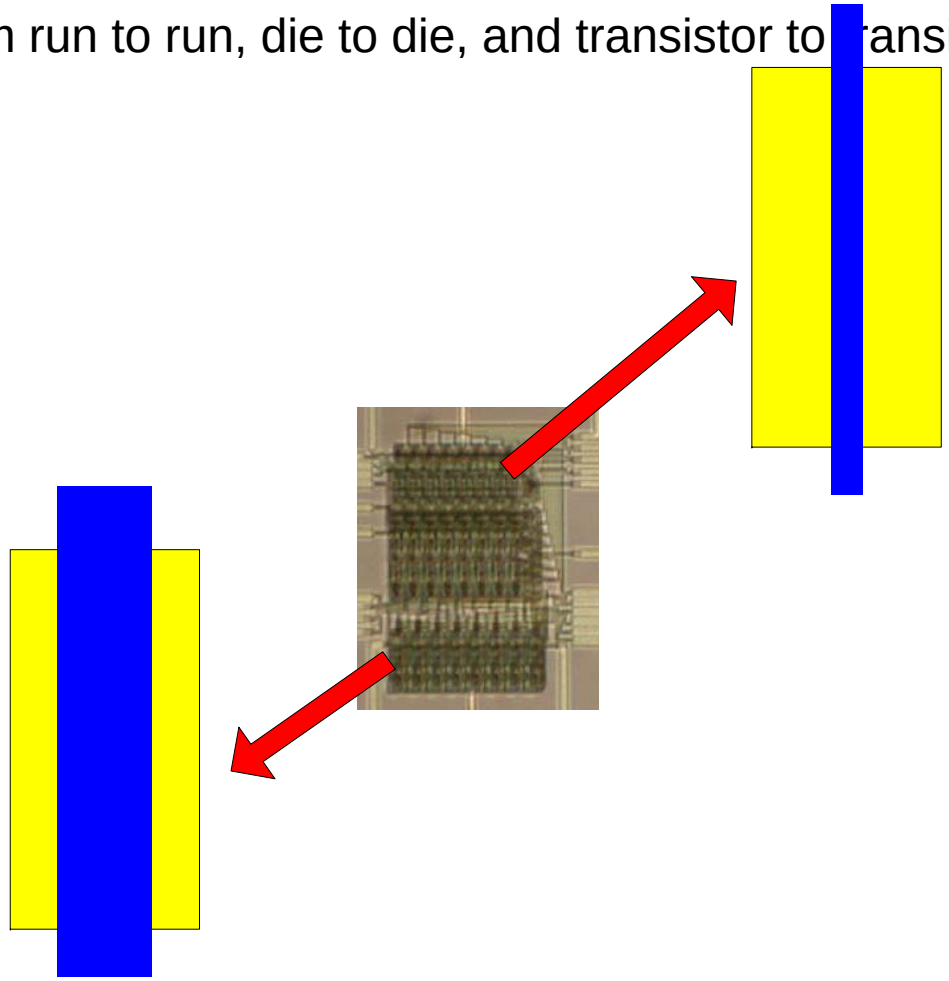
Survey of 90nm transistor issues

- **Line edge roughness**
  - Many transistor parameters depend on L. L varies for the same transistor!



Survey of 90nm transistor issues

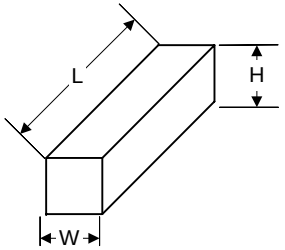
- **Variance in channel length**
  - Can vary from run to run, die to die, and transistor to transistor!
  - Off current
  - VT



Survey of 90nm transistor issues

- **RC Delay**
  - Resistors
    - Resistors impede current flow (R, Ω).
    - Ohm's Law

V=IR



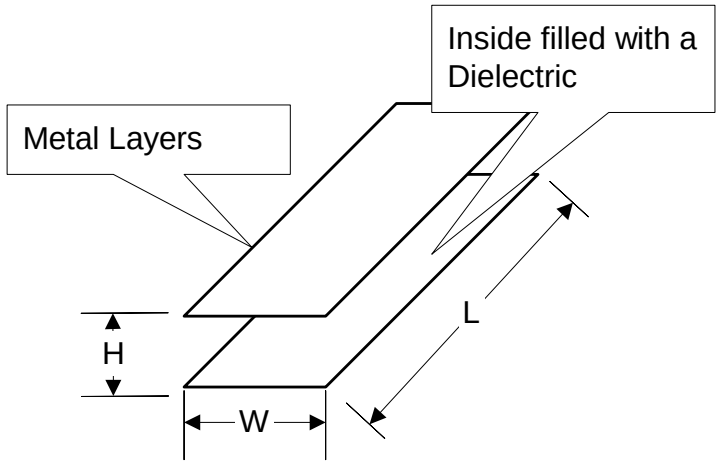
$$R = \rho \times \frac{L}{W \times H}$$

    - Everything has resistance!
    - except super conductors.
    - Resistance increases the time it takes for data to get form one point to another, and causes heat dissipation ($P=IV=I^2R$) as well as a Voltage drop (V=IR)
    - The big issue for the future is that L is remains the same while W is shrunk each successive generation. (Researchers try to keep H the same or higher or use copper (low ρ). g
    - An electric circuit element used to store charge temporarily, consisting in general of two metallic plates separated and insulated from each other by a dielectric (C, Farads).

Survey of 90nm transistor issues

- **RC Delay**
  - Capacitor
    - An electric circuit element used to store charge temporarily, consisting in general of two metallic plates separated and insulated from each other by a dielectric (C, Farads).

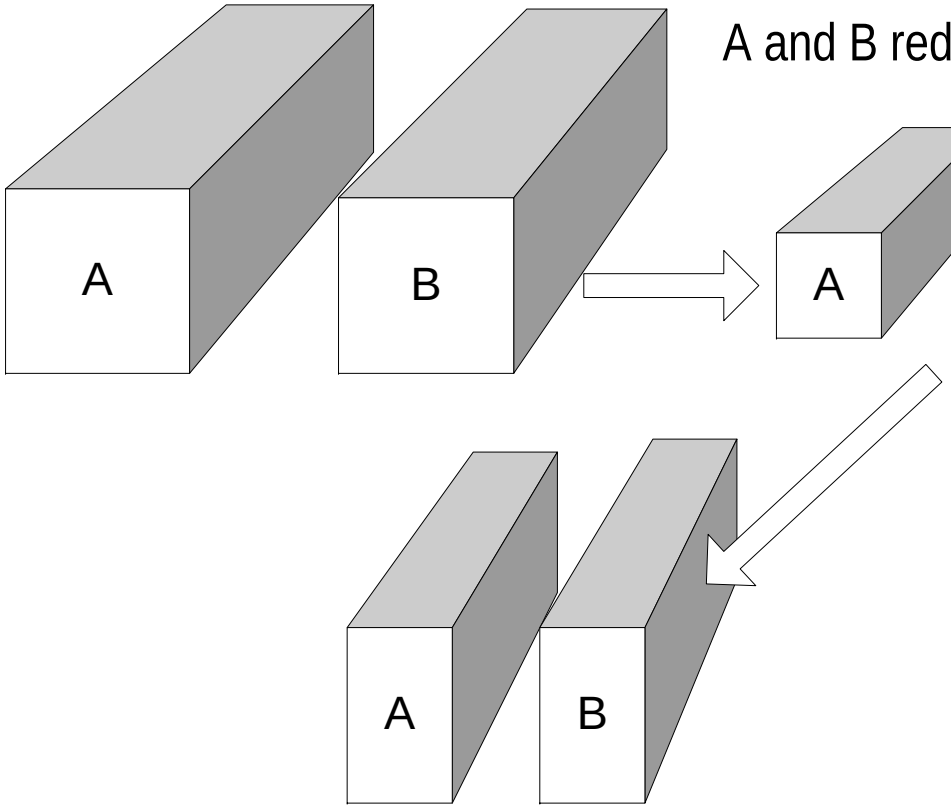
$$C = \frac{\varepsilon_0 \varepsilon_r \times L \times W}{H}$$



  - Delay is how long it takes information to travel from one end of a wire to another.
  - This can be found to be about .69RC.

Survey of 90nm transistor issues

- **RC Scaling Issues**



All dimensions are scaled, C between A and B reduced by scale factor.

R is increased by the scale factor squared.

The height of the metal lines is increased to decrease the resistance.
This increases C!

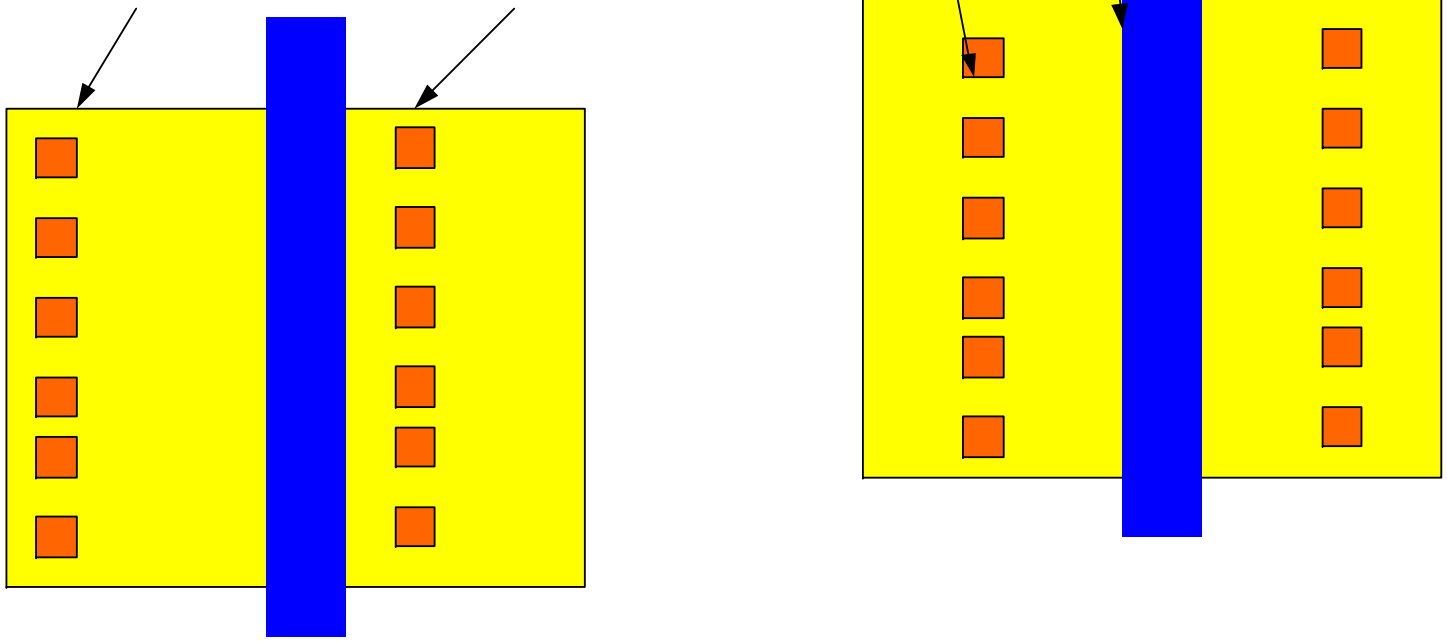
Data lines can now “talk” to each other more easily (cross-talk) and actually change the data.

Survey of 90nm transistor issues

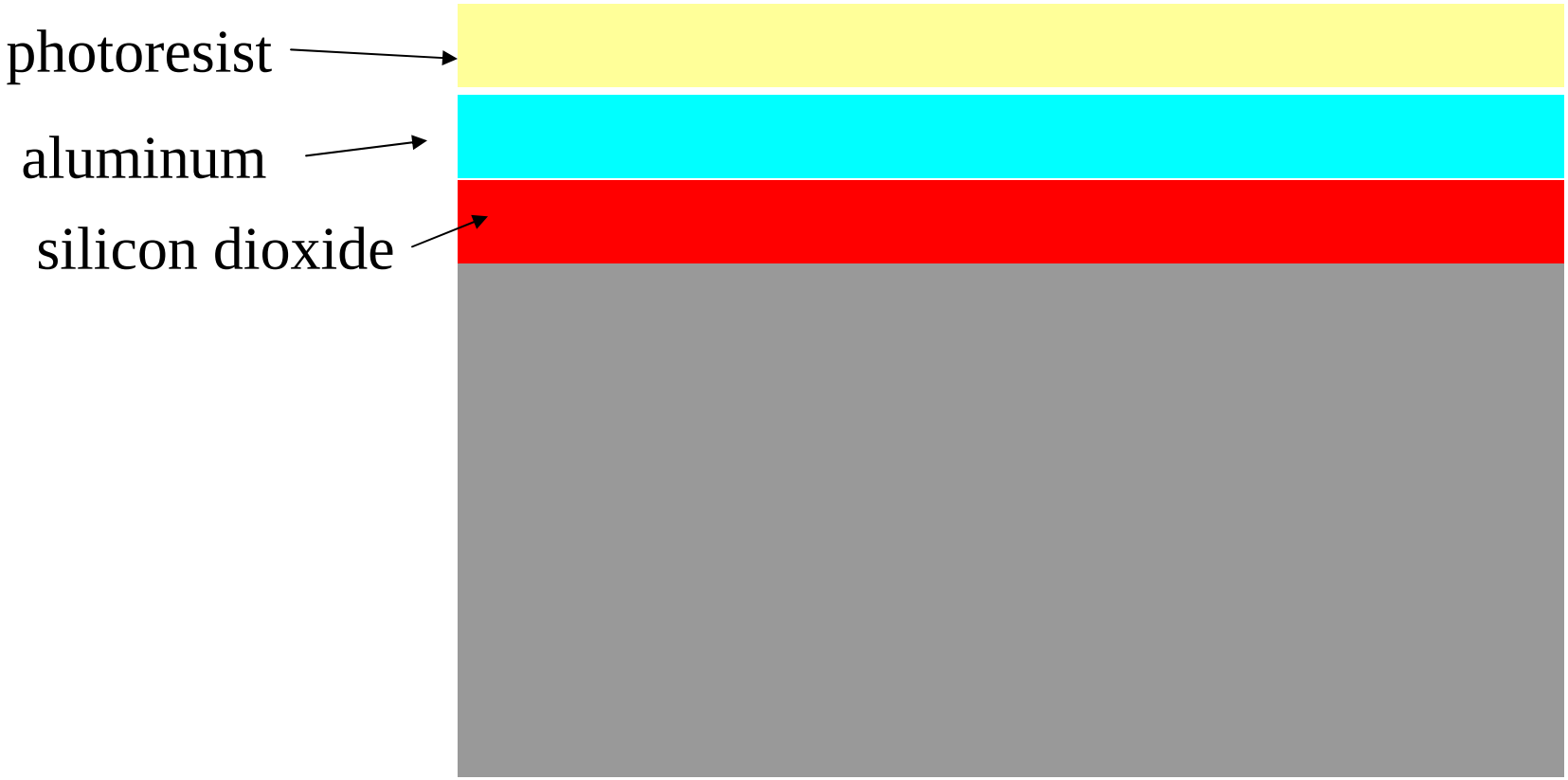
- Contact misalignment impacts the timing on timing.

Resistance is directly proportional to the distance from the contact to the gate from Contact to Gate

Misalighnment causes a one side of the transistor to have more resistance than the other.



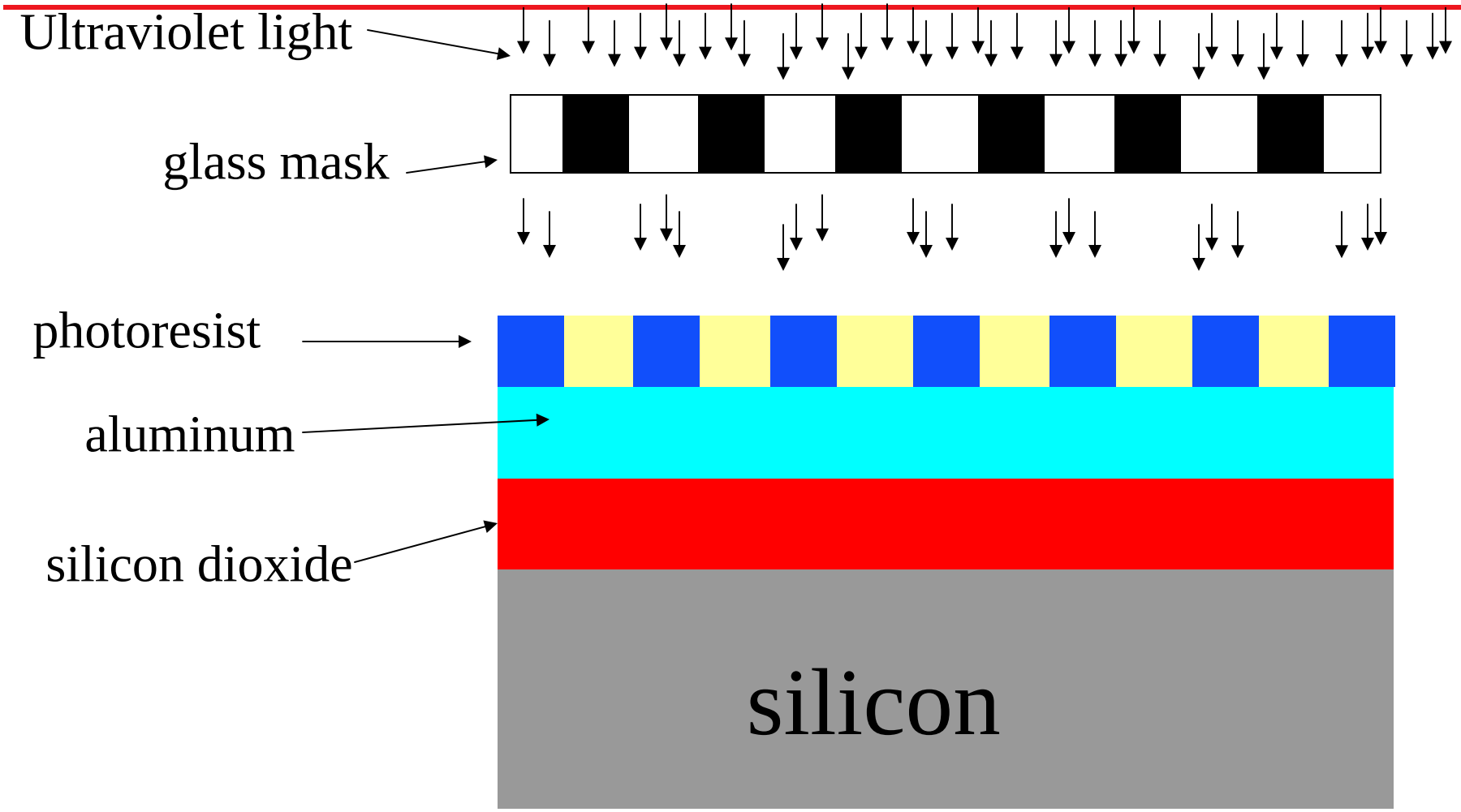
Sample Process to Etch Aluminum



This is the lithography process
Spin on the photoresist

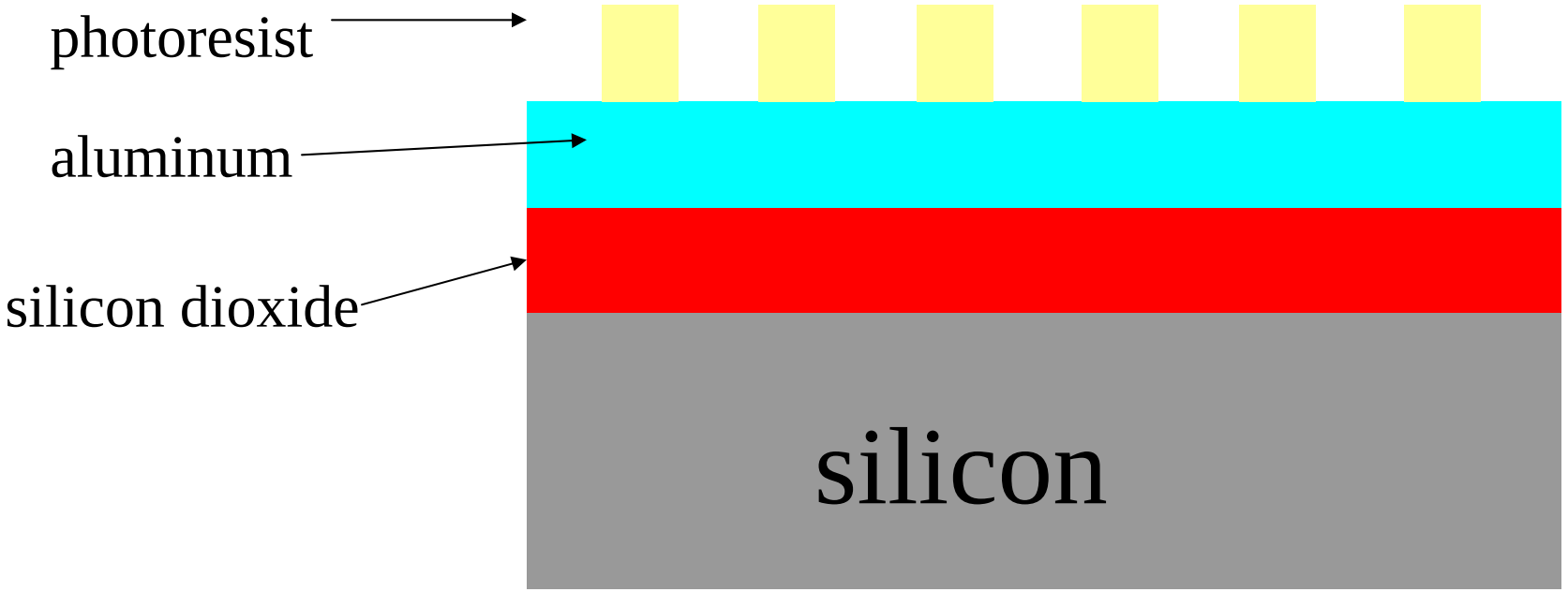
Photo-resist is a light-sensitive polymer.

Sample Process to Etch Aluminum



Expose the photoresist

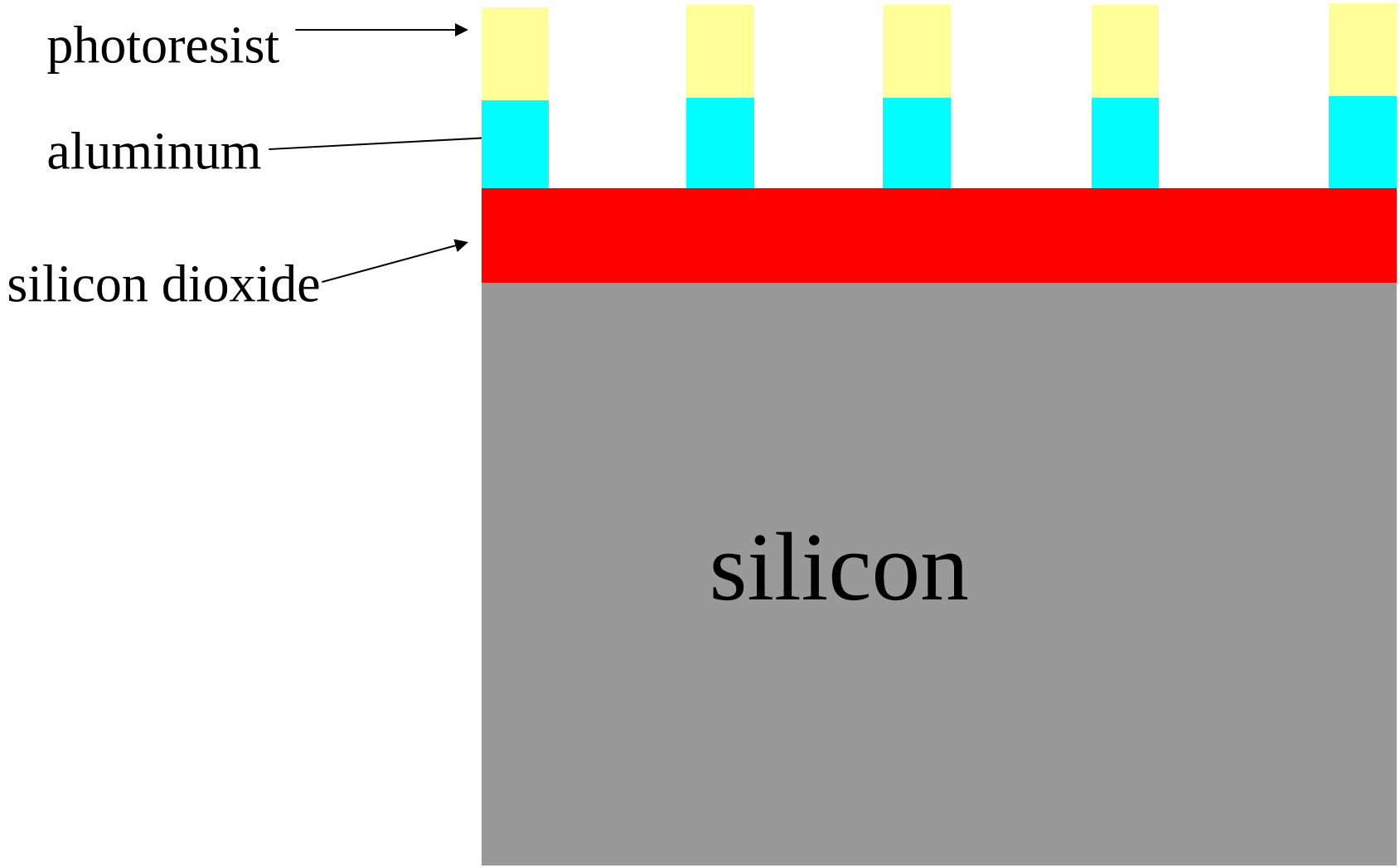
Sample Process to Etch Aluminum



Develop the photoresist

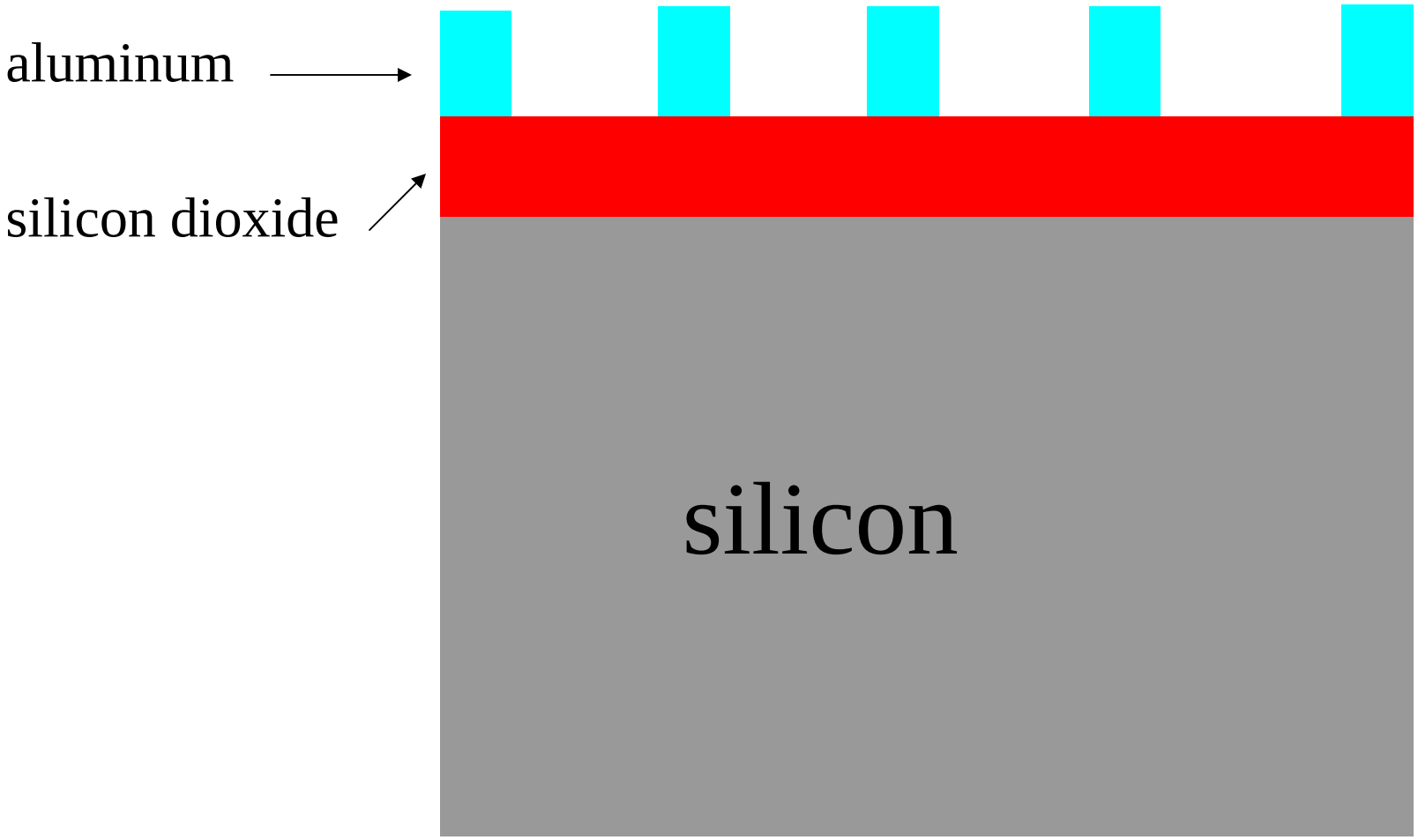
This is the lithography process

Sample Process to Etch Aluminum



Etch the aluminum in acid

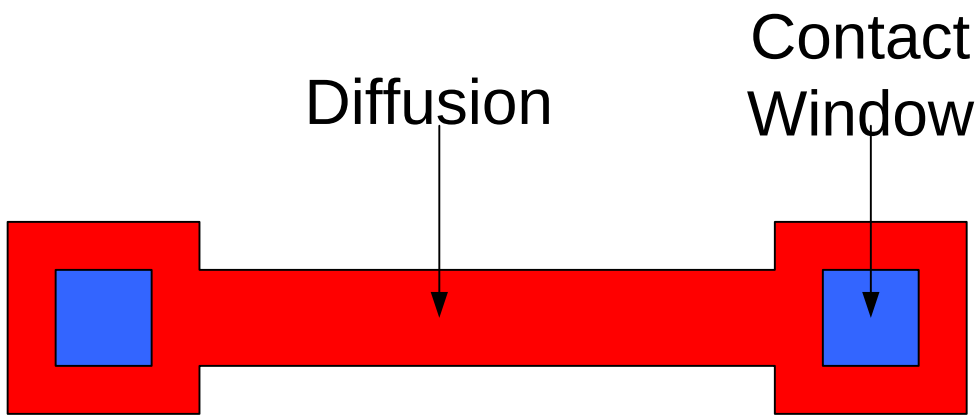
Sample Process to Etch Aluminum



Remove the photoresist in a basic solution

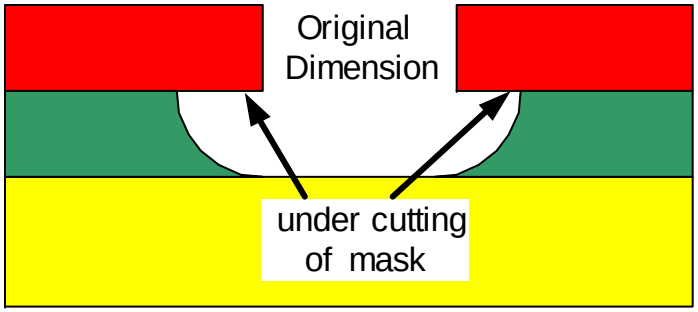
Basics

- Pattern registration
  - How well can a previous mask step be fit to to following mask step.

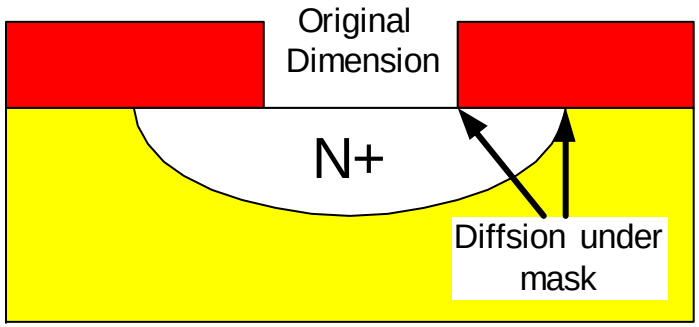


Photolithography Metrics

- Resolution
  - Smallest feature that can be resolved.
  - Ultimately, it is not how thin a line of PR we can pattern, but also how thin we can carry out our process
    - Diffusion under masks
    - Undercutting of masks

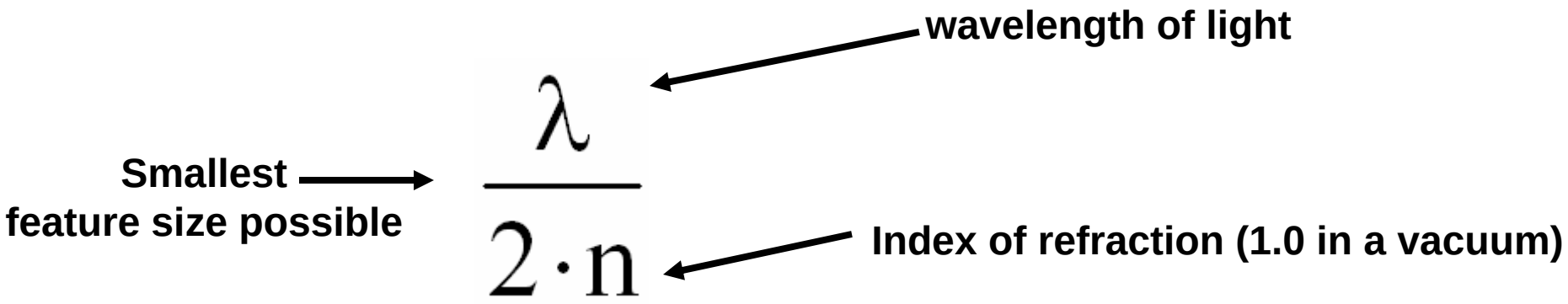


- Pattern registration
- Throughput

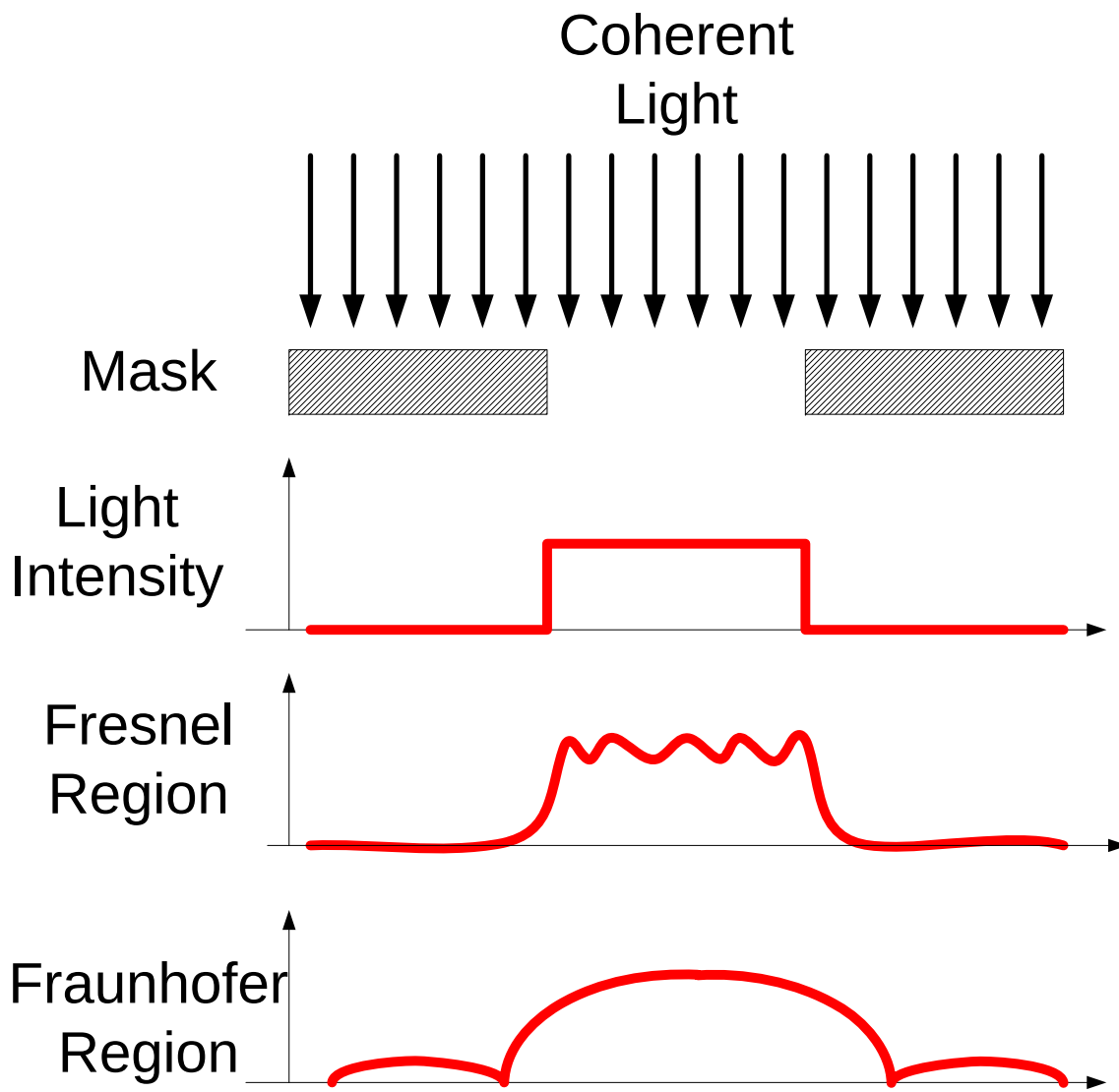


Photolithography

- Nature of light
  - Light can behave as if it were a particle and as if it were a wave.
  - Depending on the type of photolithography exposure system will dictate how you have to treat light in your model.



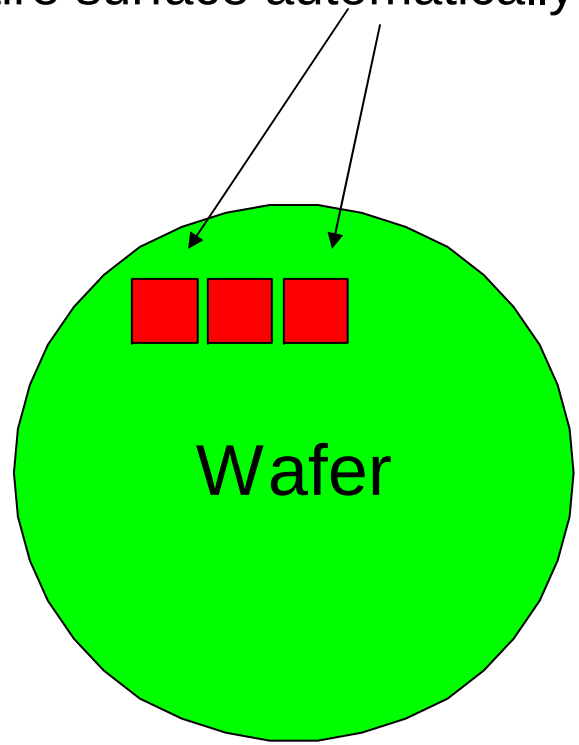
Photolithography

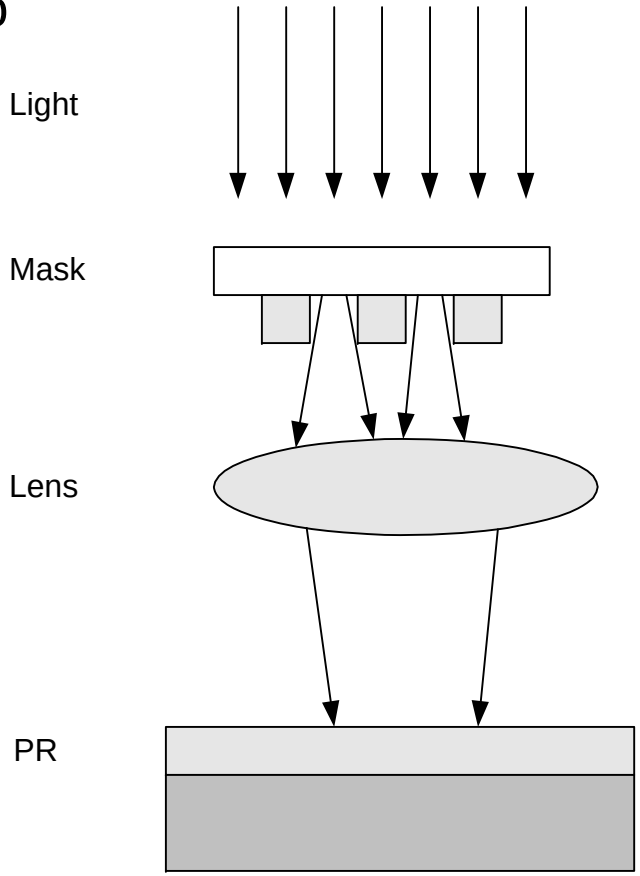


The more intensity that hits the photoresist, the more the photoresist washes away.

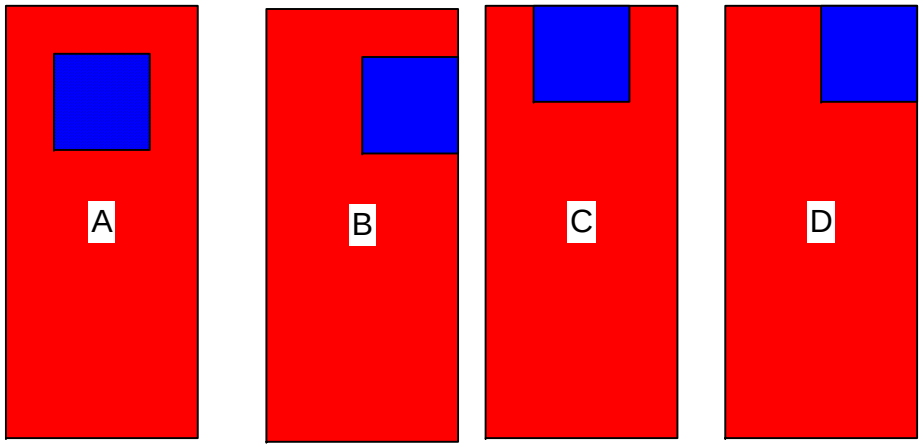
Steppers are exposure systems in which the mask features are reduced though optics to expose the photo resist

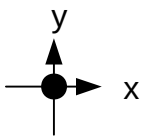
- The Mask is separated from the wafer
- The image is reduced (makes it easier to make a mask)
- The same pattern is stepped over the entire surface automatically





Alignment Errors



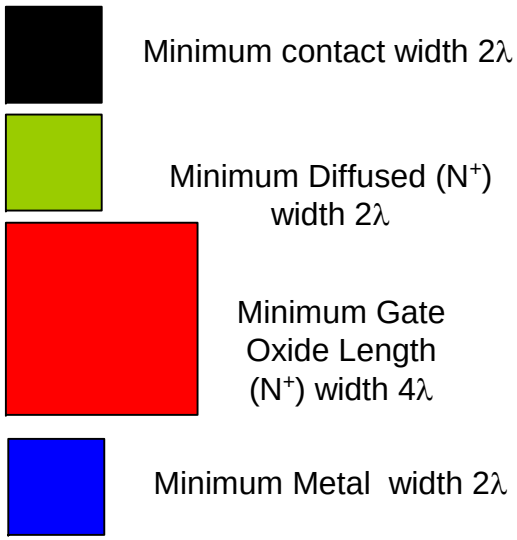


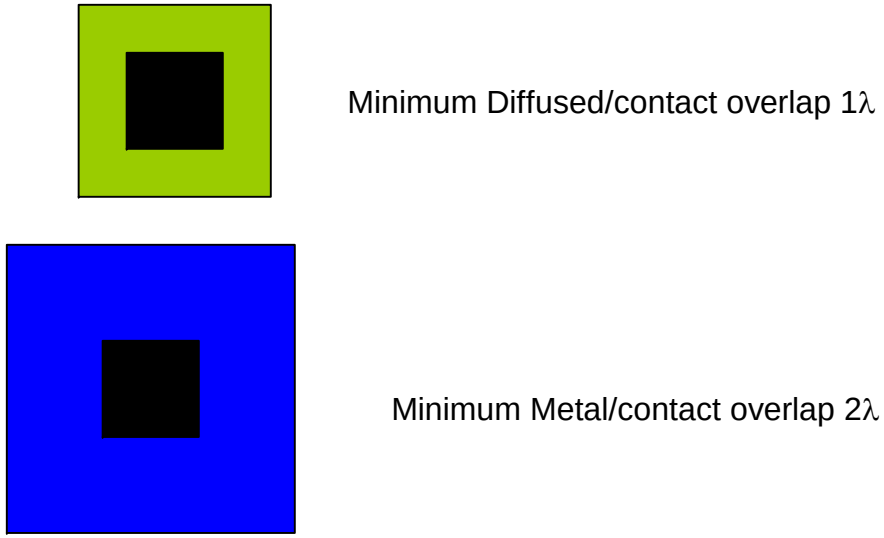
- A- No Errors
- B- Worst Case x misalignment
- C- Worst Case y misalignment
- D- Worst case x and y

We need to have a minimum overlap of the metal to contact to take into account the inherent errors in alignment.

Design Rules for a Process

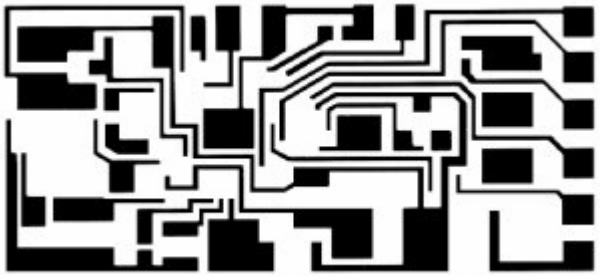
- For high yields we need to have a process that can withstand large process variations
  - ½ of our smallest feature size is equal to λ.
  - λ is equal to 45nm μm

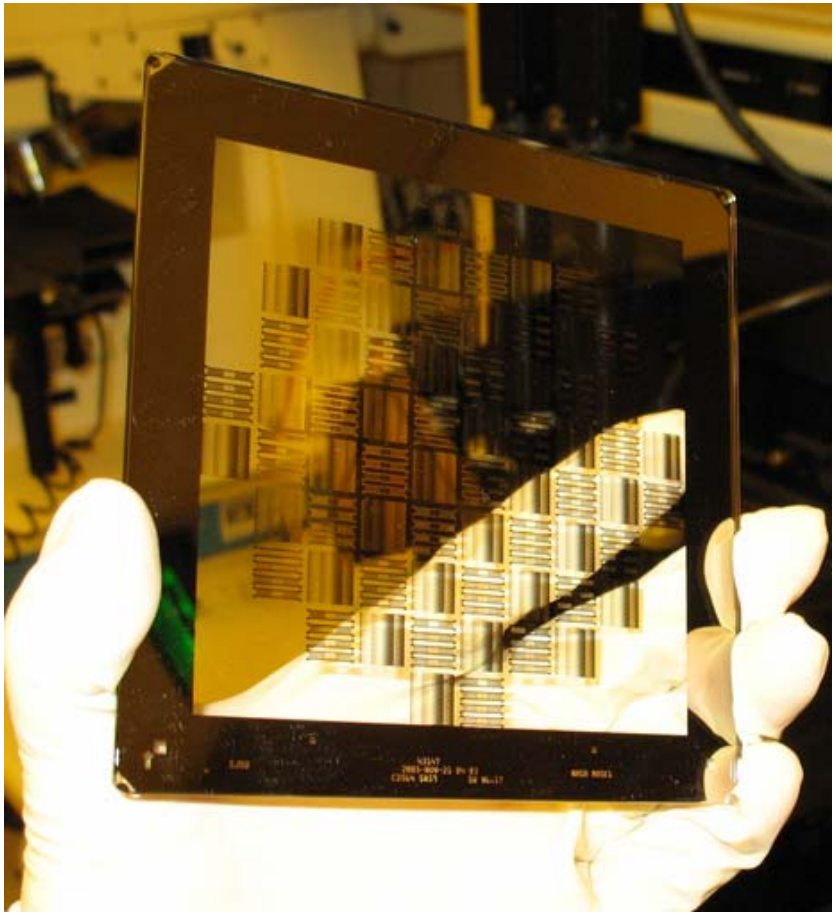




Photomask Overview

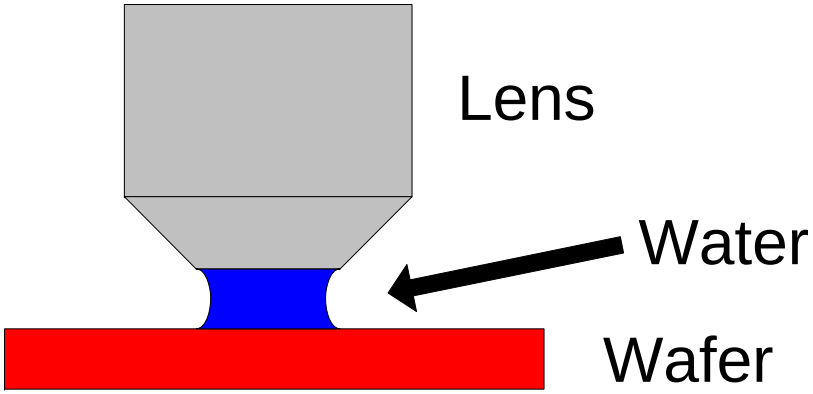
- Made of Quartz
  - Thermal Stability
  - Low loss of light
- Chrome layer patterned with the desired shape
  - Lets light though where you want to wash photo resist away





Future of Immersion Photolithography

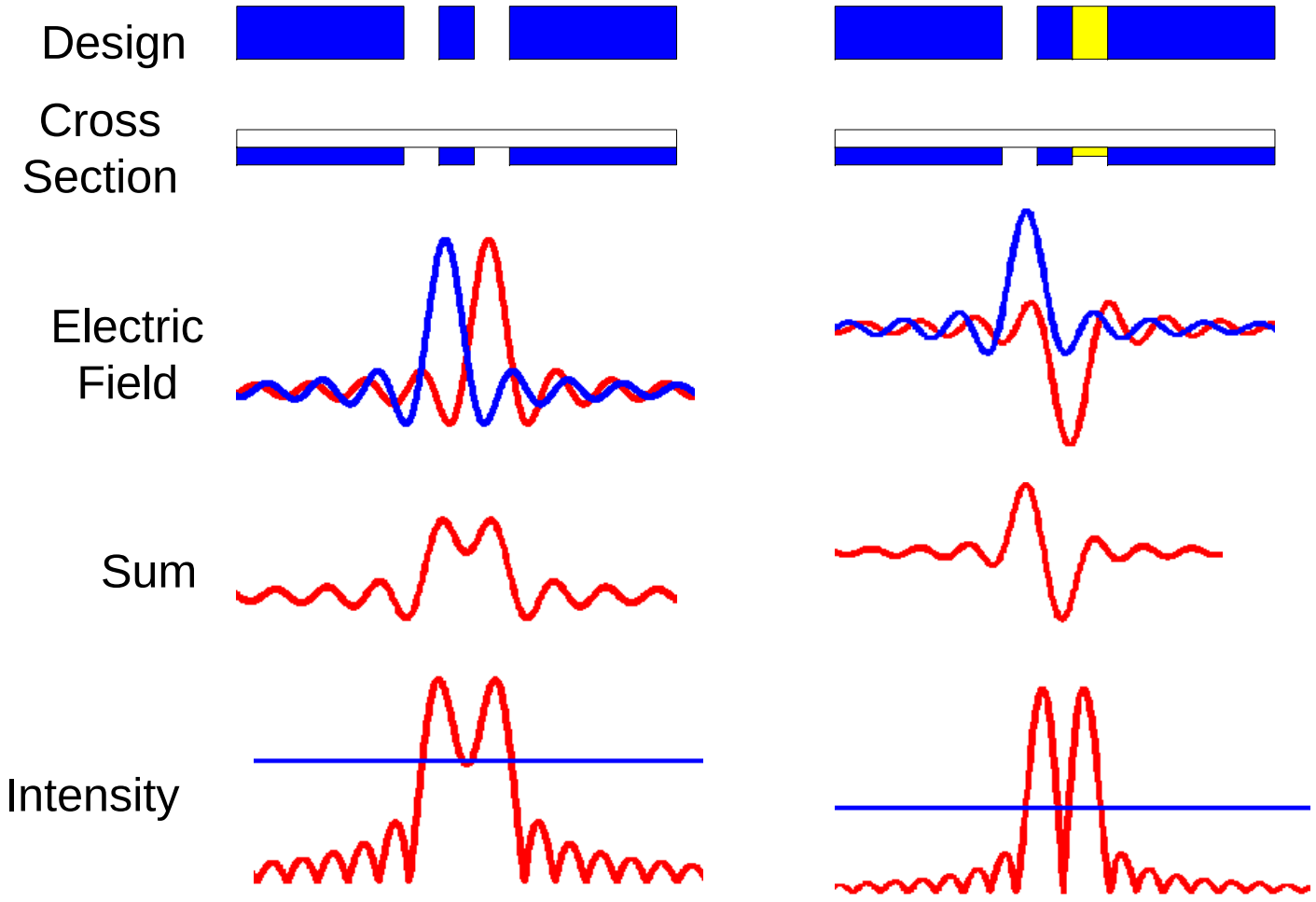
- Currently IBM, UMC Toshiba, IT and possible AMD are using Immersion
  - Use higher index lens n~2
  - Use higher index liquid (n=1.7)
  - New photo resist will be required for below 40nm



$$\frac{\lambda}{2 \cdot n}$$

Phase Shifting Mask

- Phase-shift masks are photo masks that take advantage of the interference generated by phase differences to improve image resolution in photolithography.



Draw the exposed/developed photo resist

Assume that any photo resist that is exposed at a level above the blue line is washed away after the develop step.