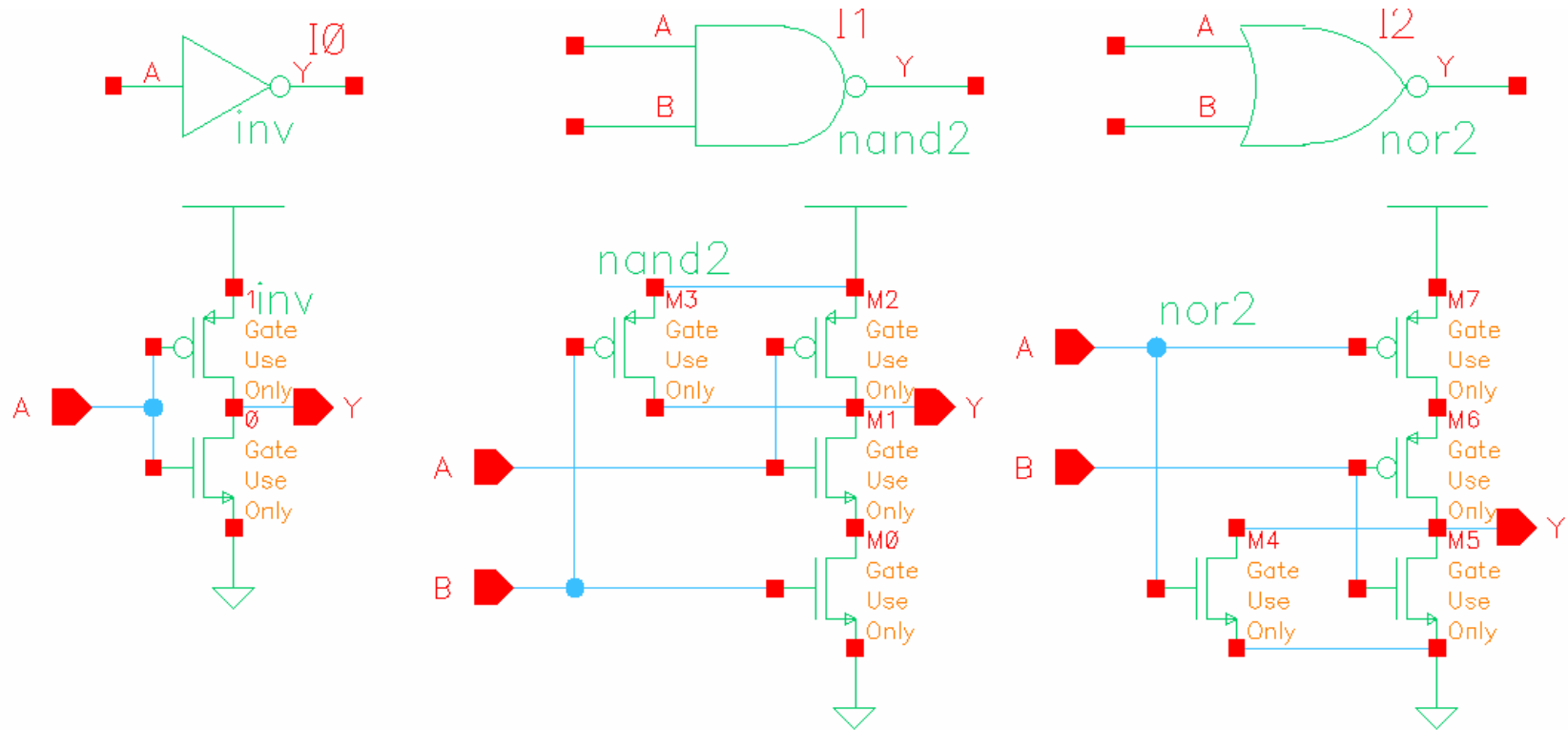


Simple Current Mirror Case Study

D. W. Parent

Static CMOS Digital circuits are easy to understand, model, fabricate, and test.



Signals go rail to rail.

Power Mostly dissipated in switching.

Can logic determine which circuit is stuck "T" or "F". IDDQ testing.

Switch logic easy to verify

This makes testing easier.

$$P = \alpha \cdot C_{Load} \cdot V_{DD} \cdot f$$

The metrics for a digital circuit are straight forward

Logic Function

Speed

Power

Area

Power Density/Cooling requirements

If there are no stuck hi or stuck low circuits after fabrication the circuit can still be sold even if it is slower than the specification.
(Reduced Price)

To model the speed or delay of a static CMOS circuit you try to simply by converting the transistor into an RC network.

$$\tau_{\text{PHL}} = \frac{L_N}{W_N \cdot K_{\text{NP}} \cdot (V_{\text{DD}} - V_{\text{TN}})} \cdot \left[\left[2 \cdot \frac{V_{\text{TN}}}{V_{\text{DD}} - V_{\text{TN}}} + \ln \left[4 \cdot \frac{(V_{\text{DD}} - V_{\text{TN}})}{V_{\text{DD}}} - 1 \right] \right] \right] \cdot C_{\text{LOAD}}$$

$$\tau_{\text{PLH}} = \frac{L_P}{W_P \cdot K_{\text{PP}} \cdot (V_{\text{DD}} + V_{\text{TP}})} \cdot \left[\left[-2 \cdot \frac{V_{\text{TP}}}{V_{\text{DD}} + V_{\text{TP}}} + \ln \left[4 \cdot \frac{(V_{\text{DD}} + V_{\text{TP}})}{V_{\text{DD}}} - 1 \right] \right] \right] \cdot C_{\text{LOAD}}$$

We can rewrite the models more simply:

$$\tau_{\text{PHL}} = \frac{L_N}{W_N} \cdot C_{\text{LOAD}} \cdot A \quad A = \frac{1}{K_{\text{NP}} \cdot (V_{\text{DD}} - V_{\text{TN}})} \cdot \left[\left[2 \cdot \frac{V_{\text{TN}}}{V_{\text{DD}} - V_{\text{TN}}} + \ln \left[4 \cdot \frac{(V_{\text{DD}} - V_{\text{TN}})}{V_{\text{DD}}} - 1 \right] \right] \right]$$

$$\tau_{\text{PLH}} = \frac{L_P}{W_P} \cdot C_{\text{LOAD}} \cdot B \quad B = \frac{1}{K_{\text{PP}} \cdot (V_{\text{DD}} + V_{\text{TP}})} \cdot \left[\left[-2 \cdot \frac{V_{\text{TP}}}{V_{\text{DD}} + V_{\text{TP}}} + \ln \left[4 \cdot \frac{(V_{\text{DD}} + V_{\text{TP}})}{V_{\text{DD}}} - 1 \right] \right] \right]$$

$$K_{\text{NP}} = \mu_N \cdot C_{\text{oxide}} \quad K_{\text{PP}} = \mu_P \cdot C_{\text{oxide}}$$

The metrics of an analog circuit are easy to understand but hard to design for.

Power

Area

Matching

Gain

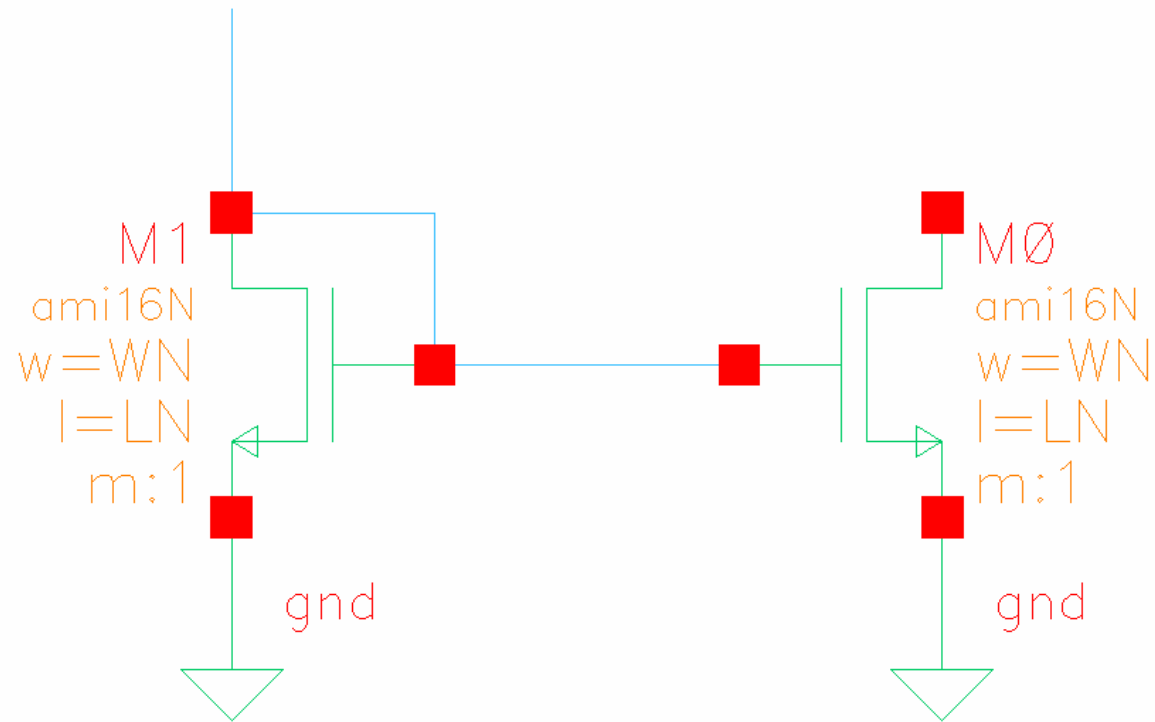
Bandwidth

Filter Characteristics.

FT

The equations for design are all interrelated, and sometimes no closed form solution exist.

To design a simple current mirror, we need to know V_T , K_N , λ



I_{IN} , I_{OUT} , R_{OUT} , and Area are all specifications

Current Mirrors operate in Saturation

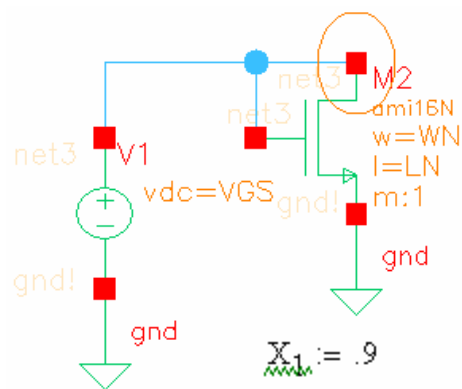
$$m := 6.82 \cdot 10^{-3} \frac{\text{A}}{\text{V}^{\frac{1}{2}}}$$

$$K_N := 2 \cdot m^2$$

$$K_N = 9.302 \times 10^{-5} \frac{\text{A}}{\text{V}^2}$$

$$\beta_N := K_N$$

$$W=L=15\mu\text{m}$$



$$X_1 := .9$$

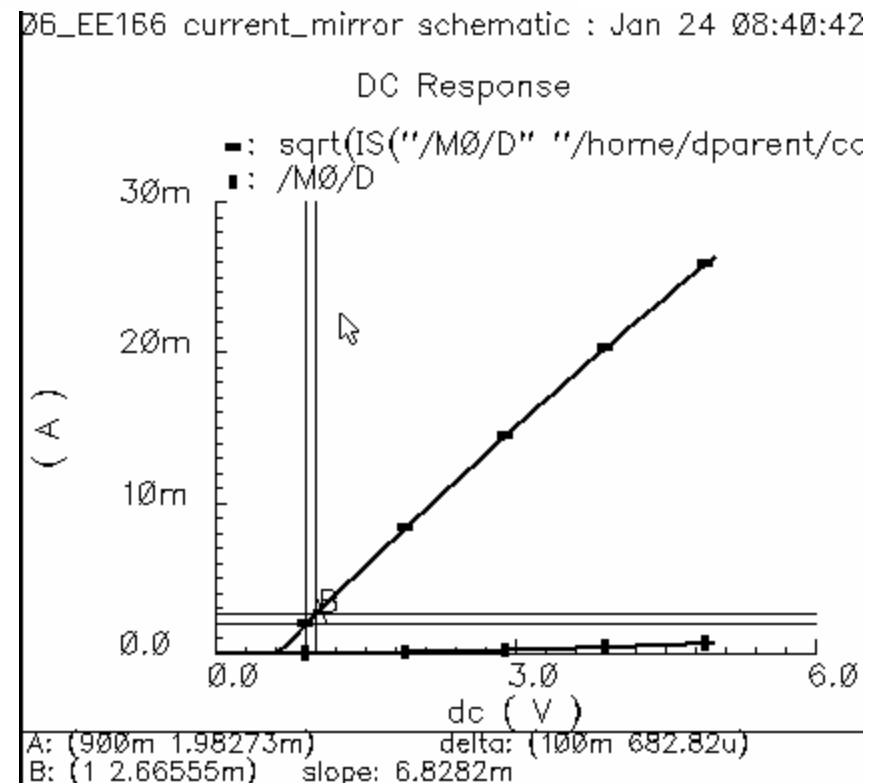
$$Y_1 := 1.98 \times 10^{-3}$$

$$m := 6.82 \times 10^{-3}$$

$$b := Y_1 - X_1 \cdot m \quad b = -4.158 \times 10^{-3}$$

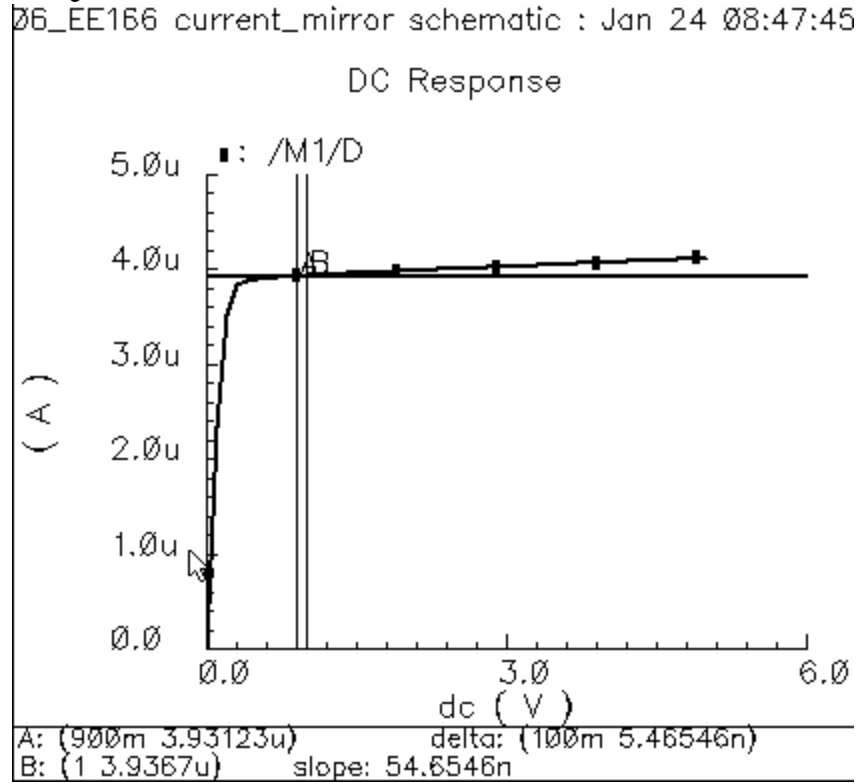
$$V_T := \frac{-b}{m}$$

$$V_T = 0.61$$



Extract near desired VGS!

λ can be quickly found from an ID, VDS curve



$\lambda = .014$

$$X_1 := .9$$

$$Y_1 := 3.93 \cdot 10^{-6}$$

$$m := 54.65 \cdot 10^{-9}$$

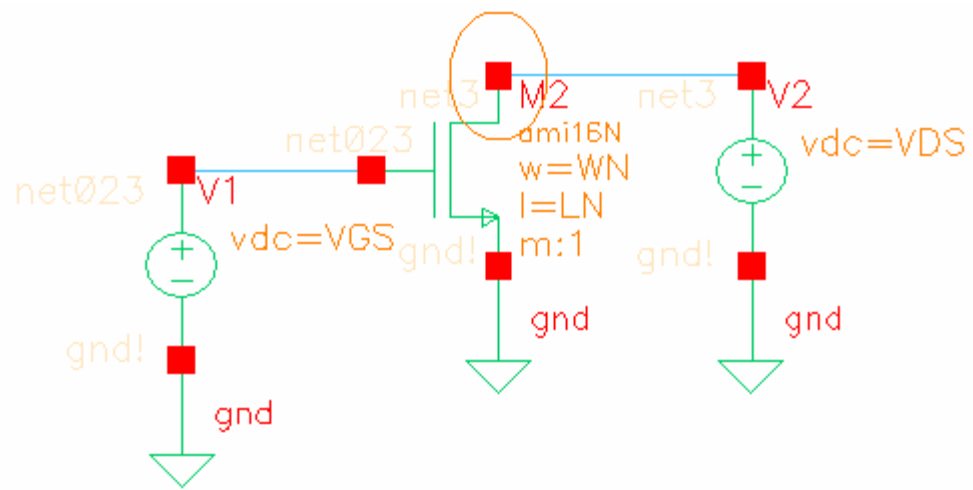
$$b := Y_1 - X_1 \cdot m \quad b = 3.881 \times 10^{-6}$$

$$X_2 := \frac{-b}{m}$$

$$X_1 = -71.012$$

$$V_{A_1} := X_1$$

$$\lambda := \frac{1}{|V_{A_1}|} \quad \lambda = 0.014$$

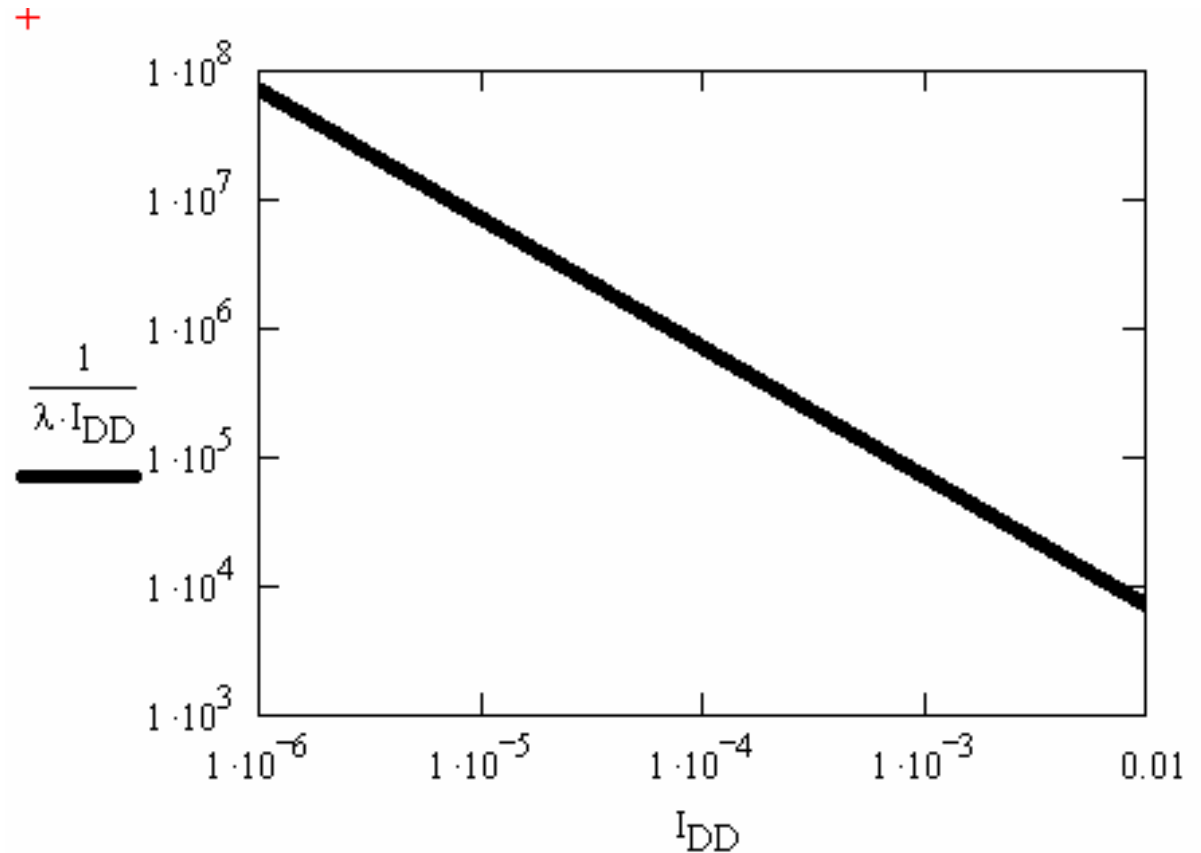


We are ready to begin?

Specification:

IREF=100uA
IOUT=100uA
Ro=10⁷ Ohms
Maximum
Output
swing

$$r_o = \frac{1}{\lambda \cdot I_D}$$



The Ro at the IOUT we want
is less 10⁶ Ω!

Which is more important Ro or IREF? New spec: Ro >10⁶ Ω 9

To design W, we need to know VGS. How do we pick it in a reasonable manner?

$$V_{Tn} := .6V$$

$$R_o := 10^6 \Omega$$

$$\lambda := .014V^{-1}$$

$$I_{REF} := \frac{1}{R_o \cdot \lambda} \quad I_{REF} = 7.143 \times 10^{-5} A$$

$$\beta_N := 9.3 \cdot 10^{-5} \frac{A}{V^2}$$

$$L_{N1} := 15 \cdot 10^{-4} \text{ cm}$$

$$W_N := \frac{I_{REF} \cdot 2 \cdot L_N}{\beta_N \cdot (V_{GS} - V_T)^2} \quad W_N = 2.56 \times 10^{-2} \text{ cm}$$

$$V_{GS} := 0.9V$$

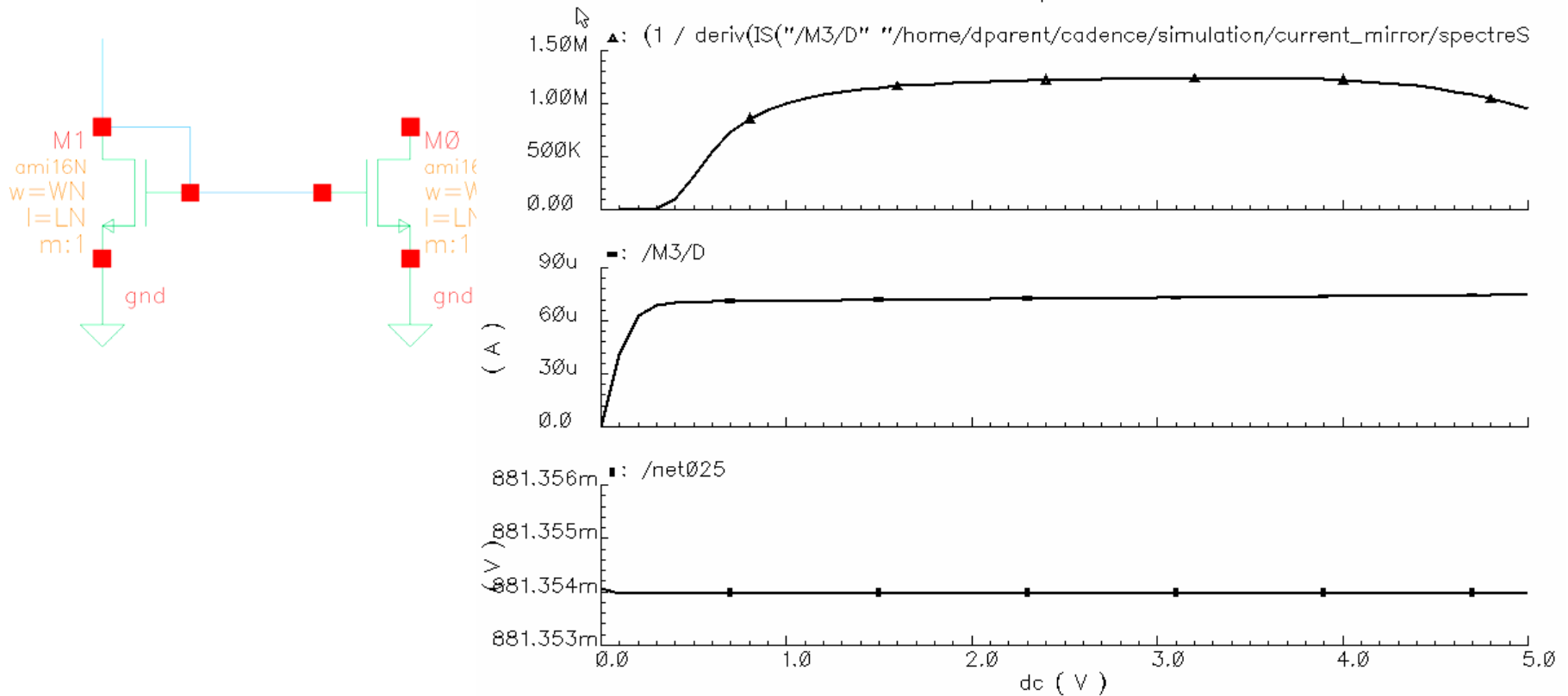
Note we had to assume a VGS or level of inversion.
0.3V above VT is a classic assumption.

DC Results of Current Mirror

$W=256\mu$, $L=15\mu$, $I_{REF}=71\mu$

AMI06_EE166 current_mirror schematic : Jan 24 08:57:33 2008

DC Response

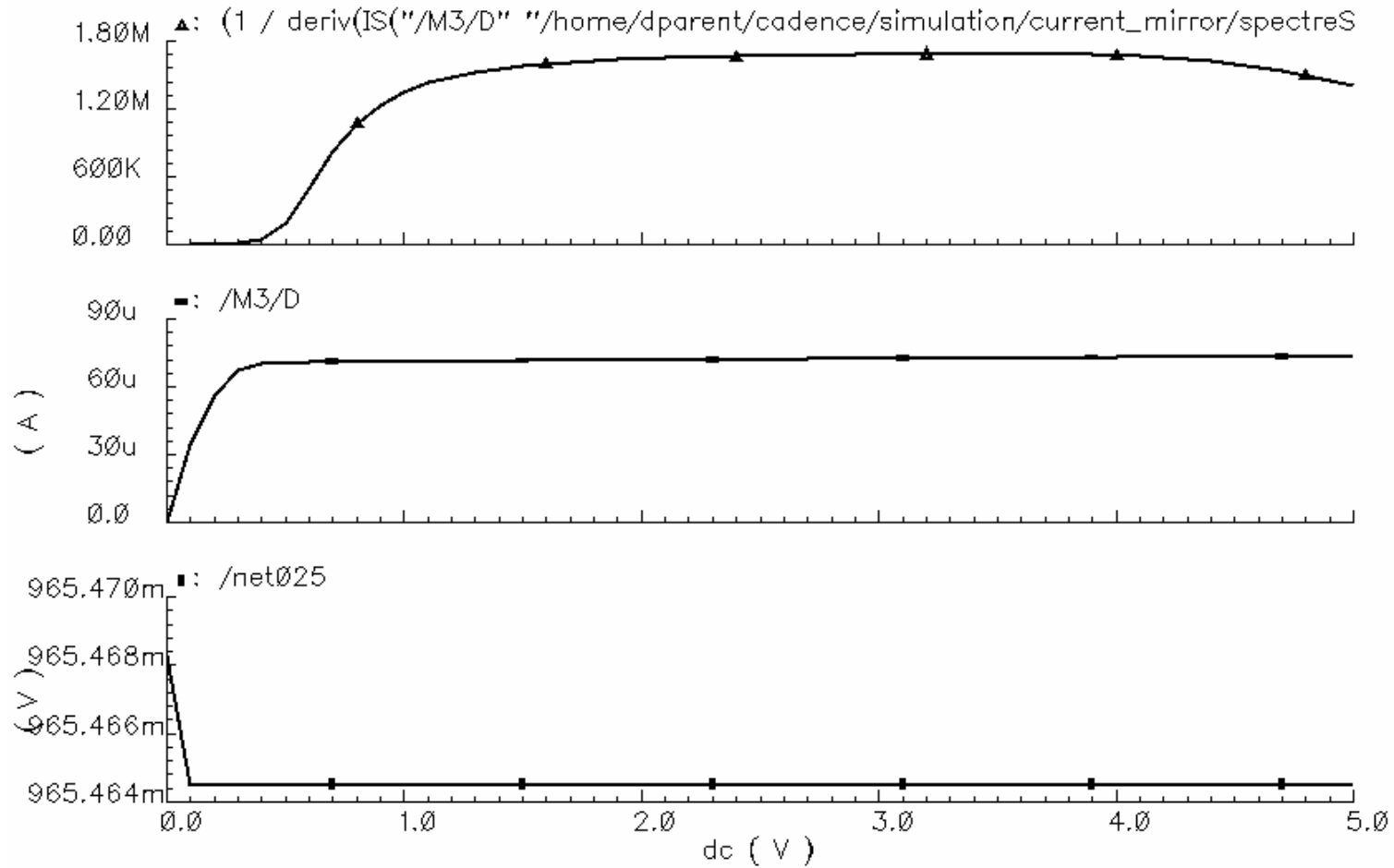


R_o within 10%, V_{GS} was measured to be .88V

We can increase R_o by increasing LN to 25 μm ($I_{REF}=71\mu$, $W=256\mu\text{m}$)

AMI06_EE166 current_mirror schematic : Jan 24 09:02:03 2008

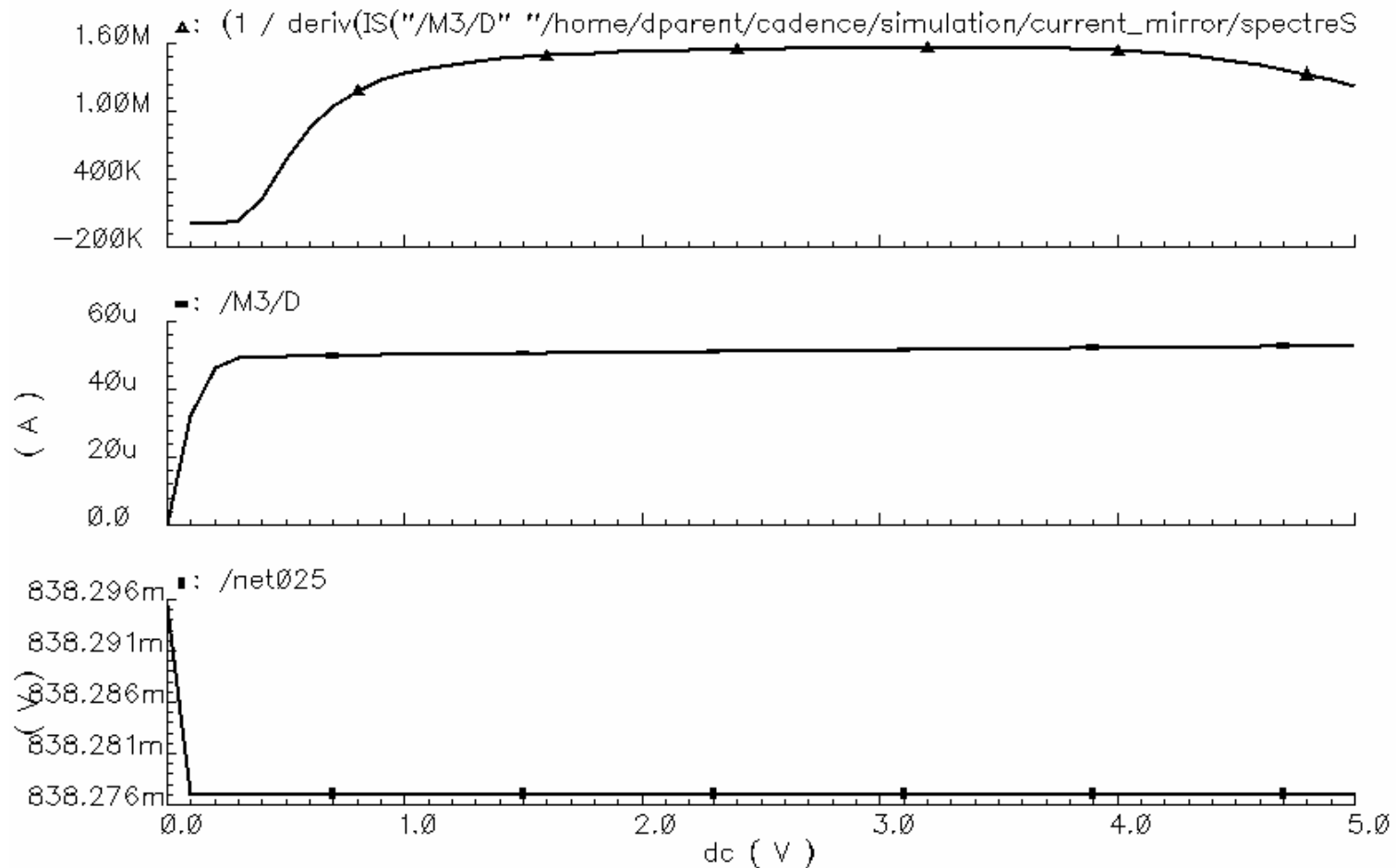
DC Response



We can increase R_o by Decreasing IFEF to 50 μ A ($L=15\mu$ m, $W=256\mu$ m)

AMI06_EE166 current_mirror schematic : Jan 24 09:05:15 2008

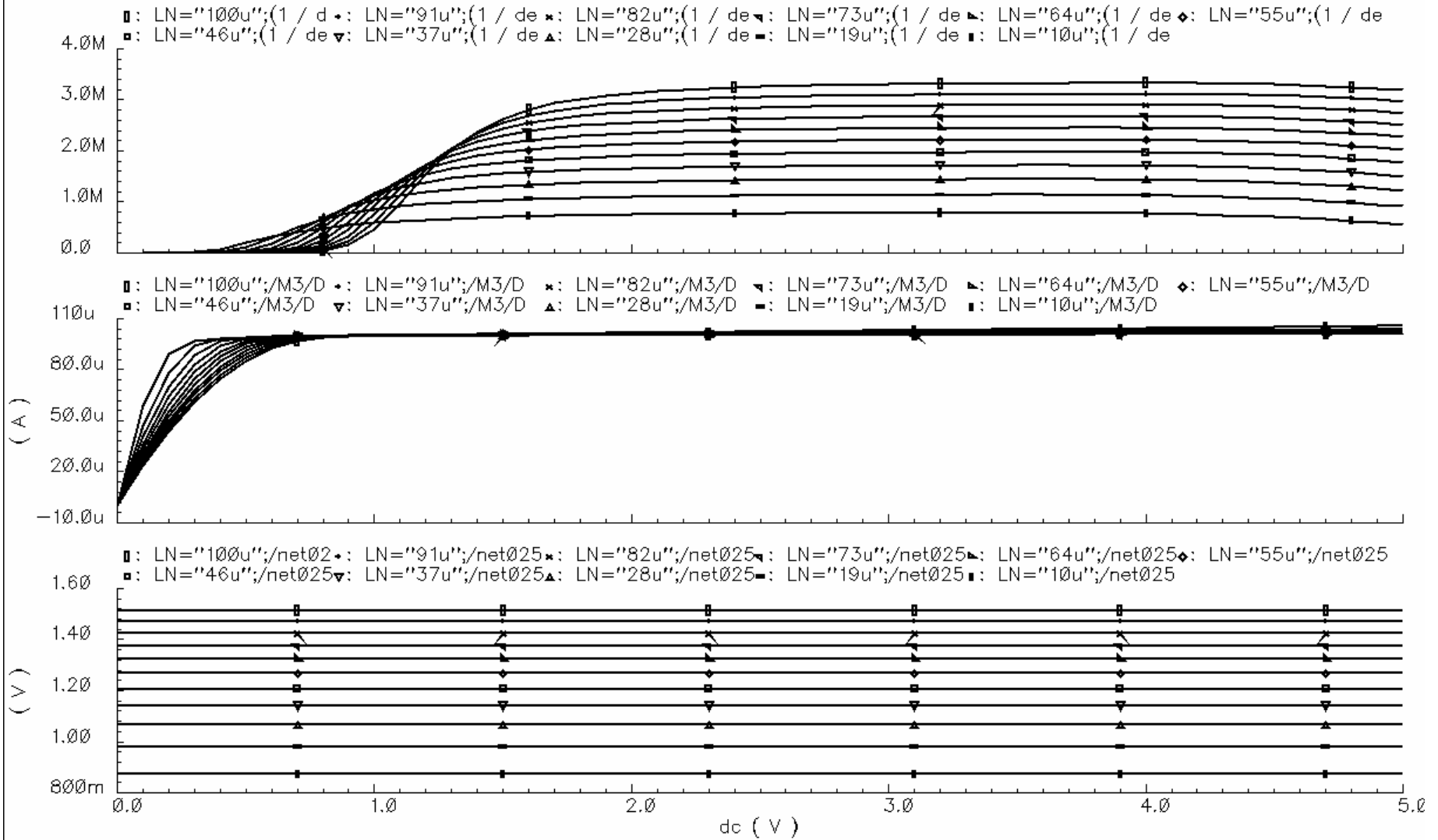
DC Response



Be Careful!

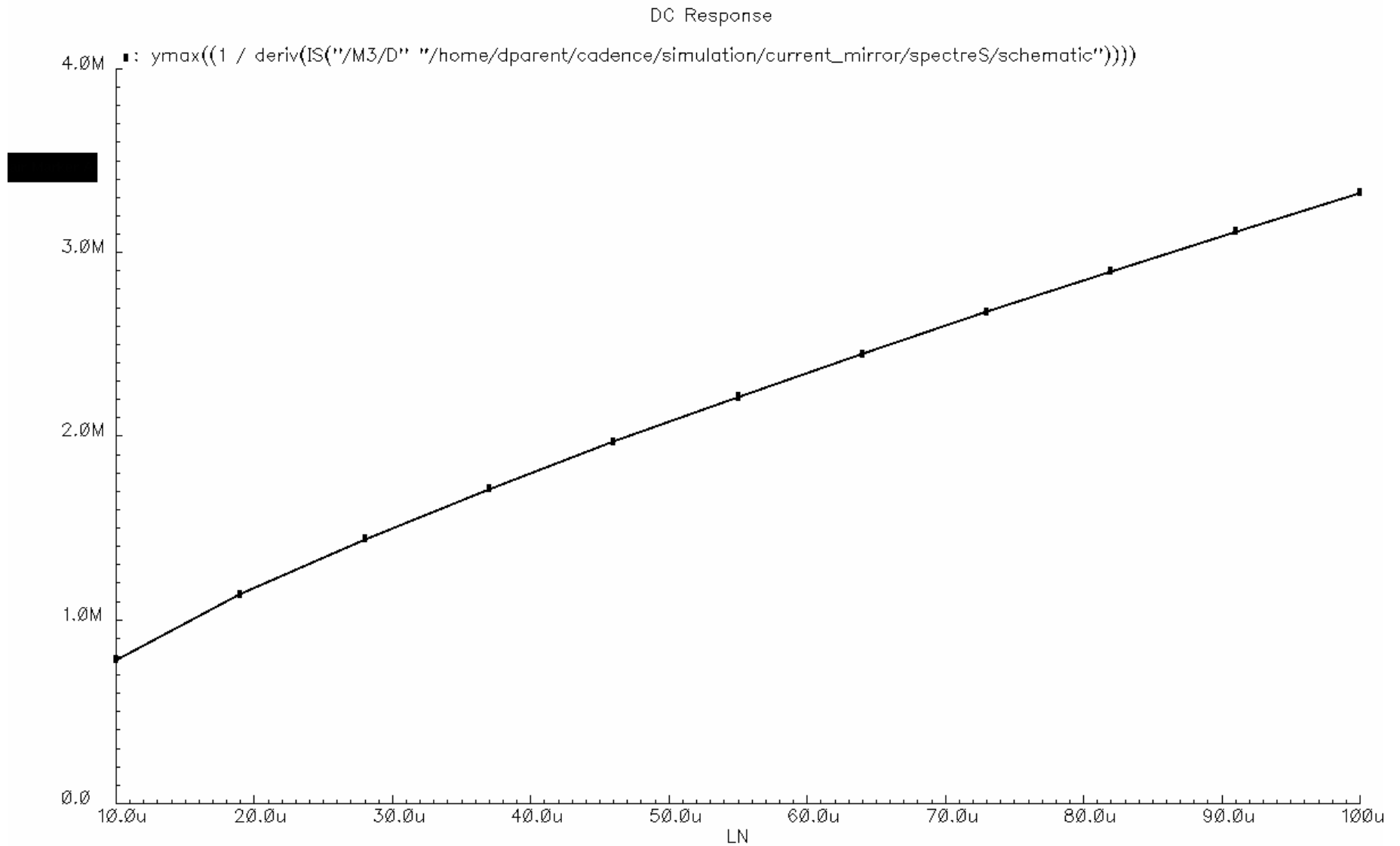
- Note how VGS changed when we changed IREF or L.
- Same for W
- We extracted right around our operating point.
- There are some IREF RO, VGS combinations we cannot achieve!

DC Response



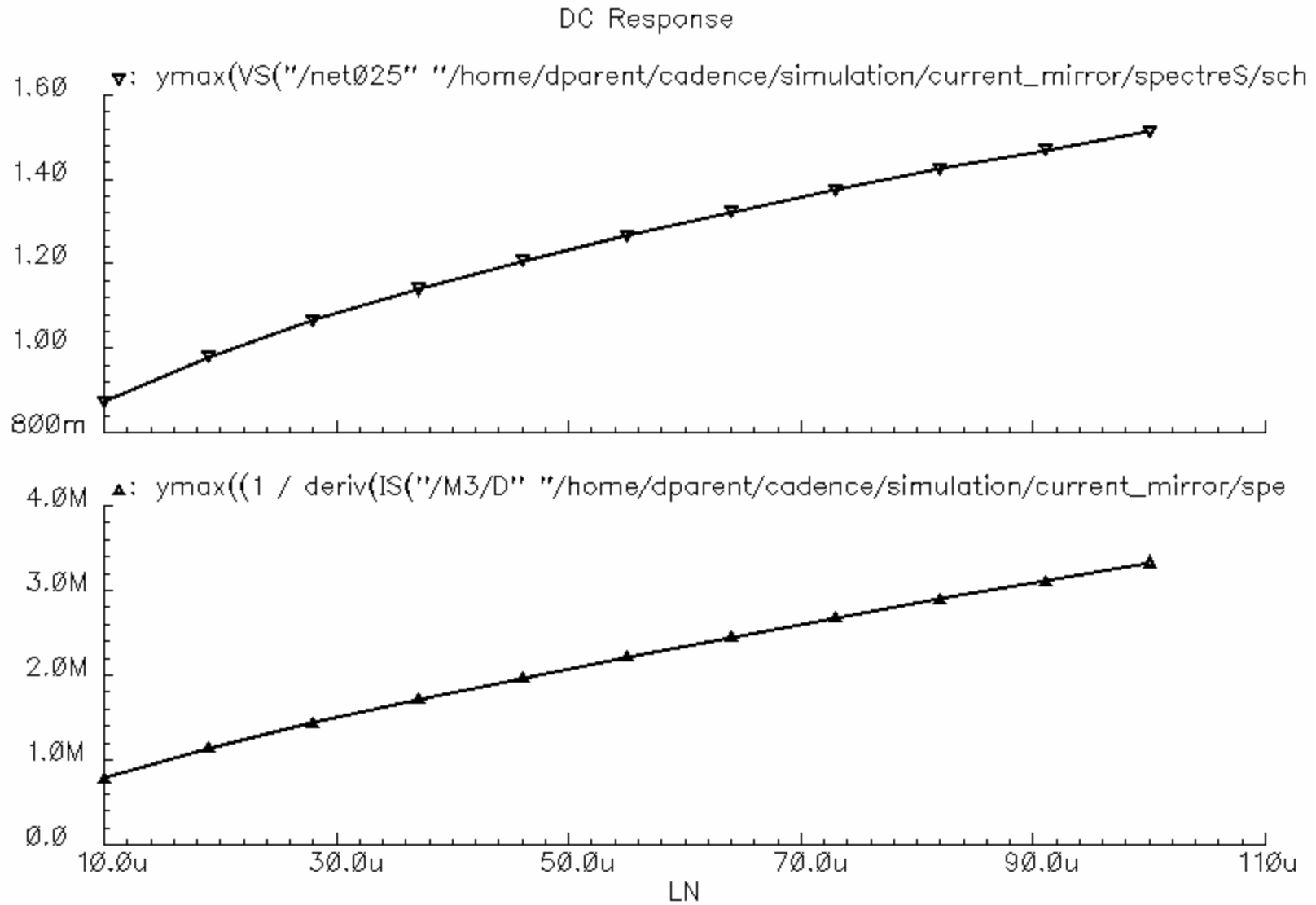
IREF=100u, W=256um, L from 10um to 100um.

There is a practical limit to RO for a given IREF.

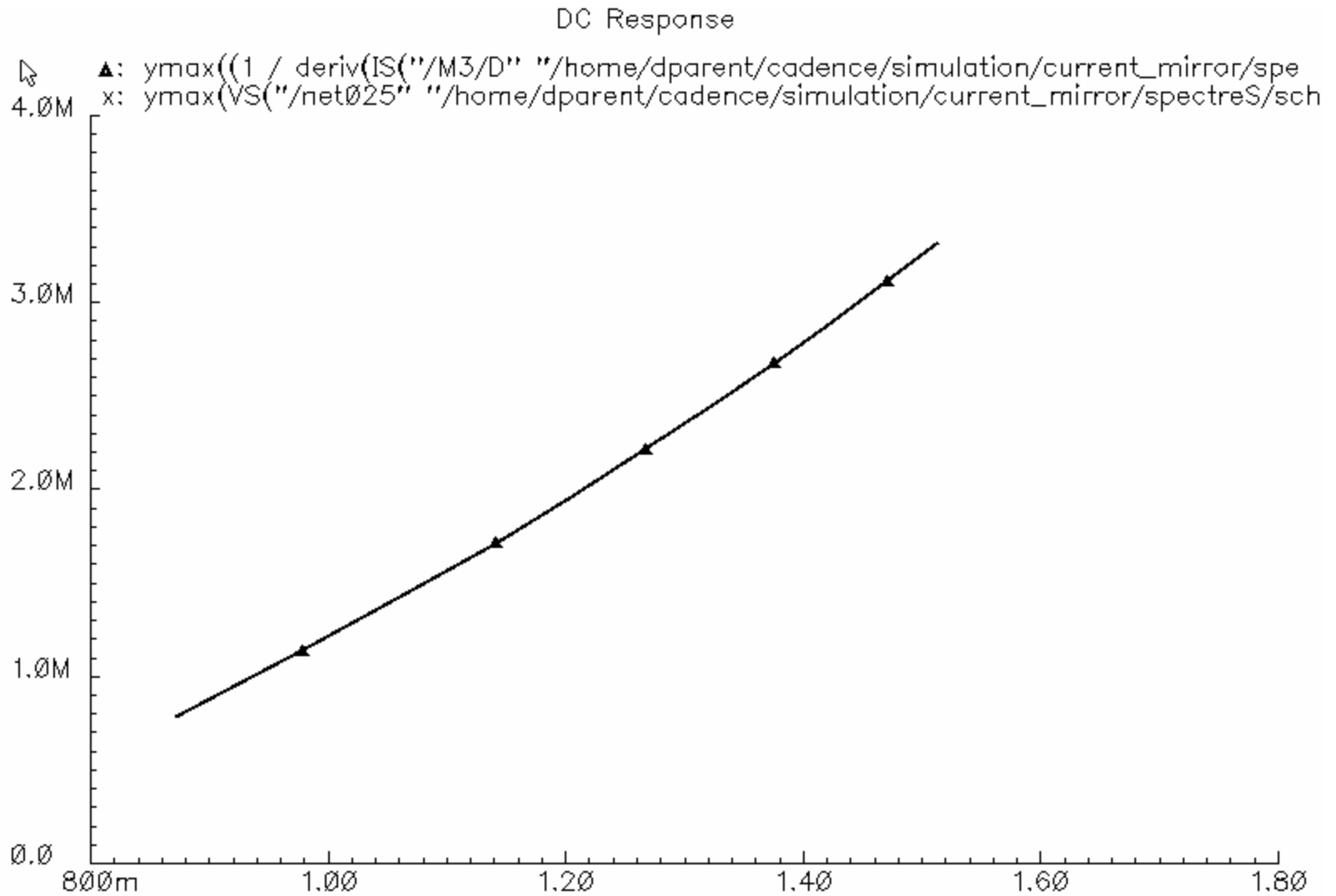


IREF=100uA, W=256um

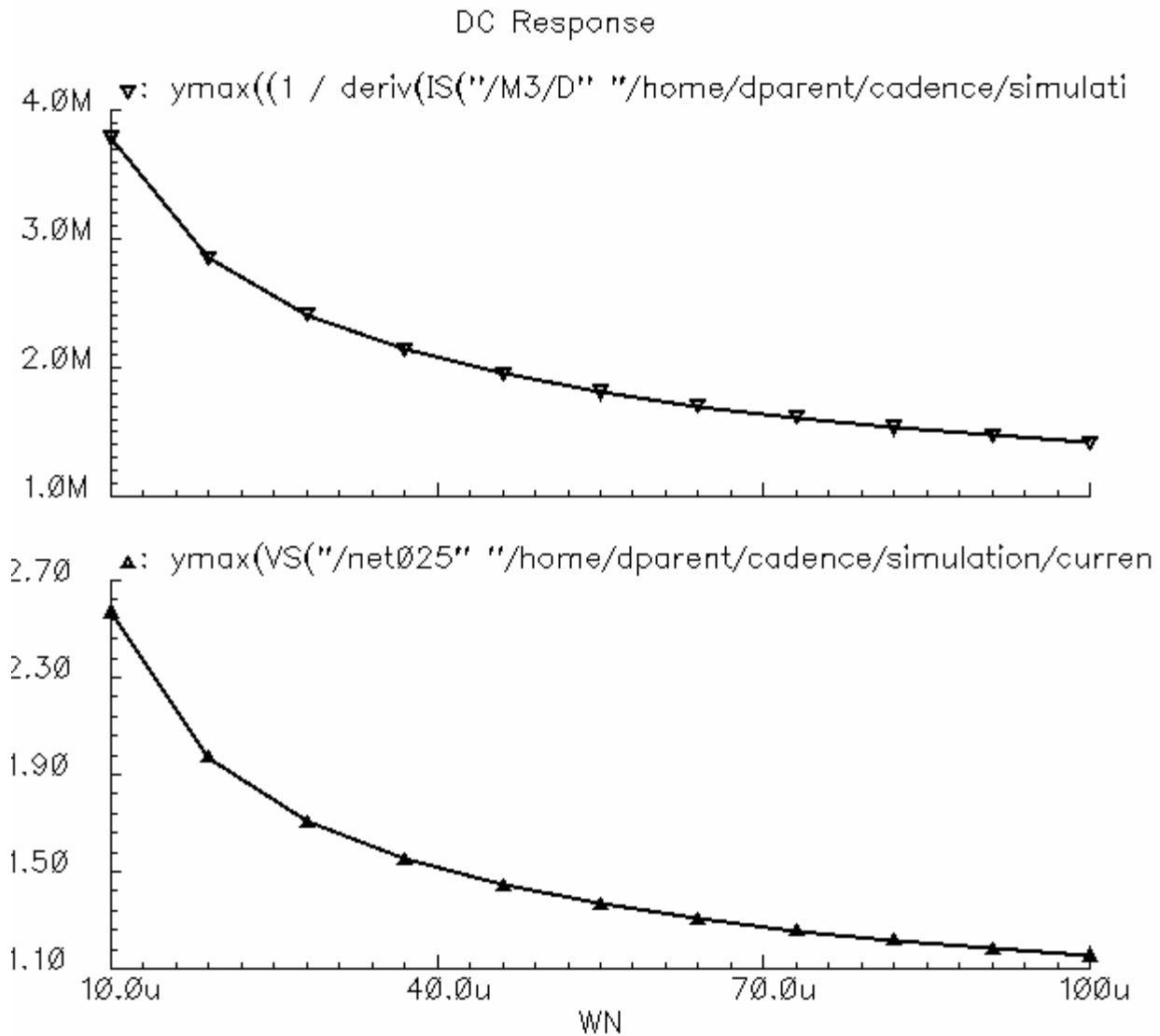
VGS and RO vs. L for fixed W=256um and IREF=100uA



RO vs VGS



VGS and RO vs. W for fixed L=15um and IREF=100uA



RO vs VGS

Note: VGS is giving different RO at from Different LN WN values!

DC Response

