Process Documentation for 4-Mask NMOS Process

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Background

- This NMOS process is based on:
  - AL Gate
  - Non self aligned structure
- Covers most microelectronic manufacturing processes
  - Photolithography
  - Diffusion
  - Oxide Growth (Wet and Dry)
  - Etch
  - Metal deposition

About the Process

- Process Design
  - To be robust with positive VT
    - Thin oxide transistors
      - VT 1-2 volts depending on the fixed oxide charge
      - ~400-550Å thick gate oxide
    - Parasitic Field Oxide transistors
      - VT 15-18 volts depending on the fixed oxide charge
      - ~4000-5000Å thick gate oxide
    - Maximum tolerable registration error ±4μm
    - Can handle large power supply
    - No ESD protection

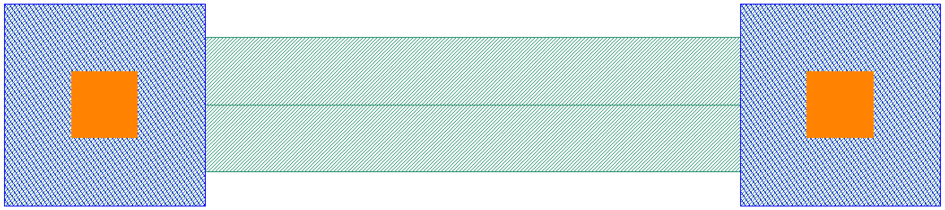
Other uses for the Process

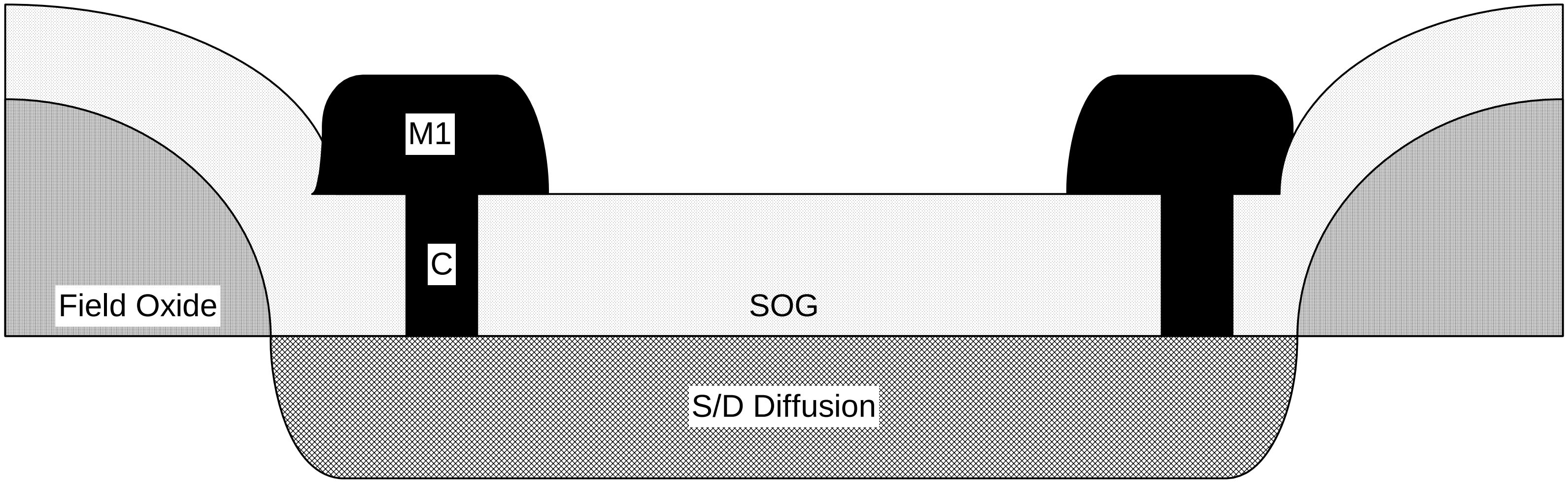
- To provide an environment where students can design fabricate and test ICs in one semester (EE122/124).
  - Utilize the existing EE/MatE129 lab
  - Real world device physics examples (EE128)
  - Statistical information can be shared (EE102, EE/MatE167)!
  - Can be used as a research/MEMS platform
- Can unify curriculum!
- See all aspects of a product design

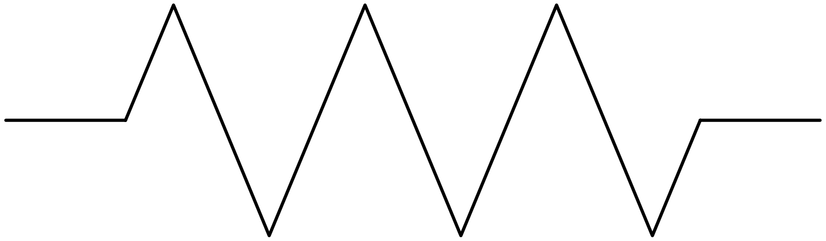
Semi Custom IC design

- The most expensive and time consuming layers are pre-processed
  - S/D diffusion, Gate oxide, contact, and metalization
- Circuits are made by wiring together the pre laid out transistors.
- One mask is made and PL done on wafers.
- Since the wafers are predone the turn around time is very short.
- Since the transistors are pre laid out design time is reduced!

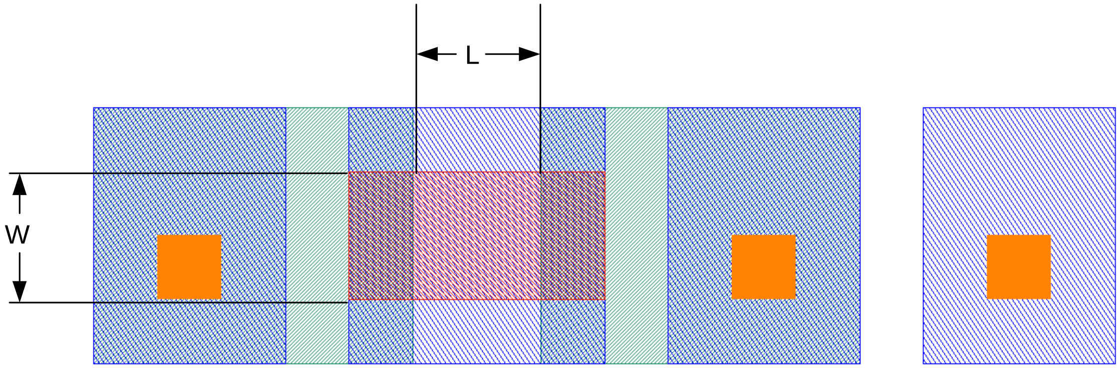
Resistor Pass-through

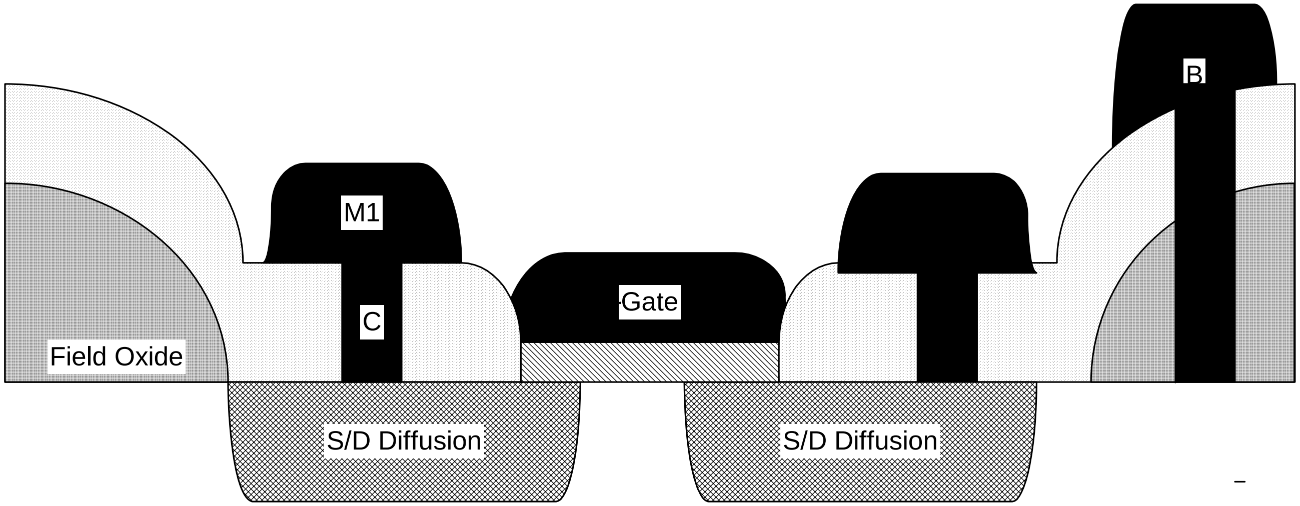


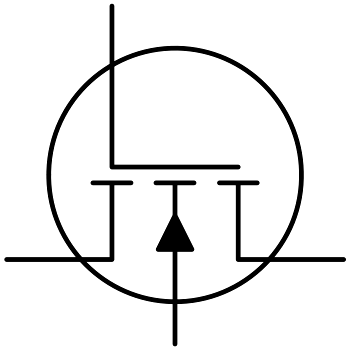




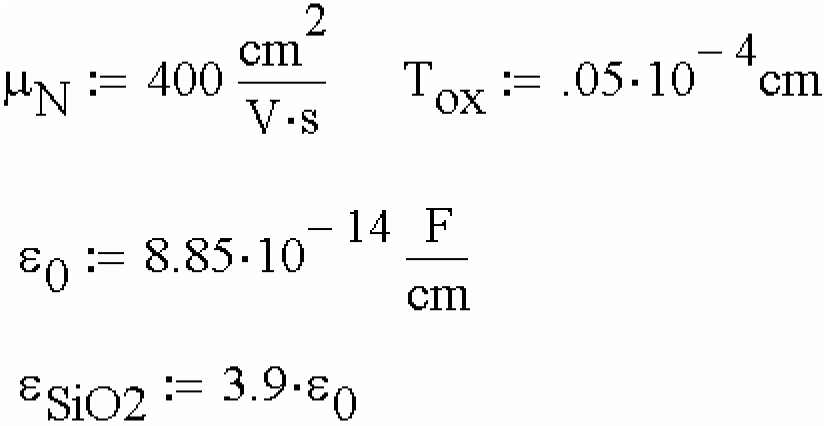
MOSFET







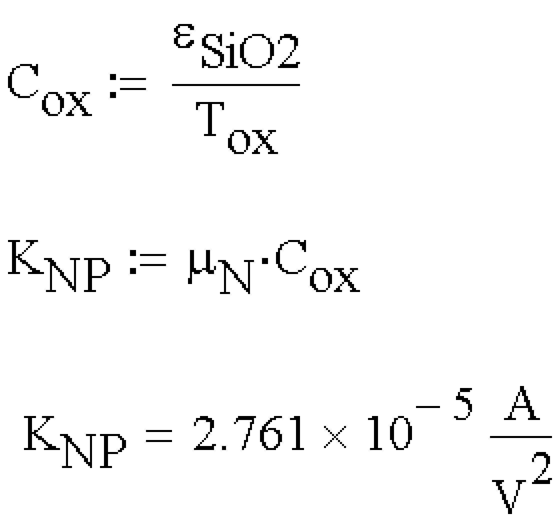
Modeling the MOSFET



$$\mu_N := 400\,\frac{\mathrm{cm}^2}{\mathrm{V}\cdot\mathrm{s}} \qquad T_{ox} := .05\cdot10^{-4}\mathrm{cm}$$

$$\varepsilon_0 := 8.85\cdot10^{-14}\,\frac{\mathrm{F}}{\mathrm{cm}}$$

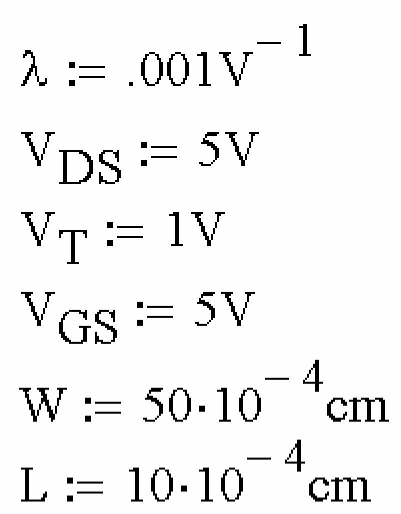
$$\varepsilon_{SiO2} := 3.9\cdot\varepsilon_0$$



$$C_{ox} := \frac{\varepsilon_{SiO2}}{T_{ox}}$$

$$K_{NP} := \mu_N\cdot C_{ox}$$

$$K_{NP} = 2.761\times10^{-5}\,\frac{\mathrm{A}}{\mathrm{V}^2}$$



$$\lambda := .001\mathrm{V}^{-1}$$

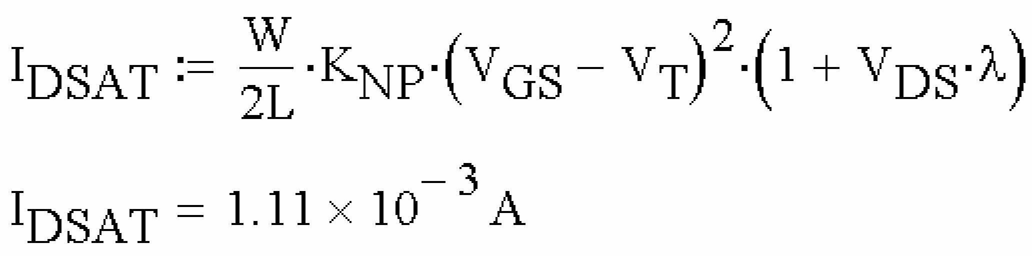
$$V_{DS} := 5\mathrm{V}$$

$$V_T := 1\mathrm{V}$$

$$V_{GS} := 5\mathrm{V}$$

$$W := 50\cdot10^{-4}\mathrm{cm}$$

$$L := 10\cdot10^{-4}\mathrm{cm}$$



$$I_{DSAT} := \frac{W}{2L}\cdot K_{NP}\cdot\left(V_{GS} - V_T\right)^2\cdot\left(1 + V_{DS}\cdot\lambda\right)$$

$$I_{DSAT} = 1.11\times10^{-3}\,\mathrm{A}$$

VT0

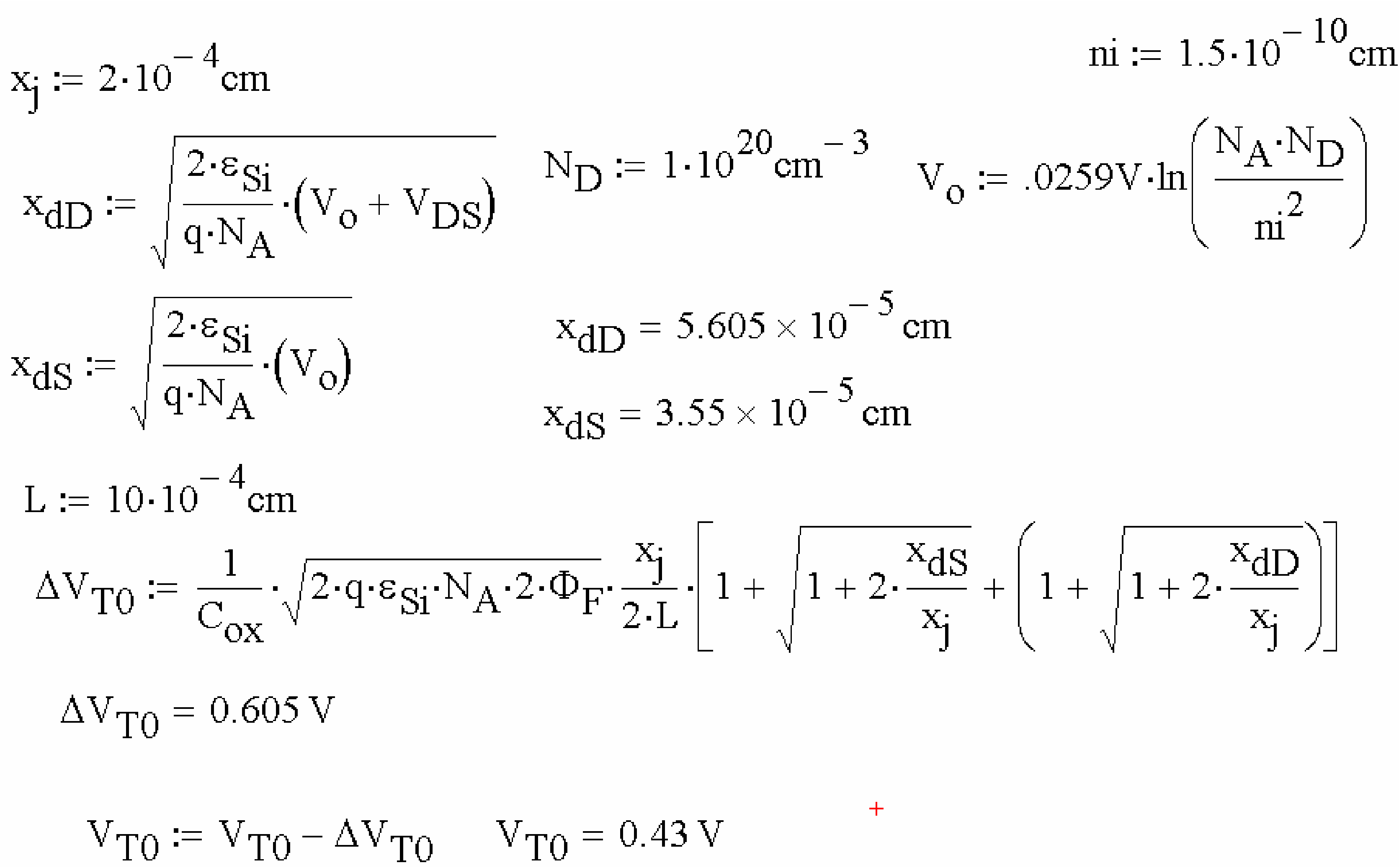
$$\phi_{ms} := -.6V - .0259V \cdot \ln\left(\frac{N_A}{n_i}\right) \quad Q_i := 5 \cdot 10^{10} \cdot \frac{q}{cm^2}$$

$$Q_D := -2 \cdot \left(\varepsilon_{Si} \cdot q \cdot N_A \cdot \Phi_F\right)^{\frac{1}{2}}$$

$$V_{T0} := \phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_D}{C_{ox}} + 2 \cdot \Phi_F$$

$$V_{T0} = 1.035\,V$$

VT short channel



$ni := 1.5\cdot 10^{-10}\,\mathrm{cm}^{-3}$

$x_j := 2\cdot 10^{-4}\,\mathrm{cm}$

$$x_{dD} := \sqrt{\frac{2\cdot\varepsilon_{Si}}{q\cdot N_A}\cdot\left(V_o + V_{DS}\right)} \qquad N_D := 1\cdot 10^{20}\,\mathrm{cm}^{-3} \qquad V_o := .0259V\cdot\ln\left(\frac{N_A\cdot N_D}{ni^2}\right)$$

$$x_{dS} := \sqrt{\frac{2\cdot\varepsilon_{Si}}{q\cdot N_A}\cdot\left(V_o\right)}$$

$x_{dD} = 5.605\times 10^{-5}\,\mathrm{cm}$

$x_{dS} = 3.55\times 10^{-5}\,\mathrm{cm}$

$L := 10\cdot 10^{-4}\,\mathrm{cm}$

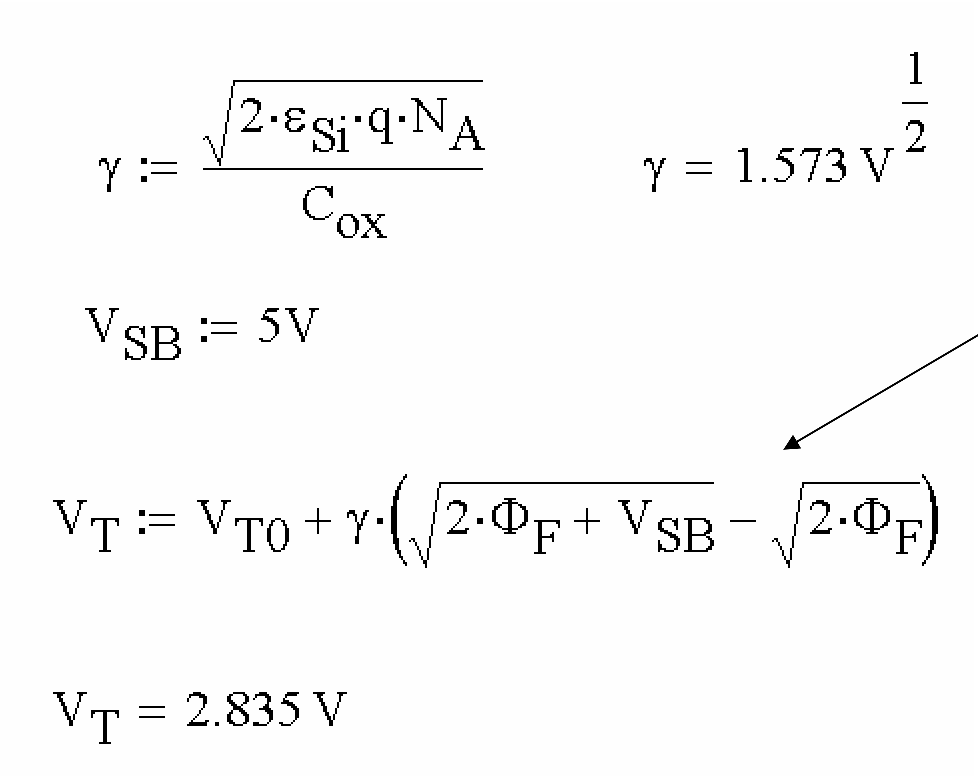
$$\Delta V_{T0} := \frac{1}{C_{ox}}\cdot\sqrt{2\cdot q\cdot\varepsilon_{Si}\cdot N_A\cdot 2\cdot\Phi_F}\cdot\frac{x_j}{2\cdot L}\cdot\left[1+\sqrt{1+2\cdot\frac{x_{dS}}{x_j}}+\left(1+\sqrt{1+2\cdot\frac{x_{dD}}{x_j}}\right)\right]$$

$\Delta V_{T0} = 0.605\,\mathrm{V}$

$V_{T0} := V_{T0} - \Delta V_{T0} \qquad V_{T0} = 0.43\,\mathrm{V}$

VT

- VT changes with VSB



$$\gamma := \frac{\sqrt{2 \cdot \varepsilon_{Si} \cdot q \cdot N_A}}{C_{ox}} \qquad \gamma = 1.573\,\mathrm{V}^{\frac{1}{2}}$$

$$V_{SB} := 5\mathrm{V}$$

$$V_T := V_{T0} + \gamma \cdot \left(\sqrt{2 \cdot \Phi_F + V_{SB}} - \sqrt{2 \cdot \Phi_F} \right)$$

$$V_T = 2.835\,\mathrm{V}$$

This will cause trouble later.

Mobility

- Mobility changes with electric field
  - The constant KNP, is never constant
  - We use an average

λ

- This is due to the channel length narrowing.
  - The reversed biased diode’s depletion region gets bigger with VDS, and thus the length of the channel gets smaller, and thus the ID goes up.

What does the circuit design engineer control?

- How big W and L are.
- How the wires are connected.
  - This does not sound like much is it is a lot.

What does the process design engineer control?

- Tox
- Na
- Junction Depth
- Qi (kind of)

Major Process Steps

- CLean1
- Screen Oxide
- Implant
- Well drive
- Field Oxide
- S/D PL and Etch
- SOG Deposition
- S/D Diffusion
- SOG Strip

Major Process Steps

- Gate PL, etch
- Gate Clean
- Gate Oxide
- Contact PL, etch and PR strip
- Metalize
- Metal PL, etch and strip
- Anneal
- Test

Clean 1

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Clean 1	**Estimated time=**	**61**	**minutes**				
1	Piranha	Bath Temp 110oC	H2SO4 (75%) + H2O2 (25%)	5	Use Diffusion CLean Bench	Use Proper PPE	
2	Dump Rinse			5			
3	BOE DIP	Bath Temp ~20oC	20:1 BOE	2	Use Diffusion CLean Bench	Use Proper PPE	
4	Dump Rinse			5			
5	Piranha	Bath Temp 110oC	H2SO4 (75%) + H2O2 (25%)	5	Use Diffusion CLean Bench	Use Proper PPE	
6	Dump Rinse			5			
7	BOE DIP	Bath Temp ~20oC	20:1 BOE	2	Use Diffusion CLean Bench	Use Proper PPE	
8	Dump Rinse			5			
9	RCA	Bath Temp 70oC	HCl:H2O2:H2O 1:1:6	10	Use Diffusion CLean Bench	Use Proper PPE	
10	Dump Rinse			5			
11	BOE DIP	Bath Temp ~20oC	20:1 BOE	2	Use Diffusion CLean Bench	Use Proper PPE	
12	Dump Rinse			5			
13	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
14	Take out Wafers	Turn off N2	Dot in, H out	0			

Clean 1

- Piranha
  - removes organics and grows a thin layer of oxide around particles on the surface of the wafer
- BOE
  - removes oxide and the particles that were trapped
- RCA
  - Remove light metal ions

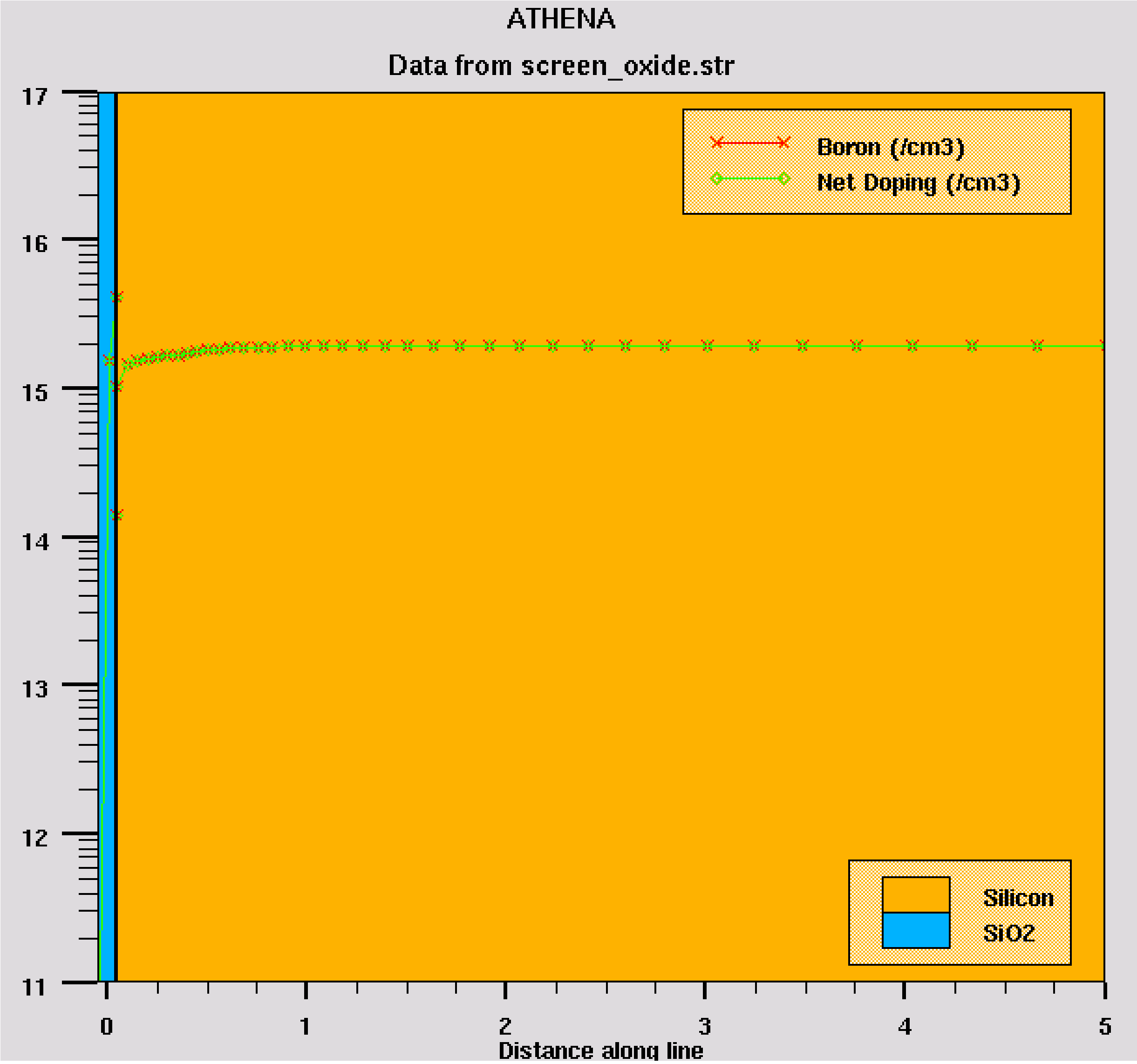
Screen Oxide

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Screen Oxide	**Estimated time=**	**115**	**minutes**				
1	Load	900oC	N2:4SLM	10	Shiny side of wafer facing into furnace, every other slot, order, 2 dummies-5 device-2 dummies	Push Quartz boat until last wafer is past ceramic ring.	
2	Push	900oC	N2:4SLM	15	Use quartz rod		
3	Ramp	900oC to 1100oC	N2:4SLM	15	Cap on, Restrictor on, Door open		
4	Stabilize	1100oC	N2:4SLM	5	Cap on, Restrictor on, Door open		
5	Soak	1100oC	O2:10SLM	30	Cap on, Restrictor on, Door open		
6	Purge	1100oC	N2:10SLM	10	Cap on, Restrictor on, Door open		
7	Pull	1100oC	N2:4SLM	20	Use quartz rod		
8	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows	Ramp furnace back down	

Screen Oxide

- Scatters the implanted ions so they are more evenly distributed in the wafer

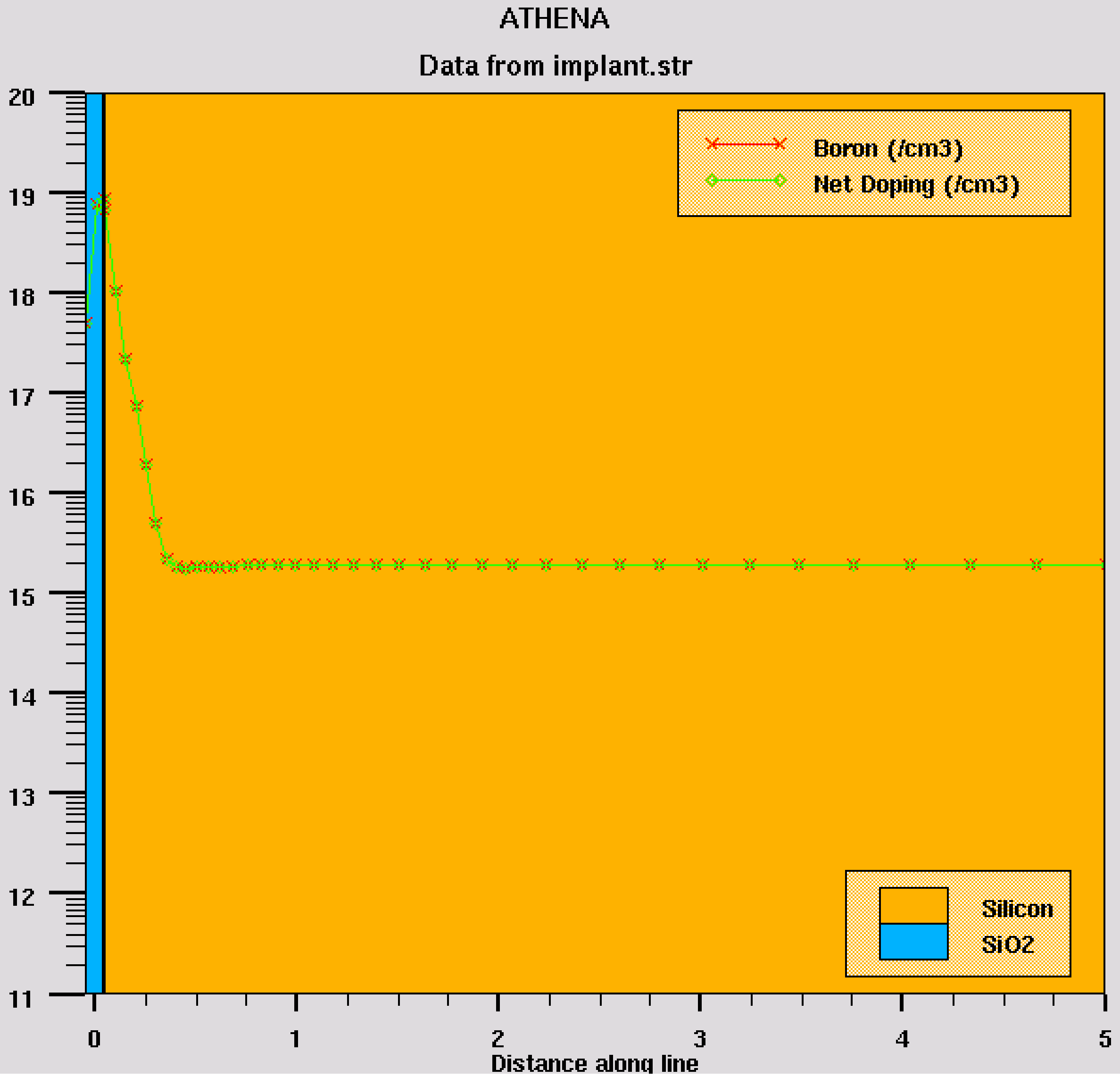
Screen Oxide



Implant

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
PWELL Implant	**Estimated time=**	**15**	**minutes**				
1	Inspect	Blue color		10			
2	Implant (Inovian)	Species=B11	E=100keV	5	dose=8e13	Tilt=7	

Implant


ATHENA
Data from implant.str
20
19
18
17
16
15
14
13
12
11
0
1
2
3
4
5
Distance along line
Boron (/cm3)
Net Doping (/cm3)
Silicon
SiO2

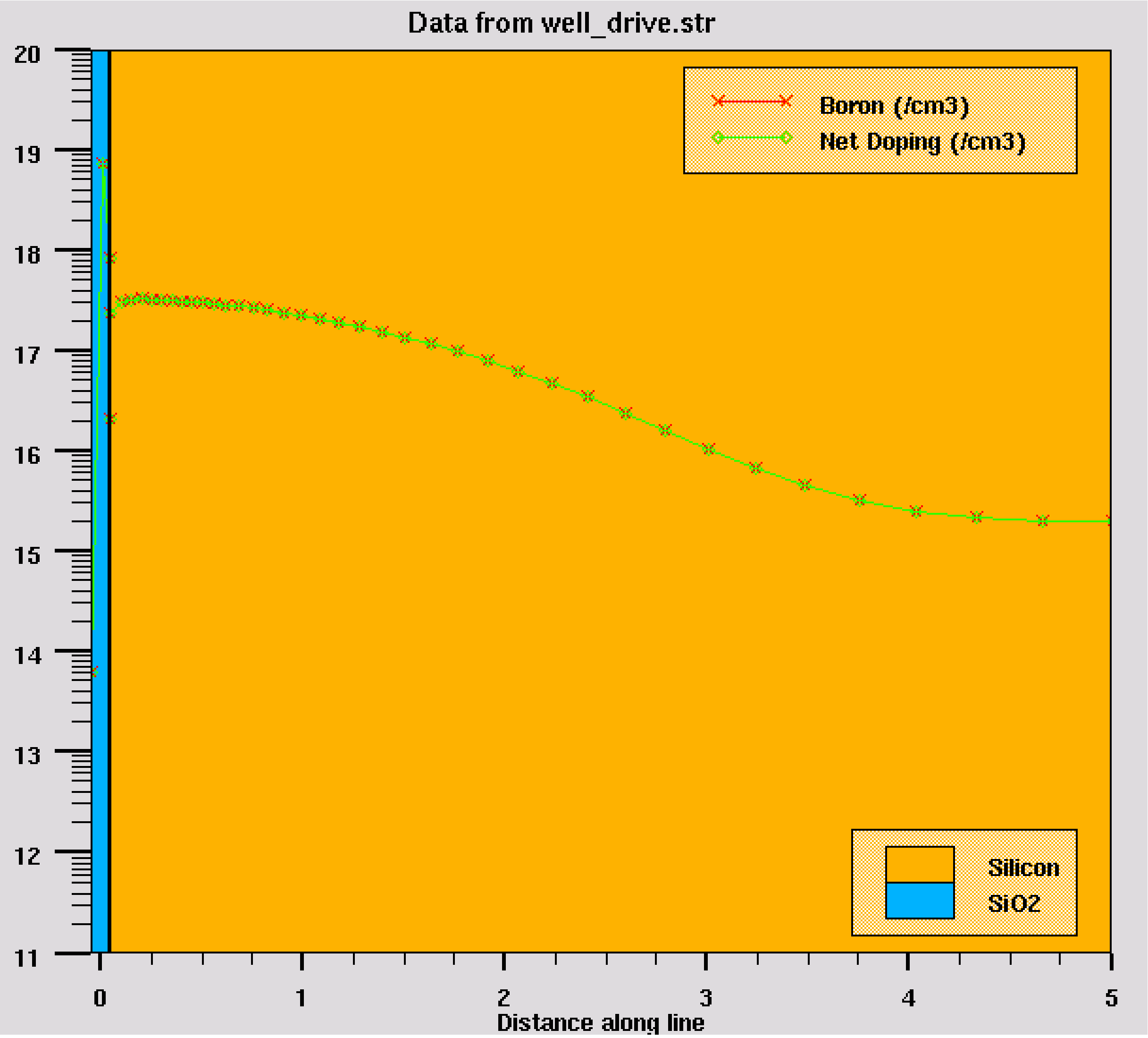
Well Drive

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Well Drive	**Estimated time=**	**310**	**minutes**				
1	Load	900oC	N2:4SLM	10	Shiny side of wafer facing into furnace, every other slot, order, 2 dummies-5 device-2 dummies	Push Quartz boat until last wafer is past ceramic ring.	
2	Push	900oC	N2:4SLM	15	Use quartz rod		
3	Ramp	900oC to 1100oC	N2:4SLM	15	Cap on, Restrictor on, Door open		
4	Soak	1100oC	N2:4SLM	240	Cap on, Restrictor on, Door open		
5	Pull	1100oC	N2:4SLM	20	Use quartz rod		
6	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows	Ramp furnace back down	

Well Drive

- Brings the surface concentration of the boron down to values that will produce positive VT.

Well Drive


Data from well_drive.str
20
19
18
17
16
15
14
13
12
11
0
1
2
3
4
5
Distance along line
Boron (/cm3)
Net Doping (/cm3)
Silicon
SiO2

Pre Oxide Oxide

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Pre OXIDE CLEAN	**Estimated time=**	**10**					
	Bath Temp 110oC	H_2SO_4 (75%) + H_2O_2 (25%)	5	Use Diffusion CLean Bench	Use Proper PPE		0
			5				0

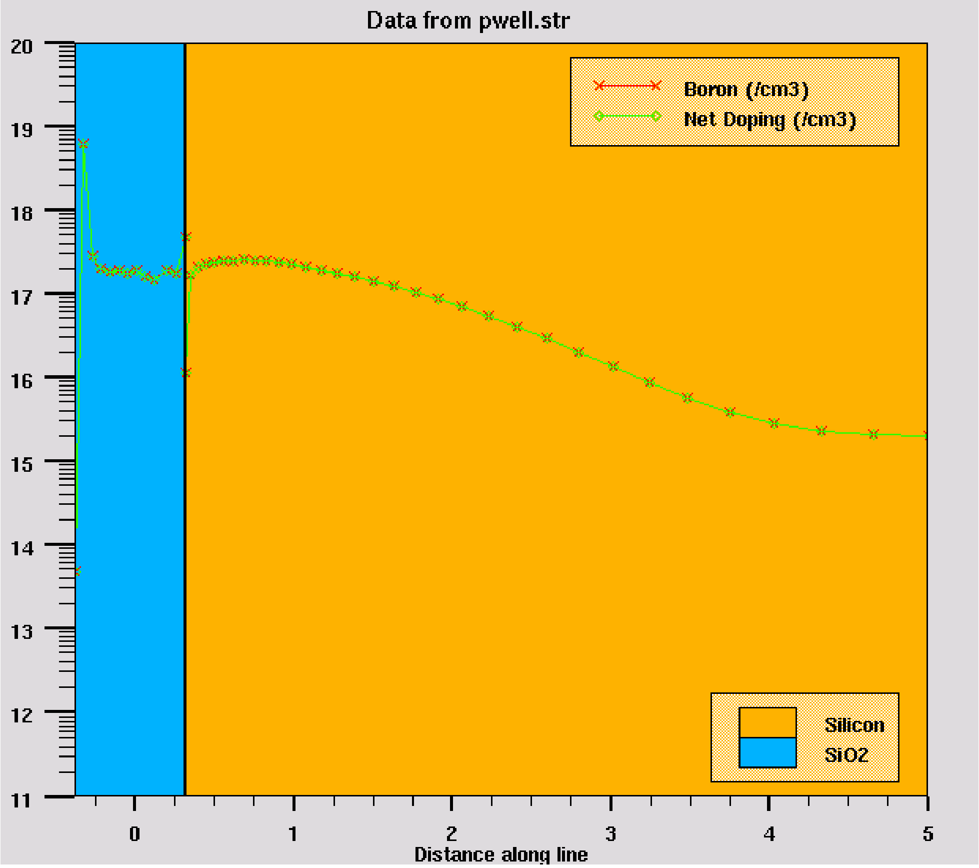
Pre Oxide Clean

- Removes any organics that were put on the wafer during handling.

Field Oxidation

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Field Oxide	**Estimated time=**	**115**	**minutes**				
1	Load	900oC	N2:4SLM	10	Shiny side of wafer facing into furnace, every other slot, order, 2 dummies-5 device-2 dummies	Push Quartz boat until last wafer is past ceramic ring.	
2	Push	900oC	N2:4SLM	15	Use quartz rod		
3	Ramp	900oC to 1100oC	N2:4SLM	15	Cap on, Restrictor on, Door open		
4	Stabilize	1100oC	N2:4SLM	5	Cap on, Restrictor on, Door open		
5	Soak	1100oC	4SLM Wet	60	Cap on, Restrictor on, Door open	7mL HCL at T=95°C (#8)Ensure N2 is flowing if light is on and H2O is boiling	
6	Purge	1100oC	N2:10SLM	10	Cap on, Restrictor on, Door open		
7	Pull	1100oC	N2:4SLM	20	Use quartz rod		
8	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows	Ramp furnace back down	
9	Inpsect	Measure Oxide Thickness	Should be over 4000A	10	Nanop SPec or Filmetrcs	5 points per wafer	

Field Oxidation



Field Oxide

- Acts a a diffusion mask to phosphorous doping.
- Creates thick oxides (and thus large VT) for parasitic field oxide transistors.

S/D Mask 1 PL

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 1 S/D PL	**Estimated time=**	**4.5**	**minutes**				
1	Singe	125oC	Air	1	Eric's Hotplate	Vacuum on	
2	Prime	3000 rmp	HMDS Prime	0.5	Use manual dispenser		
3	Spin PR	3000 rmp	Shipley	1	Use manual dispenser	Use automatic or Loral	
4	Pre-Bake	110oC	AIR	1			
5	Expose	XXmJ	Verify with dummy	?			
6	Post Expose Bake	110oC	AIR	1			
7	Develop	Room	Developer recipe	0.5		1.75% TMHA in DI (Use automatic developer or bucket)	
8	Hard Bake	120oC	AIR	1	hotplate	This is automatic if using the auto developer	
9	Inspect			10		Inspect wafers for alignment and quality. Redo if necessary (Error exceeds 4um)	

S/D Mask 1 PL

- Defines a window for the phosphorous dopant to diffuse into creating and N+/P junction

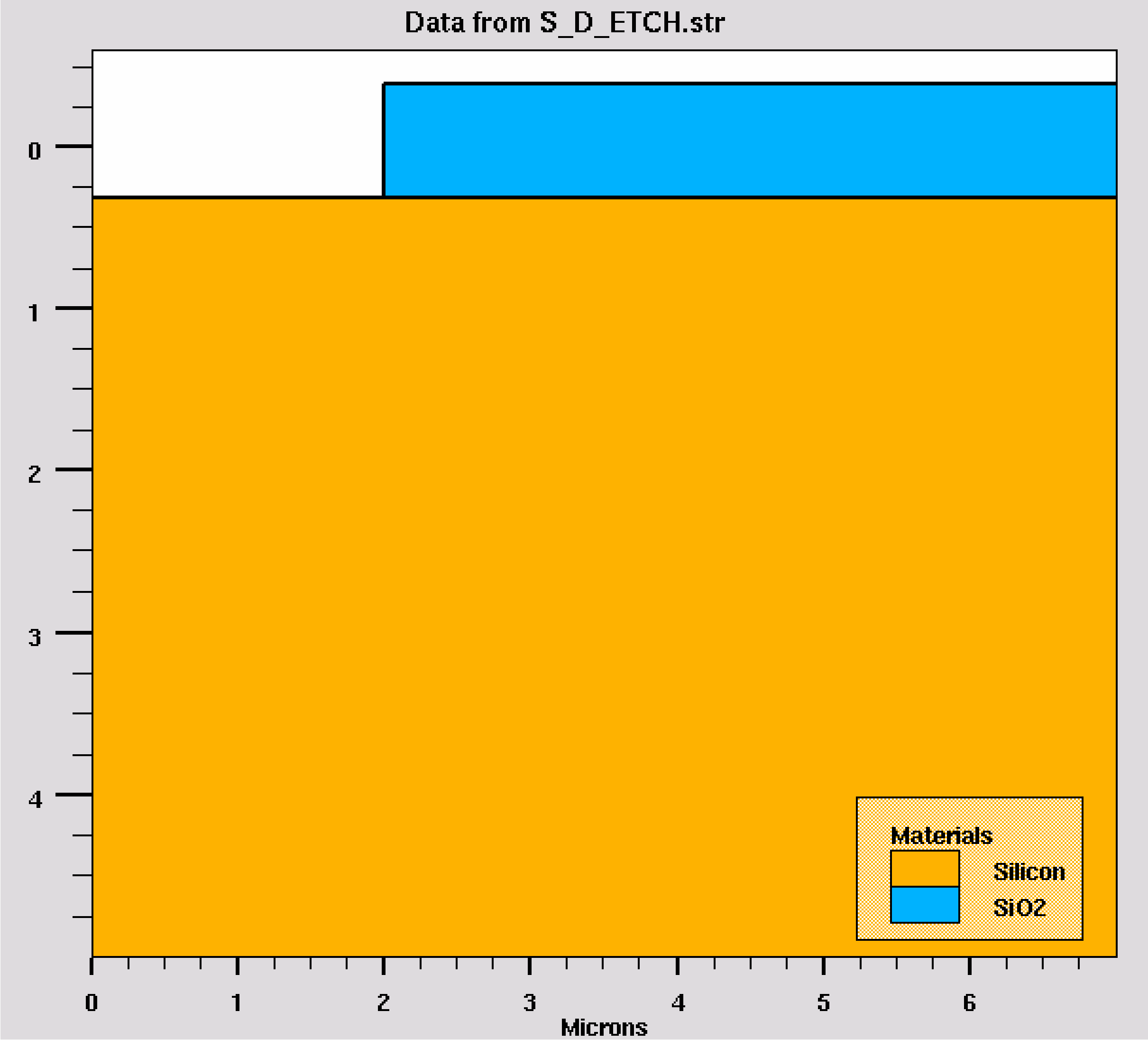
S/D Etch

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 1 S/D Etch	**Estimated time=**	**60**	**minutes**				
1	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thick setting on nano spec		
2	BOE ETCH	Bath Temp ~20oC	20:1 BOE	30	Use Etch Bench	Use Proper PPE	
3	Dump Rinse			5			
4	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
5	Take out Wafers	Turn off N2	Dot in, H out	0			
6	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thin setting on nano spec	Measuremeant must read below 20A, If not repeat etch for 5 minutes.	

S/D Etch

- Opens a window for the phosphorous SOG so we get selective N+ regions.

Source Drain Etch



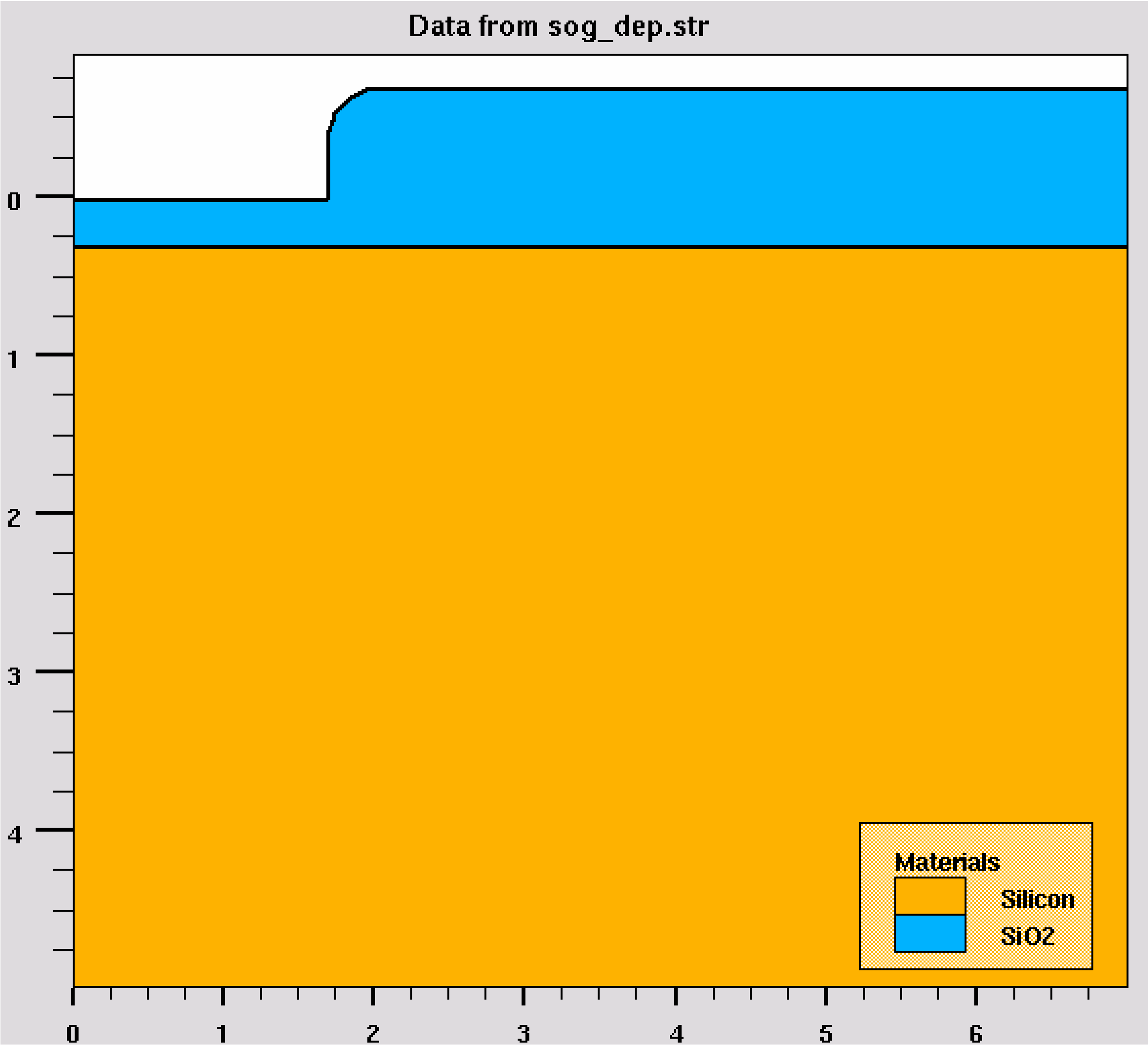
P SOG Deposition

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
P SOG Deposition	**Estimated time=**	**15.5**	**minutes**				
1	Piranha	Bath Temp 110oC	H_2SO_4 (75%) + H_2O_2 (25%)	5	Use Diffusion CLean Bench	Use Proper PPE	
2	Inpsect	Make sure PR is gone	Make sure fresh chemicals are used.				
3	Dump Rinse			5			
4	Spin Rinse Dry	Turn on N_2		5	Use correct SRD		
5	Take out Wafers	Turn off N_2	Dot in, H out	0			
6	Spin on P-SOG	5X1020 phosphorus	RPM’s = 3000 for 15 sec	0.5	Quantity SOG = 3 ml		
7	Bake	hotplate	110oC	1			

P SOG Deposition

- This layer contains the phosphorous dopant to make the source and drains of the transistors.

P SOG Deposition



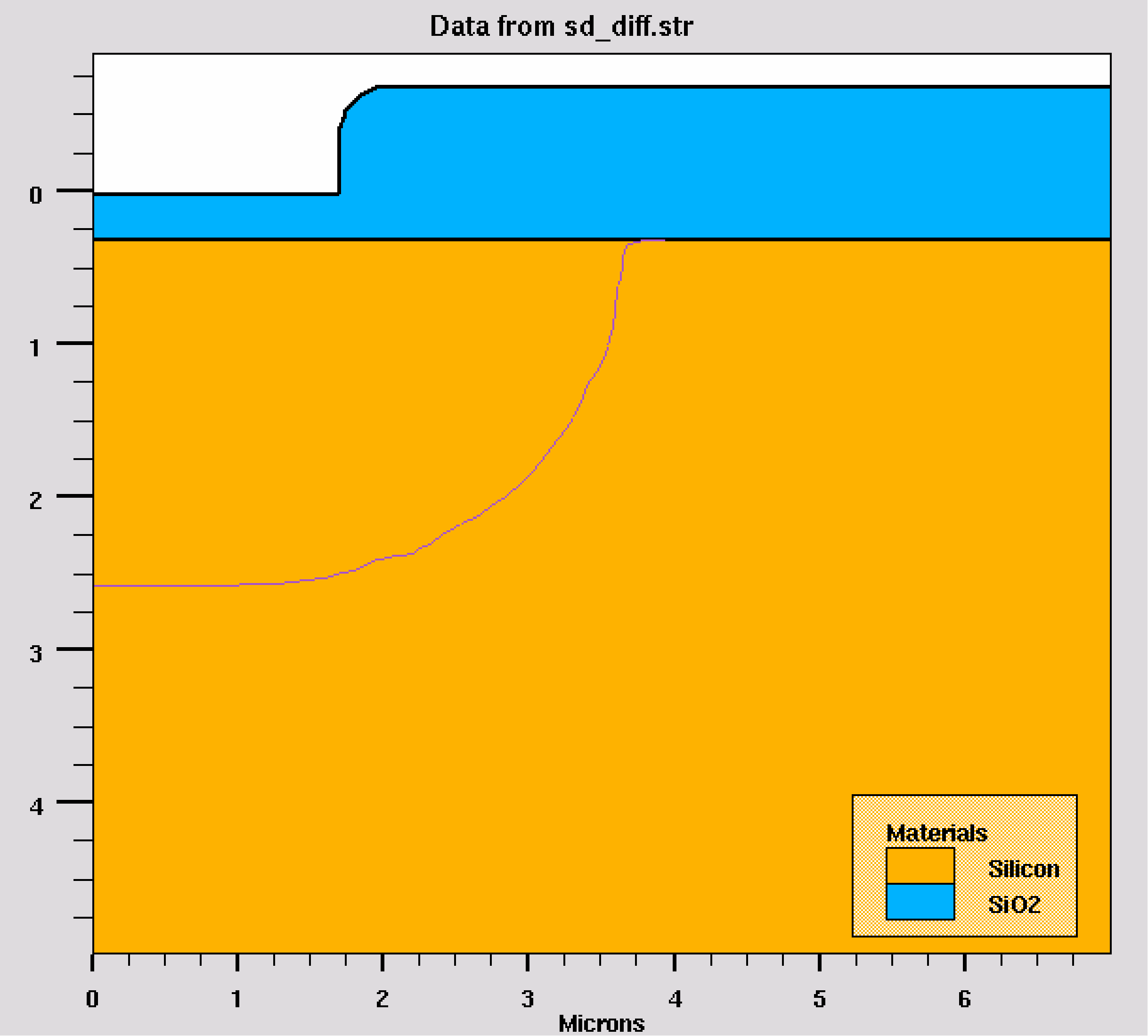
S/D Diffusion

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
S/D Diffusion	**Estimated time=**	**125**	**minutes**				
1	Load	900oC	N2:4SLM, O2:2SLM	10	Shiny side of each wafer facing each other, every other slot	Push Quartz boat until last wafer is past ceramic ring. Face active sides of wafers together., at least two dummies on other end of wafers	
2	Push	900oC	N2:4SLM, O2:2SLM	15	Use quartz rod		
3	Ramp	900oC to 1100oC	N2:4SLM, O2:2SLM	15	Cap on, Restrictor on, Door open		
4	Stabilize	1100oC	N2:4SLM, O2:2SLM	5	Cap on, Restrictor on, Door open		
5	Soak	1100oC	N2:4SLM, O2:2SLM	60	Cap on, Restrictor on, Door open		
6	Pull	1100oC	N2:4SLM, O2:2SLM	20	Use quartz rod		
7	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows	Ramp furnace back down	

S/D P Diffusion

- The dopant will not diffuse into the silicon in our lifetime if we do not raise the temperature.
- The high Tempe true raise the surface concentration of the N+ region so we can make low resistance ohmic contacts.

S/D Diffusion



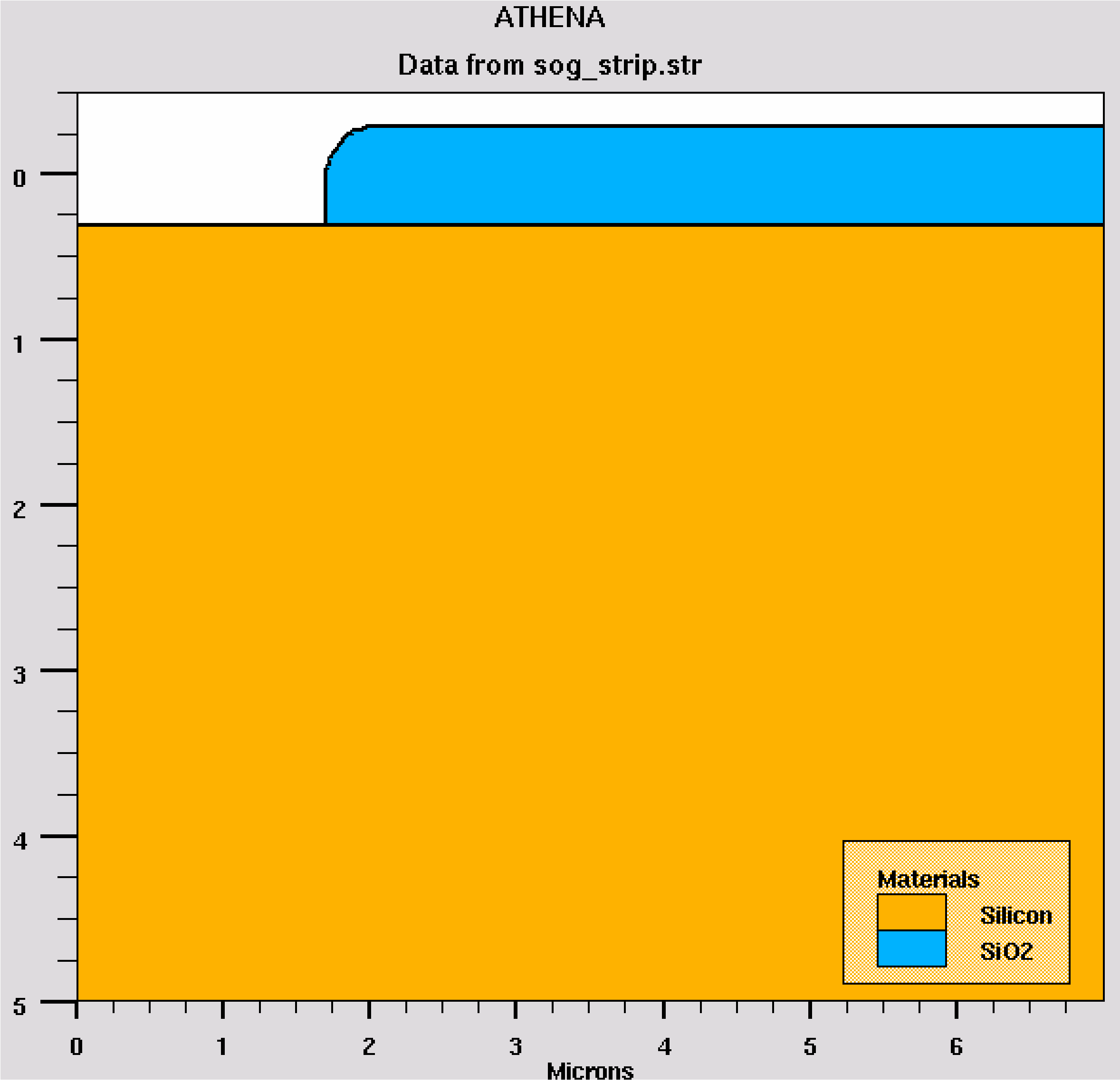
SOG Strip

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
SOG STRIP	**Estimated time=**	**12**	**minutes**				
1	BOE DIP	Bath Temp ~20oC	20:1 BOE	2	Use Diffusion CLean Bench	Use Proper PPE	
2	Dump Rinse			5			
3	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
4	Take out Wafers	Turn off N2	Dot in, H out	0			
5	Measure Oxide Thickness	Do not meaure in S/D holes	Just Measure the Fieild Oxide	0	Just Make sure SOG is gone from Field Area	You can etch down to 4000A and be ok.	0

SOG Strip

- The SOG acts like an oxide with a a fixed oxide charge that will make the VT of the filed oxide transistors to be –100Volts.
- These field oxide transistor surround the thin gate transistor and make them appear normally on .
- We strip it off to prevent this.

P SOG Strip


ATHENA
Data from sog_strip.str
0
1
2
3
4
5
0
1
2
3
4
5
6
Microns
Materials
Silicon
SiO2

Gate PL

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 2 Gate PL	**Estimated time=**	**16**	**minutes**				
1	Singe	125oC	Air	1	Eric's Hotplate	Vacuum on	
2	Prime	3000 rmp	HMDS Prime	0.5	Use manual dispenser		
3	Spin PR	3000 rmp	Shipley	1	Use manual dispenser	Use automatic or Loral	
4	Pre-Bake	110oC	AIR	1			
5	Expose	XXmJ	Verify with dummy	?			
6	Post Expose Bake	110oC	AIR	1			
7	Develop	Room	Developer recipe	0.5		1.75% TMHA in DI (Use automatic developer or bucket)	
8	Hard Bake	120oC	AIR	1	hotplate	This is automatic if using the auto developer	
9	Inspect			10		Inspect wafers for alignment and quality. Redo if necessary (Error exceeds 4um)	

Gate PL

- Defines the pattern where the Gates will be.

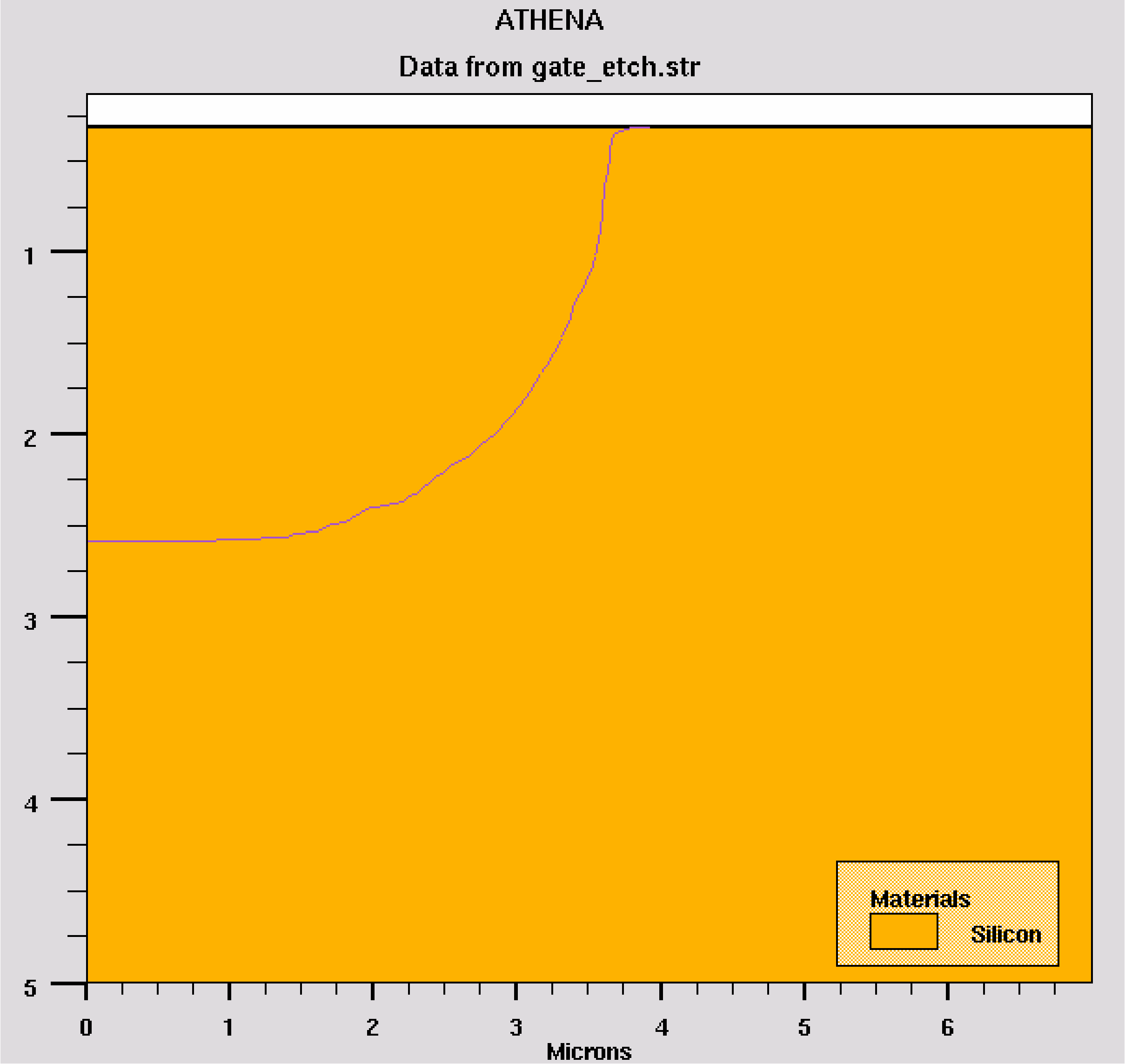
Gate Etch

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 2 Gate Etch	**Estimated time=**	**60**	**minutes**				
1	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thick setting on nano spec		
2	BOE ETCH	Bath Temp ~20oC	20:1 BOE	30	Use Etch Bench	Use Proper PPE	
3	Dump Rinse			5			
4	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
5	Take out Wafers	Turn off N2	Dot in, H out	0			
6	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thin setting on nano spec	Measuremeant must read below 20A, If not repeat etch for 5 minutes.	

Gate Etch

- Remove the field oxide so we can grow thin gate oxide for our transistors.

Gate Etch


ATHENA
Data from gate_etch.str
1
2
3
4
5
0
1
2
3
4
5
6
Microns
Materials
Silicon

Gate Clean

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Gate Clean	**Estimated time=**	**55**	**minutes**				
1	Piranha	Bath Temp 110oC	H2SO4 (75%) + H2O2 (25%)	5	Use Etch Bench	Use Proper PPE	
2	Dump Rinse			5	Make sure PR is removed		
3	BOE DIP	Bath Temp ~20oC	20:1 BOE	5 sec max	Use Difusion CLean Bench	Use Proper PPE	
4	Dump Rinse			5			
5	Piranha	Bath Temp 110oC	H2SO4 (75%) + H2O2 (25%)	5	0	Use Proper PPE	
6	Dump Rinse			5	Make sure PR is removed		
7	BOE DIP	Bath Temp ~20oC	20:1 BOE	5 sec max	Use Difusion CLean Bench	Use Proper PPE	
8	Dump Rinse			5			
9	RCA	Bath Temp 70oC	HCl:H2O2:H2O 1:1:6	10	Use Diffusion CLean Bench	Use Proper PPE	
10	Dump Rinse			5			
11	BOE DIP	Bath Temp ~20oC	20:1 BOE	5 sec max	Use Diffusion CLean Bench	Use Proper PPE	
12	Dump Rinse			5			
13	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
14	Take out Wafers	Turn off N2	Dot in, H out	0			

Gate Clean

- Piranha
  - removes organics and grows a thin layer of oxide around particles on the surface of the wafer
- BOE
  - removes oxide and the particles that were trapped
- RCA
  - Removes light metal ions

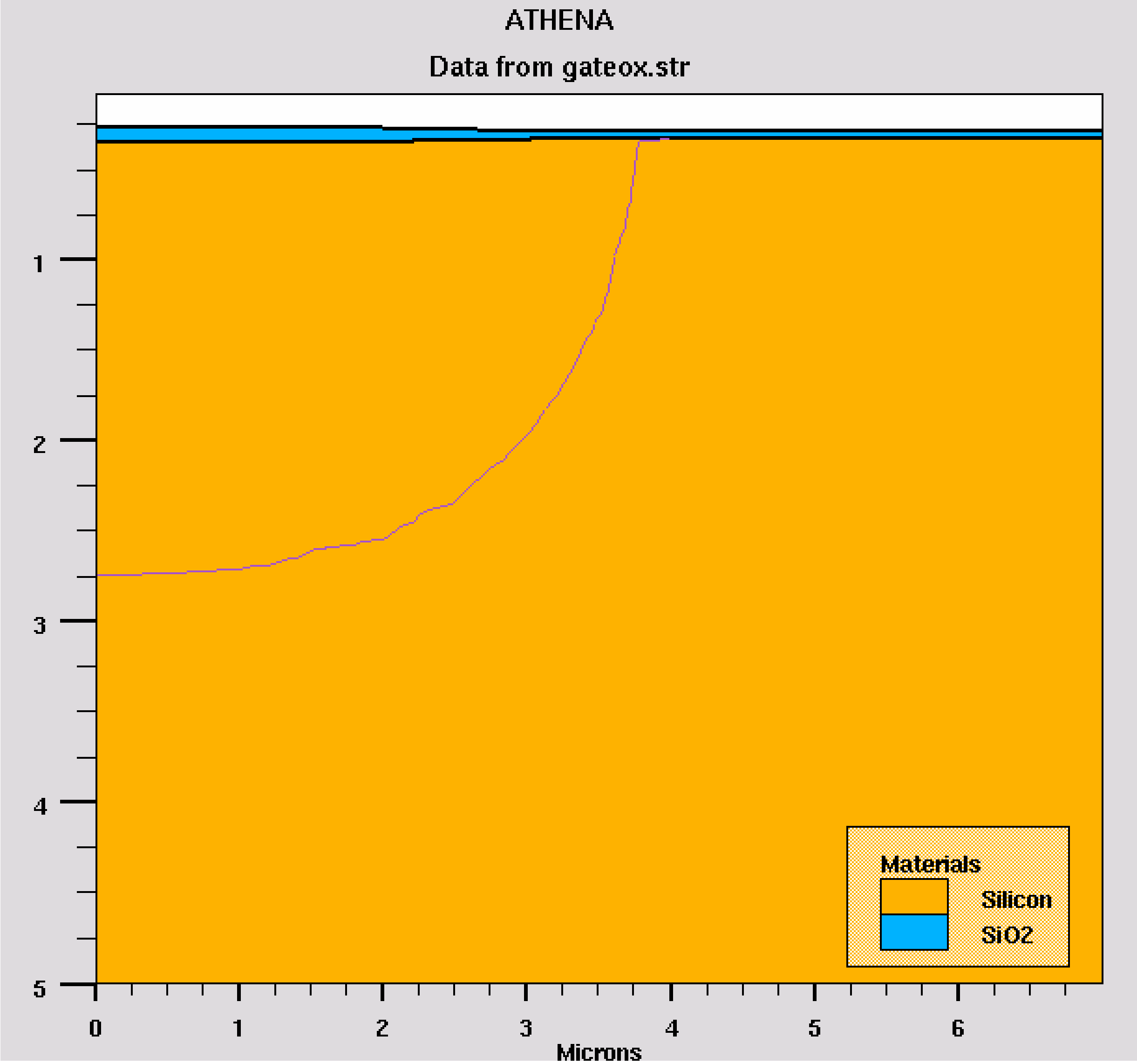
Gate Oxide

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Gate Oxide	**Estimated time=**	**175**	**minutes**				
1	Load	700oC	N2:4SLM	10	Shiny side of wafer facing into furnace, every other slot, order, 2 dummies-5 device-2 dummies	Push Quartz boat until last wafer is past ceramic ring.	
2	Push	700oC	N2:4SLM	15	Use quartz rod		
3	Ramp	700oC to 1000oC	N2:4SLM	15	Cap on, Restrictor on, Door open		
4	Stabilize	1000oC	N2:4SLM	5	Cap on, Restrictor on, Door open	Make sure funrace was properly cleaned day before (wet ox with 150ml HCl into 3L DI)	
5	Soak	1000oC	02:10SLM	45	Cap on, Restrictor on, Door open	7mL HCL at T=95°C (#8)Ensure N2 is flowing if light is on and H2O is boiling	
6	Post Oxide Anneal	1000oC	N2:10SLM	45	Cap on, Restrictor on, Door open		
7	Pull	1000oC	N2:4SLM	20	Use quartz rod		
8	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows	Ramp furnace back down	
9	Inpsect	Measure Gate Oxide Thickness	Should be around 500A	10	Nanop SPec	5 points per wafer	

Gate Oxide

- 700 C push in temp prevents oxide growth during ramp up.
- Dry oxidation make a low fixed oxide charge and dense oxide that can withstand large voltages and not leak or punch through.
- Post oxide anneal reduces fixed oxide charge.

Gate Oxide Growth



Contact PL

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 3 Conact PL	**Estimated time=**	**16**	**minutes**				
1	Singe	125oC	Air	1	Eric's Hotplate	Vacuum on	
2	Prime	3000 rmp	HMDS Prime	0.5	Use manual dispenser		
3	Spin PR	3000 rmp	Shipley	1	Use manual dispenser	Use automatic or Loral	
4	Pre-Bake	110oC	AIR	1			
5	Expose	XXmJ	Verify with dummy	?			
6	Post Expose Bake	110oC	AIR	1			
7	Develop	Room	Developer recipe	0.5		1.75% TMHA in DI (Use automatic developer or bucket)	
8	Hard Bake	120oC	AIR	1	hotplate	This is automatic if using the auto developer	
9	Inspect			10		Inspect wafers for alignment and quality. Redo if necessary (Error exceeds 4um)	

Contact PL

- Defines the pattern where the contacts will be.

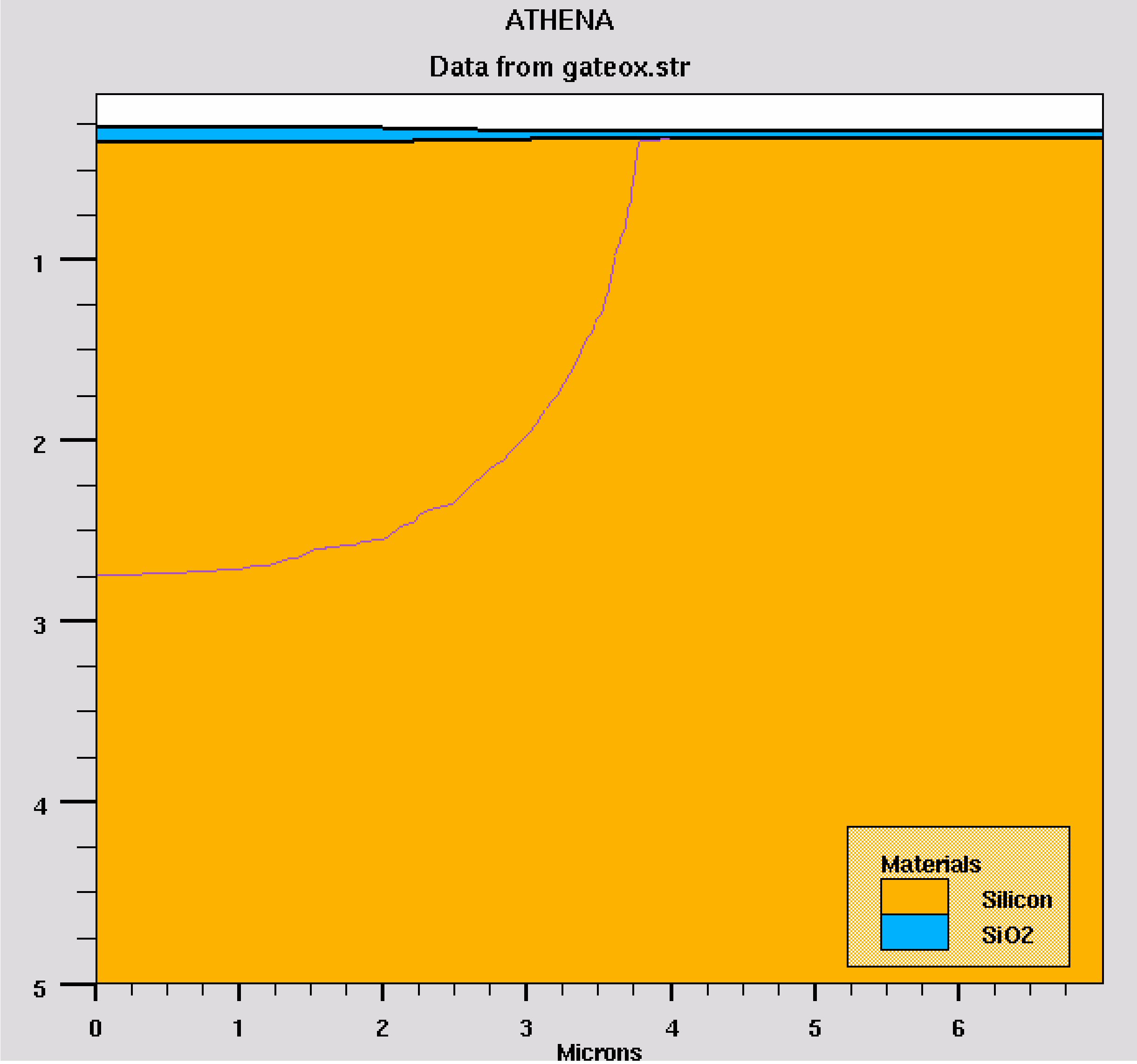
Contact Etch

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 3 Contact Etch	**Estimated time=**	**60**	**minutes**				
1	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thick setting on nano spec		
2	BOE ETCH	Bath Temp ~20oC	20:1 BOE	30	Use Etch Bench	Use Proper PPE	
3	Dump Rinse			5			
4	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
5	Take out Wafers	Turn off N2	Dot in, H out	0			
6	Measure Oxide thickness	Use Nano Spec	Use freshly BOE etched wafer to calibrate	10	Use thin setting on nano spec	Measuremeant must read below 20A, If not repeat etch for 5 minutes.	

Contact Etch

- Removes the field oxide so we can contact the S/Ds and bodys of our transistors.

Contact Etch



PR Strip

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 3 PR Strip	**Estimated time=**	**20**	**minutes**				
1	Piranha	Bath Temp 110oC	H2SO4 (75%) + H2O2 (25%)	5	Use Etch Bench	Use Proper PPE	
2	Dump Rinse			5	Make sure PR is removed		
3	BOE DIP	Bath Temp ~20oC	20:1 BOE	5 sec max	Use Difusion CLean Bench	Use Proper PPE	
4	Dump Rinse			5			
5	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
6	Take out Wafers	Turn off N2	Dot in, H out	0			

PR Strip

- Removes photo resist

Metalize

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Metalize	**Estimated time=**	**122.5**	**minutes**				
1	Evaporate 1	Follow Proceedure		60			
2	Evaporate 2	Follow Proceedure		60			

Metalize

- Two runs for a uniform thickness
- AL is the gate
- Al is used to connect transistors into circuits.

Metal PR

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 4 Metal PL	**Estimated time=**	**4.5**	**minutes**				
1	Singe	125oC	Air	1	Eric's Hotplate	Vacuum on	
2	Prime	3000 rmp	HMDS Prime	0.5	Use manual dispenser		
3	Spin PR	3000 rmp	Shipley	1	Use manual dispenser	Use automatic or Loral	
4	Pre-Bake	110oC	AIR	1			
5	Expose	XXmJ	Verify with dummy	?			
6	Post Expose Bake	110oC	AIR	1			
7	Develop	Room	Developer recipe	0.5		1.75% TMHA in DI (Use automatic developer or bucket)	
8	Hard Bake	120oC	AIR	1	hotplate	This is automatic if using the auto developer	
9	Inspect			10		Inspect wafers for alignment and quality. Redo if necessary (Error exceeds 4um)	

Metal PL

- Defines the pattern where the metal won’t be.

Metal Etch

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 4 Metal Etch	**Estimated time=**	**15**	**minutes**				
1	AL Etch	Bath Temp 60oC	AL Etch FRESH ETCH	5	Use Etch CLean Bench	Use Proper PPE	
2	Dump Rinse			5			
3	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
4	Take out Wafers	Turn off N2	Dot in, H out	0			

Metal Etch

- Removes unwanted metal.

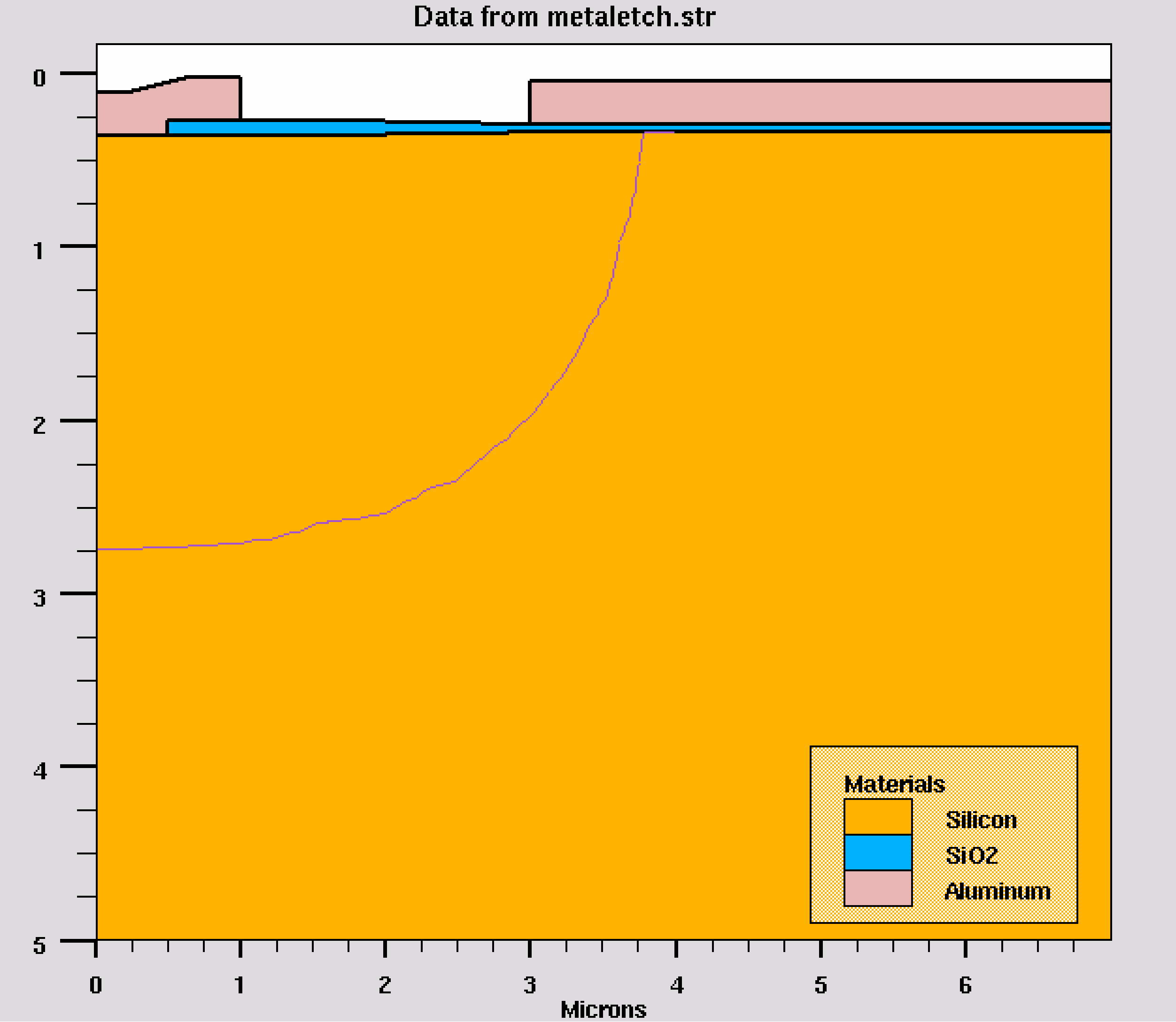
Strip PR

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Mask 4 PR Strip	**Estimated time=**	**20**	**minutes**				
1	Stripper	Bath Temp 60oC	microstrip 2001 Stripper	10	Stripper Bench	Use Proper PPE	
2	Dump Rinse			5	Make sure PR is removed		
3	Spin Rinse Dry	Turn on N2		5	Use correct SRD		
4	Take out Wafers	Turn off N2	Dot in, H out	0			

Strip PR

- Use Solvent!
  - Piranha will etch away the Al!
- Impossible to take of Al after anneal
  - Don’t ask, but it has happened.

Metalize and Etch



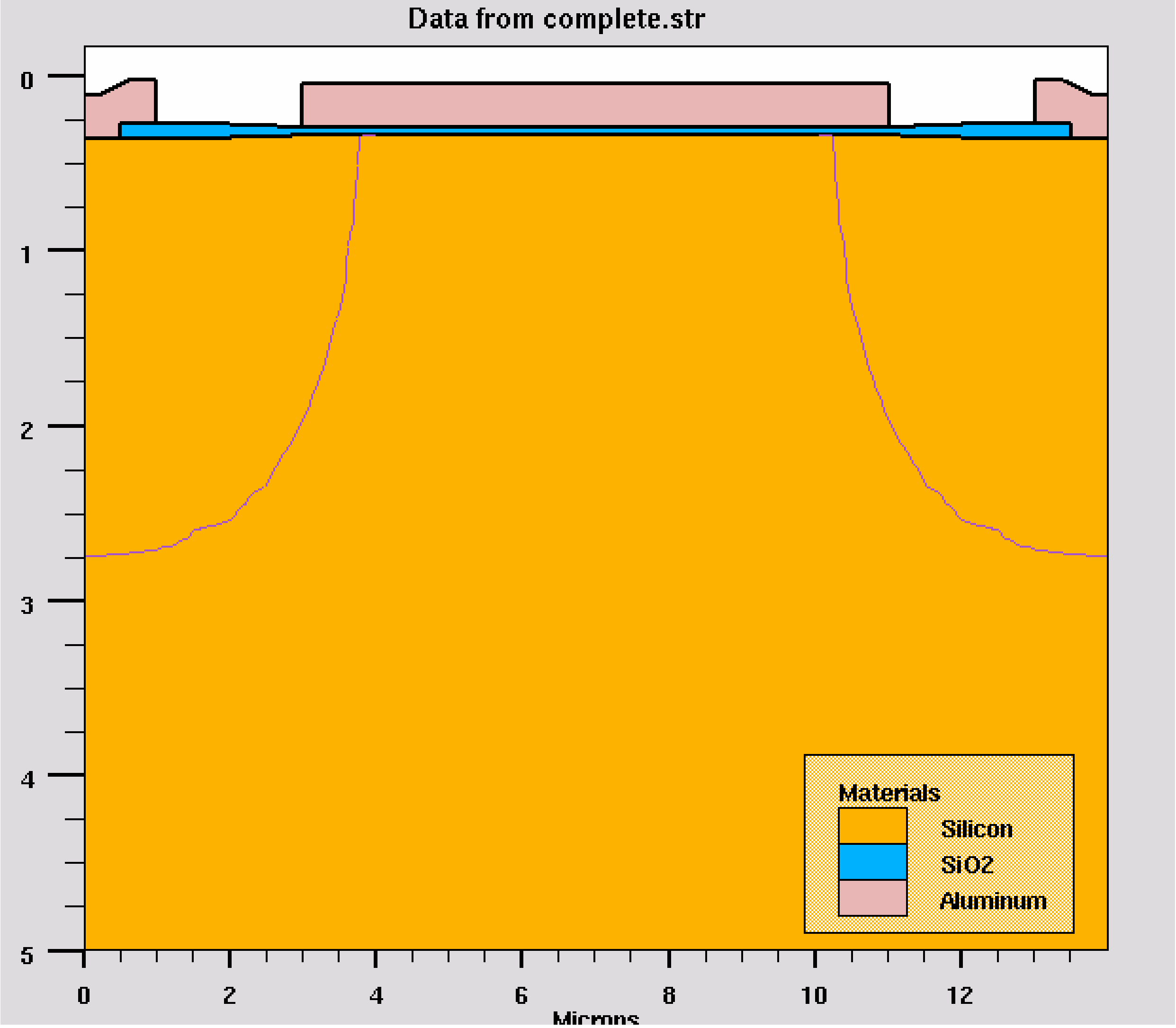
Anneal

Step	Step Name	Process Detail 1	Process Detail 2	Time	Process Detail 3	Process Detail 4	DATE & Operator intial
Anneal	**Estimated time=**	**56**	**minutes**				
1	Load	450oC	90N2:10H2	5	every other slot	Push Quartz boat until last wafer is past ceramic ring.	
2	Push	450oC	90N2:10H3	6	Use quartz rod		
3	Soak	450oC	90N2:10H4	30	Cap on,		
4	Pull	450oC	90N2:10H5	5	Use quartz rod		
5	Cool	Room Temp	Transfer wafers to cool quartz boats	10	Turn of gas flows		

Anneal

- Reduces fixed oxide charge
- Creates a low resistance ohmic contact to the source and drain.

Final Devices

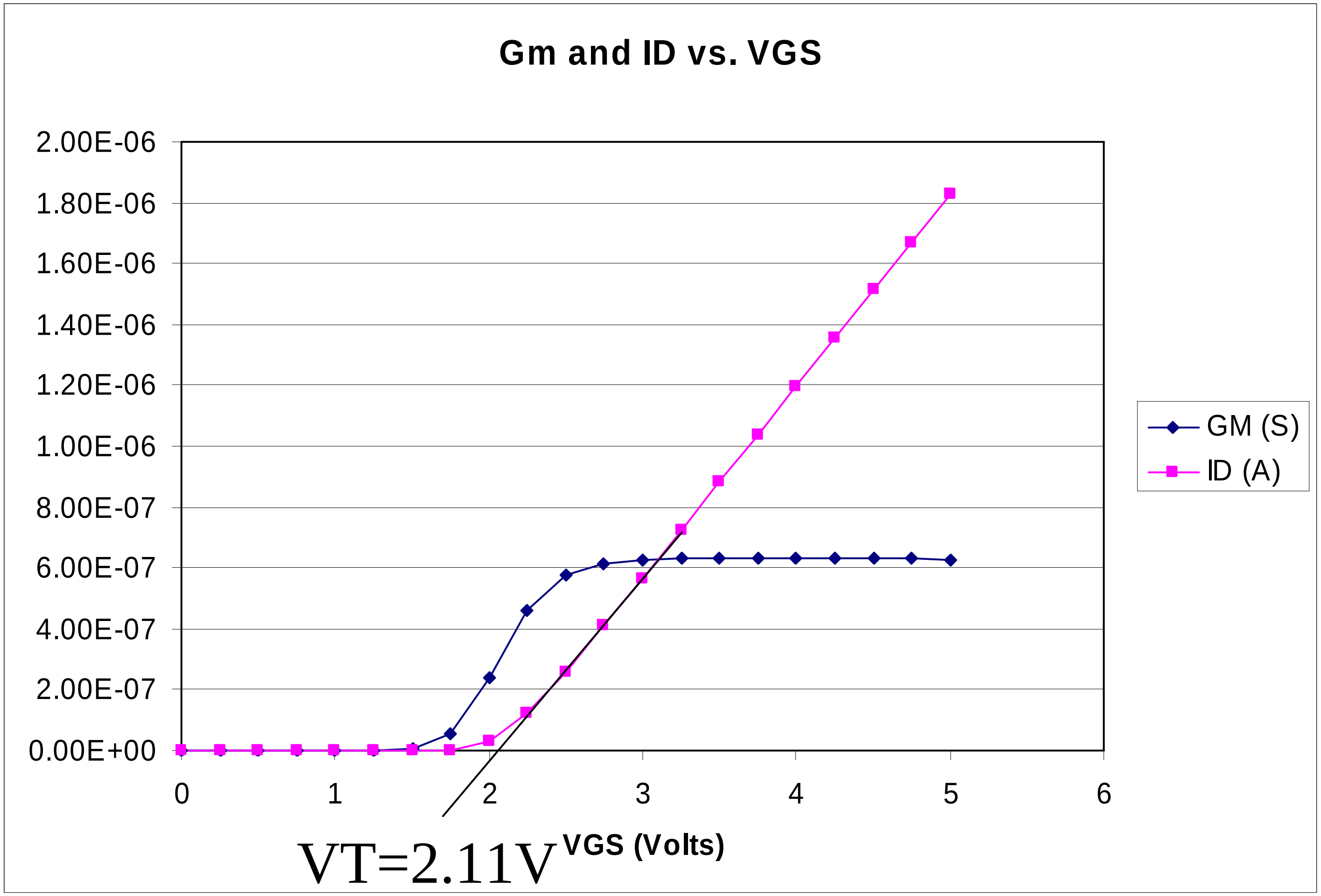


Test the Devices

- Proves your process worked!
- Makes you truly understand how a transistor works.
- One of the most sought after skills this course teaches.
- You can see if your professors know what they are talking about!

From simulation.

Thin oxide



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