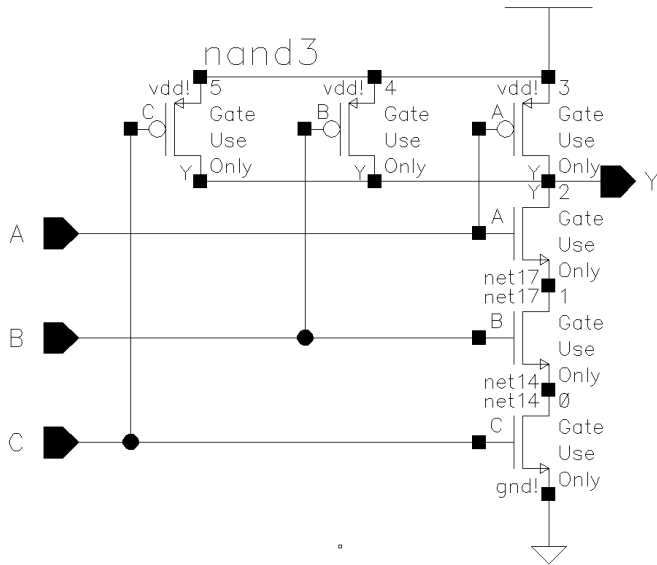


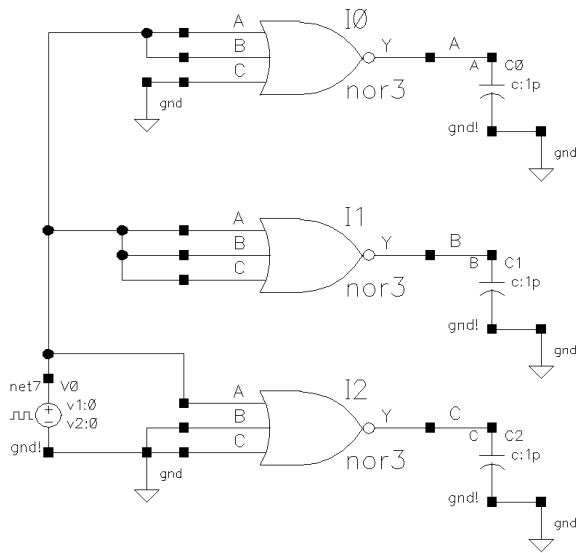
Question 1 (20 PTS):

You are designing a FLIP FLOP that uses three input NAND GATES that have both reset and set. You know that the reset and set pins will hardly ever be used to set or reset the circuit. Which pins do you put the set or reset on to make the circuit as fast as possible? You do not need to know the exact structure of the FF. Explain why for full credit.



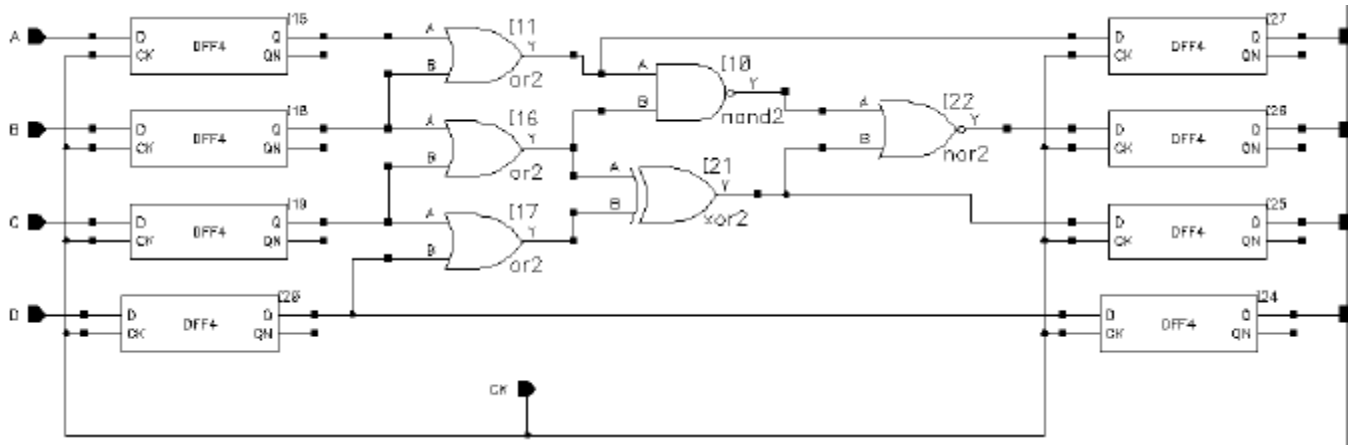
Question 2 (10PTS):

Which circuit will have the fastest fall time?
 Why?
 Which circuit will have the slowest fall time?
 Why?



Question 3 (50PTS):

Below is a circuit that needs to run at 200MHz. Describe how you would go about making sure that the circuit can function at this speed. Explain the process you would go through to find WN WP for each gate.



Question 4 (20PTS):

Draw a set of test vectors that will demonstrate a set up error on a DFF with a setup and hold time of 2ns.

Question 5 (20PTS):

Using the AOI technique design a CMOS circuit to implement the following logic function **that minimizes propagation delay**.

$$Z=(AB+C+DEF)G$$

Show the PNET and the NNET connected into a circuit

Question 6 (10PTS):

Using the Euler path method come up the order of the inputs for the circuit in question 5. **(5pts.)**

Show stick diagram (5pts)