Area Delay Product

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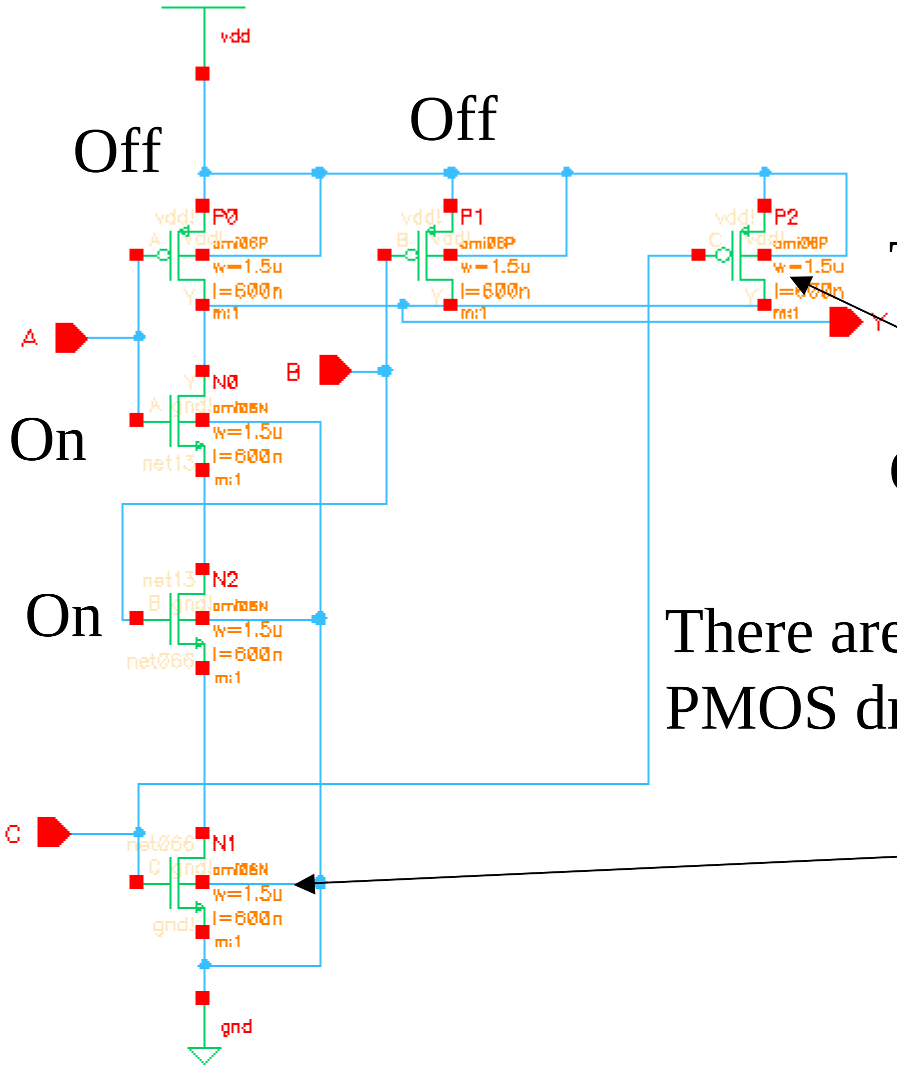
NAND Example

- We want to design an optimized 3 input NAND gate with symmetric rise and fall time for the worst case transitions. (The load will be 3 NAND3 gates)
  - We want to optimize for **speed** and **area**.
  - Of course these are opposing criteria.
    - **Area goes up, when you increase the width of the transistors to have smaller (faster) delay times.**
  - Note: Symmetric rise and fall times leads to better noise performance.

What are the “worst-case” transitions?

- Rise time or propagation delay low to high:
  - Only one PMOS is available to charge to VDD
- Fall time or propagation delay high to low:
  - Does it make a difference both NMOS transistors have to be on to discharge?
    - Yes! If the bottom most NMOS turn on after the other NMOS in the tree, then the output load capacitance is composed of all the drain caps in the tree!

Low to High Worst Case



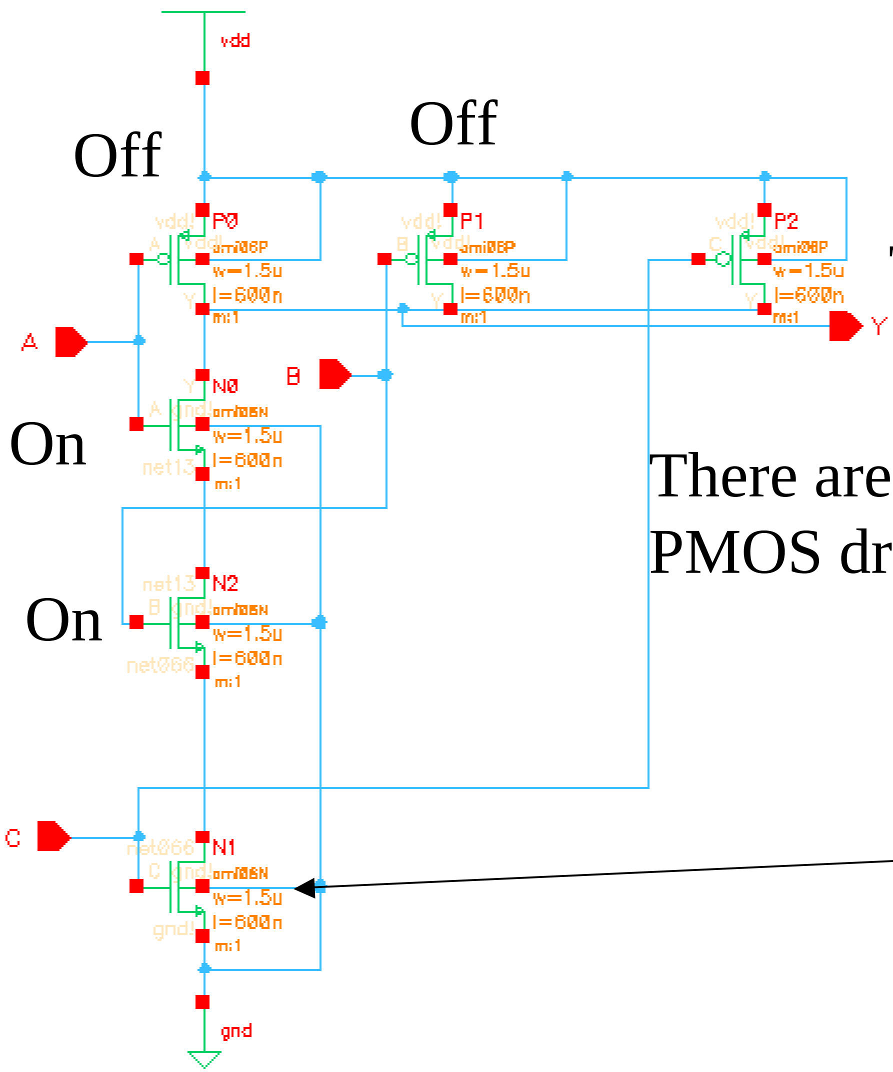
Turns On

Only one PMOS conducts

There are 5 NMOS drain caps and three PMOS drain caps to charge

Turns Off

High to low Worst Case

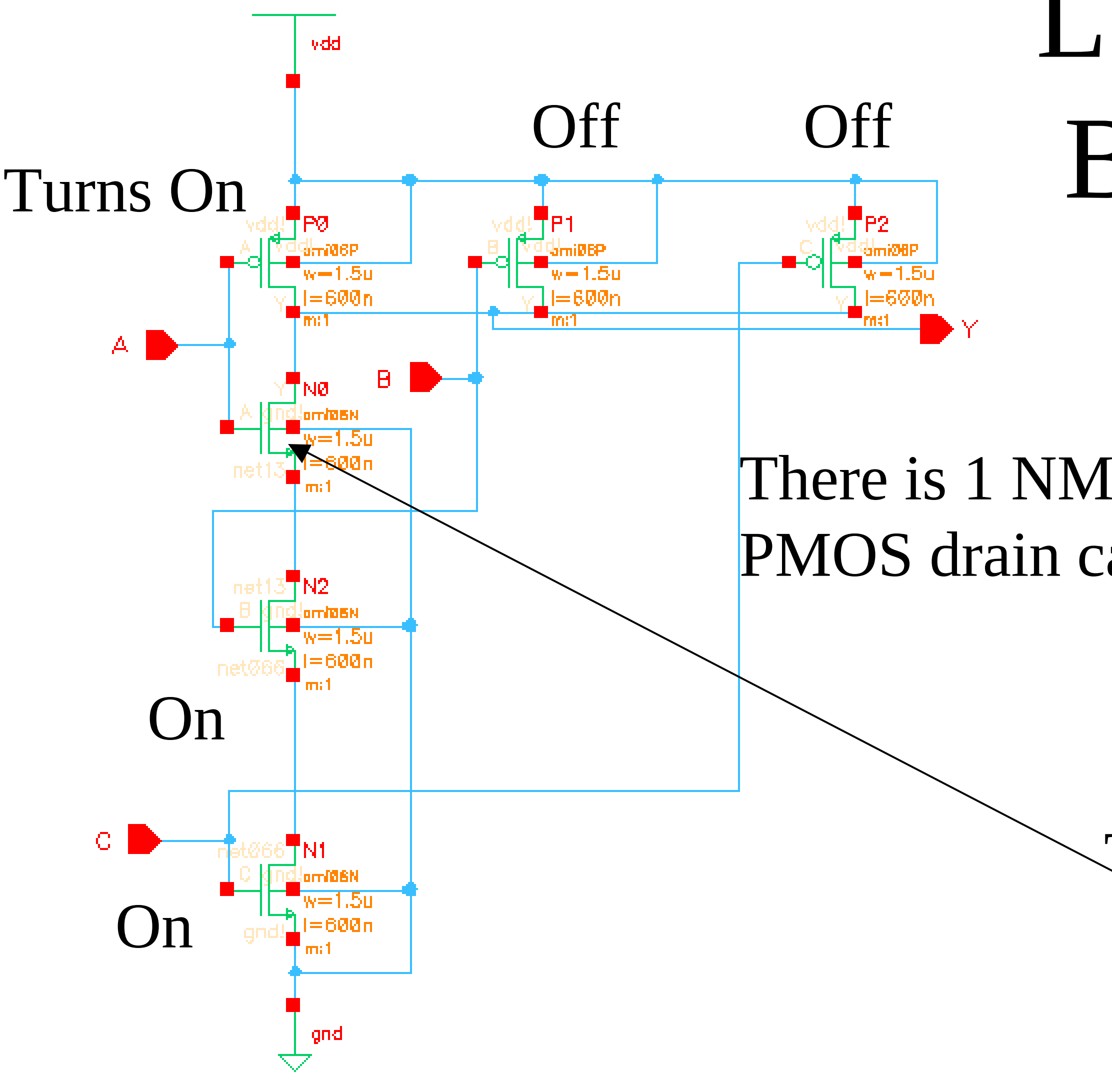


Turns Off

There are 5 NMOS drain caps and three PMOS drain caps to charge

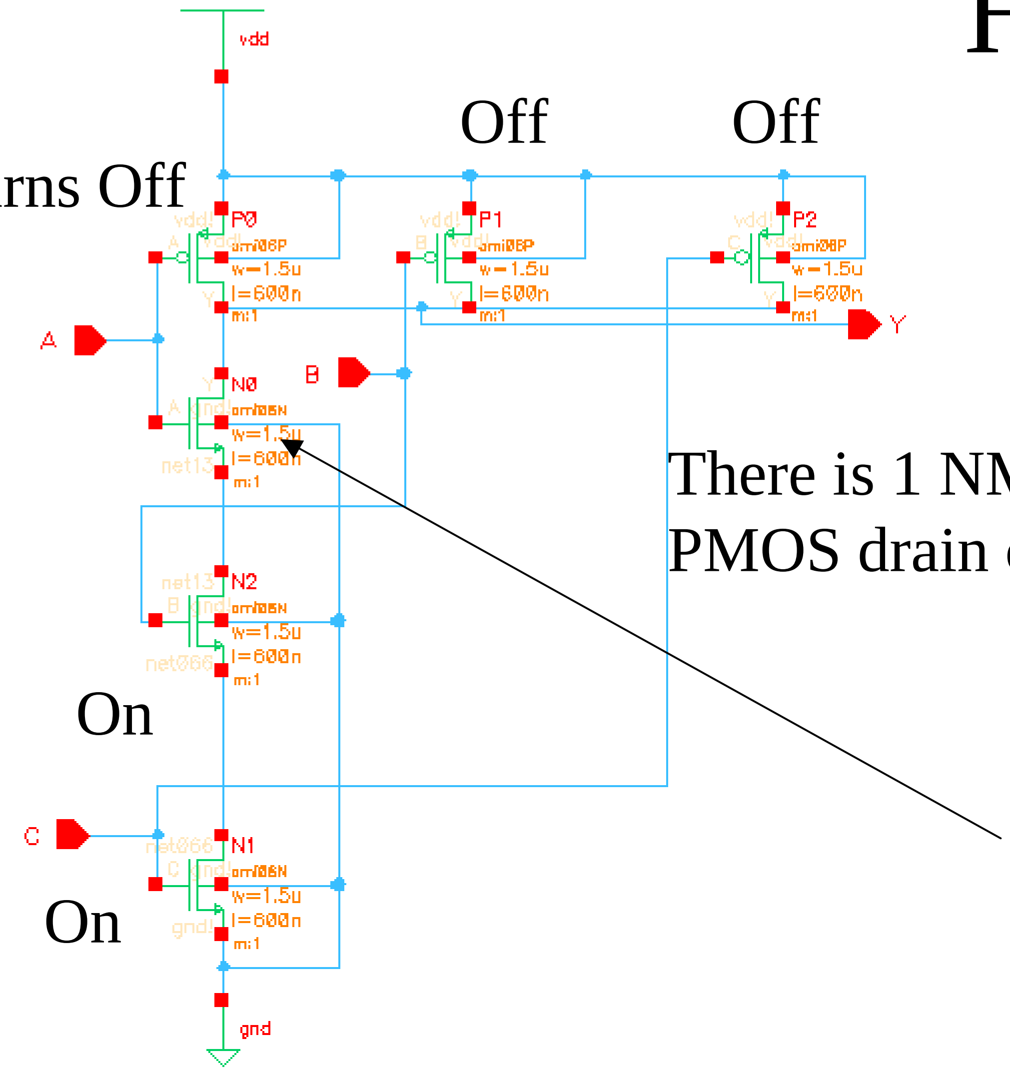
Turns On

Low to High Better Case



There is 1 NMOS drain cap and three PMOS drain caps to charge

High to Low Best Case



Turns Off

Off

Off

On

On

There is 1 NMOS drain cap and three PMOS drain caps to discharge

Turns On

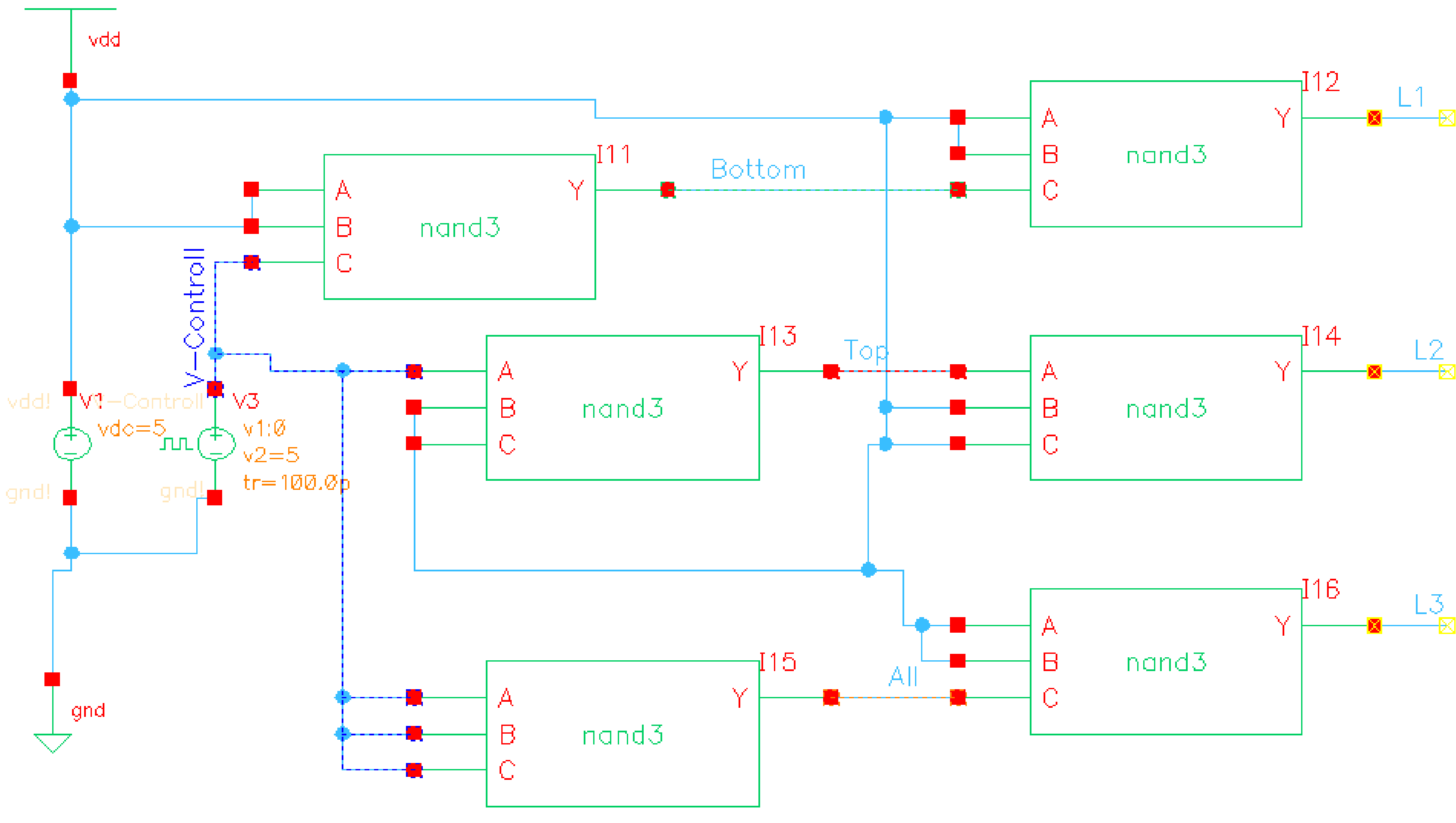
What if all the inputs were tied together?

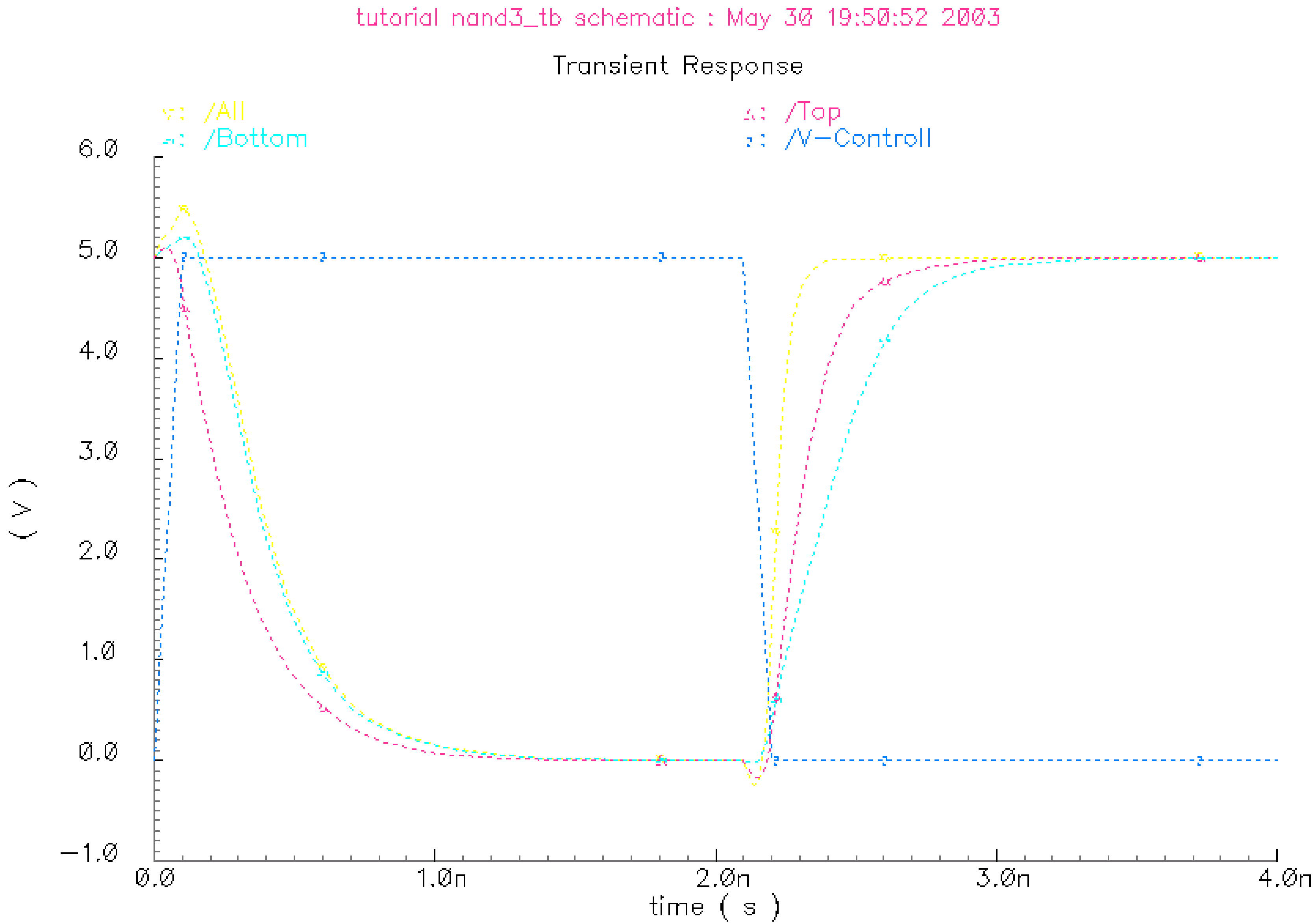
- The charge times would be the fastest
- The discharge time would in fact be slower because more PMOS would be trying to charge until they are turned off!
- More feedback capacitances would be seen.

What to do?

- If possible have the signal that controls the gates state closest to the output node.
- Make sure that you realize that the noise performance will change depending on how many PMOS transistors are conducting.
  - The more PMOS transistors conduct the higher the switching threshold in an NAND configuration.

Setting up a NAND3 test bench

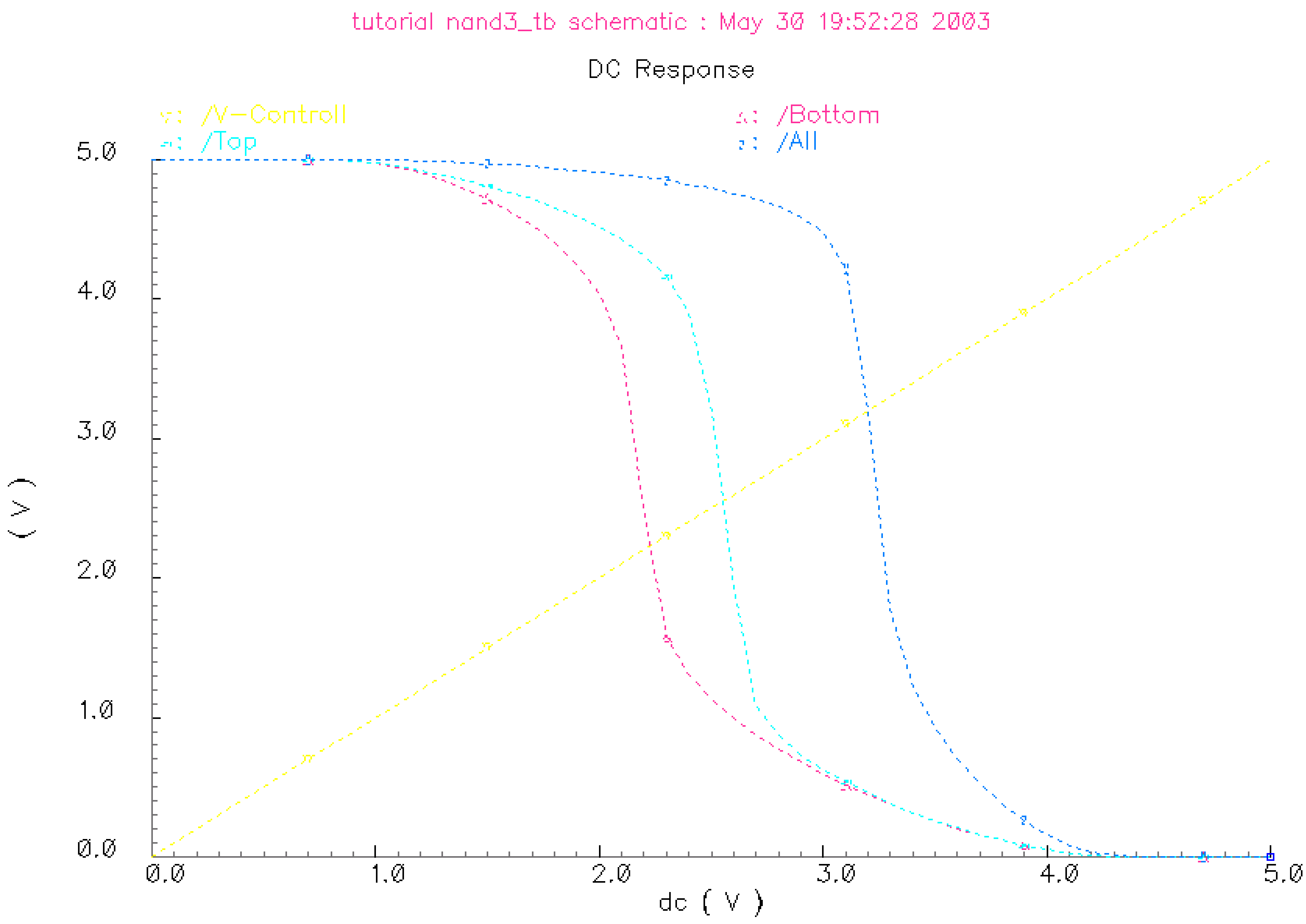




tutorial nand3_tb schematic : May 30 19:50:52 2003
Transient Response
/All
/Bottom
/Top
/V-Controll
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
(V)
0.0
1.0n
2.0n
3.0n
4.0n
time (s)

Summary

- Having the top NMOS transistor control the signal is faster that having the bottom transistor control the signal.
- Having all the inputs toggle at the same time improves the rise time, but degrades the fall time.
- Having all the inputs toggle is no more than having an inverter (logically), so why bother?
  - Maybe you need an inverter with a different noise performance.

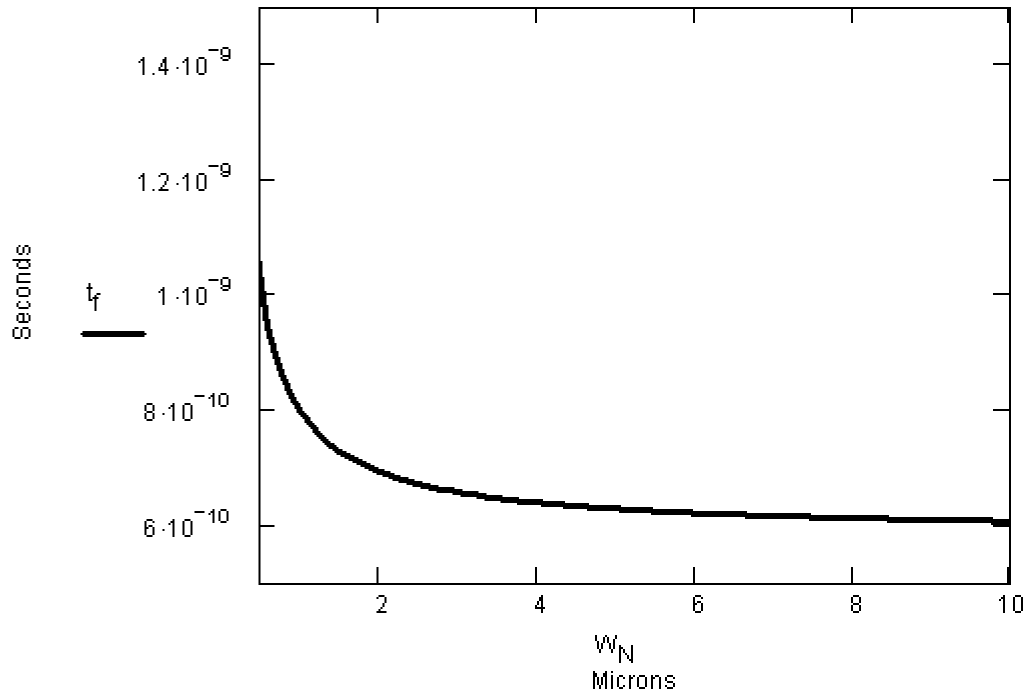

tutorial nand3_tb schematic : May 30 19:52:28 2003
DC Response
/V-Controll
/Top
/Bottom
/All
5.0
4.0
3.0
2.0
1.0
0.0
(V)
0.0
1.0
2.0
3.0
4.0
5.0
dc (V)

Estimating the delay

- We now know which test vectors will produce the slowest delay
- Now we need to:
  - Calculate the input and output capacitances of a NAND3 gate, assuming that the NAND3 will drive 3 identical NAND3 gates and that WP=WN.
  - Then we calculate the fall time vs. WN.

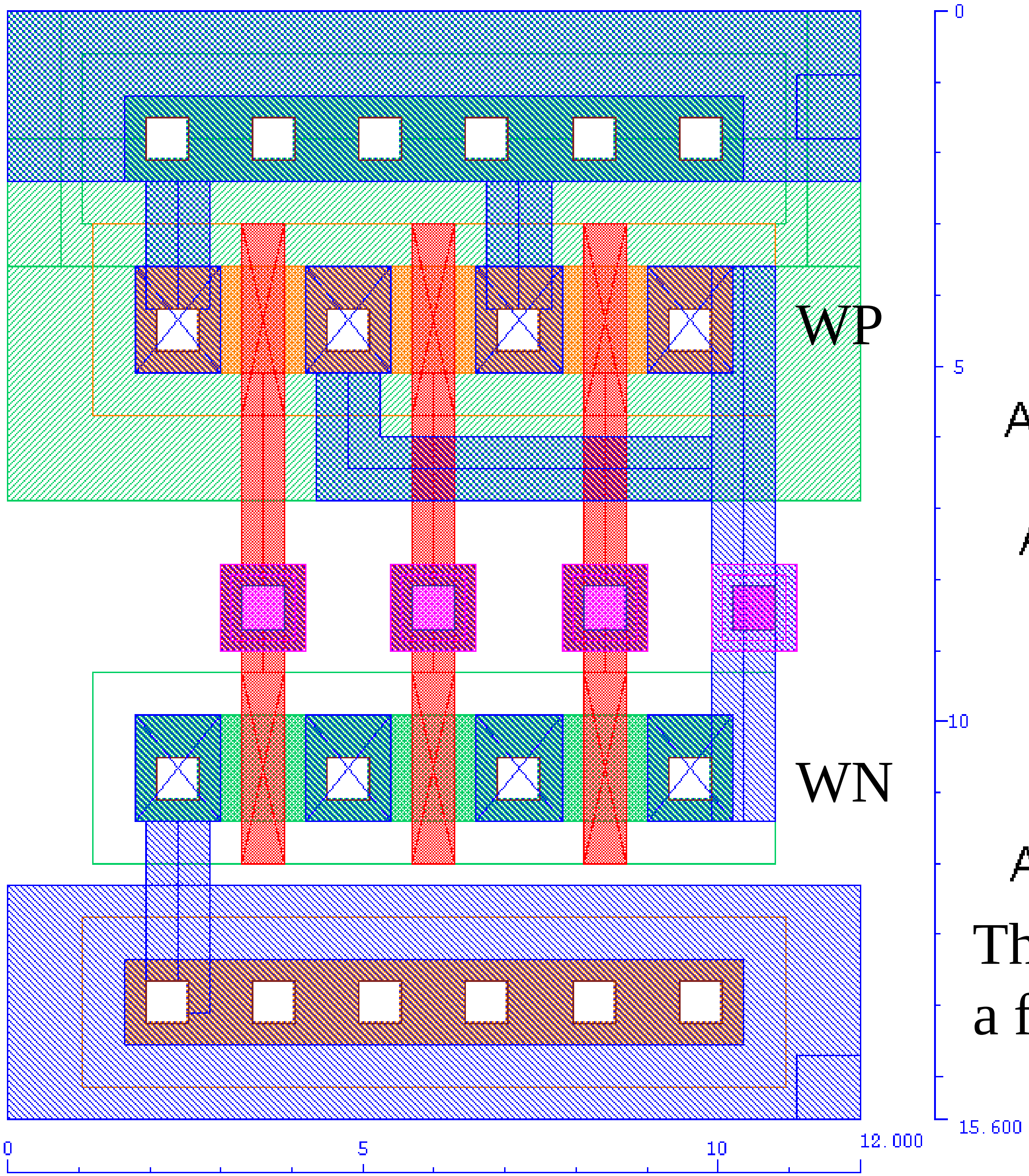
Delay vs. Width

- We need to plot delay vs. WN (Assuming WP=WN)



Area vs. Width

- We need to come up with an equation for the area of a NAND3 Gate vs. width.
- Since you have to lay it out any way the easiest thing to do is layout the minimum sized NAND3 and come up with how much the area increases with WN and WP



First we calculate the area of the NAND3 if WP and WN=0

$$A_{MIN} := 15.6 \cdot 12 - 1.5 \cdot 12 - 1.5 \cdot 12$$

$$A_{MIN} = 1.51 \times 10^{2}$$

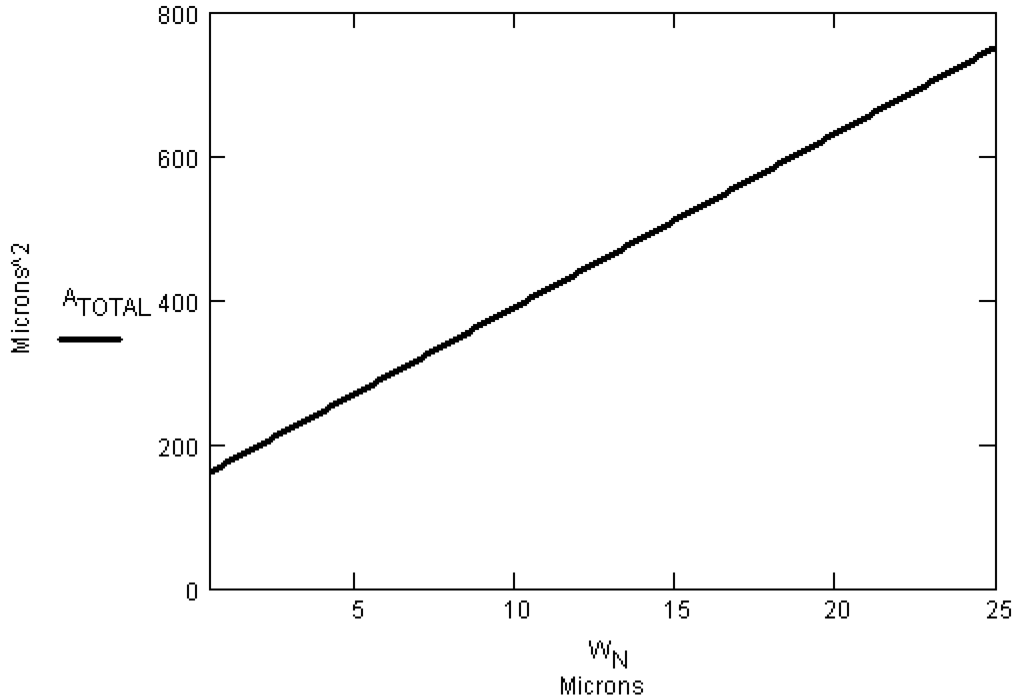
Then we calculate the extra area per WN.

$$A_{EXTRA} := \left(W_N + W_P\right) \cdot 12$$

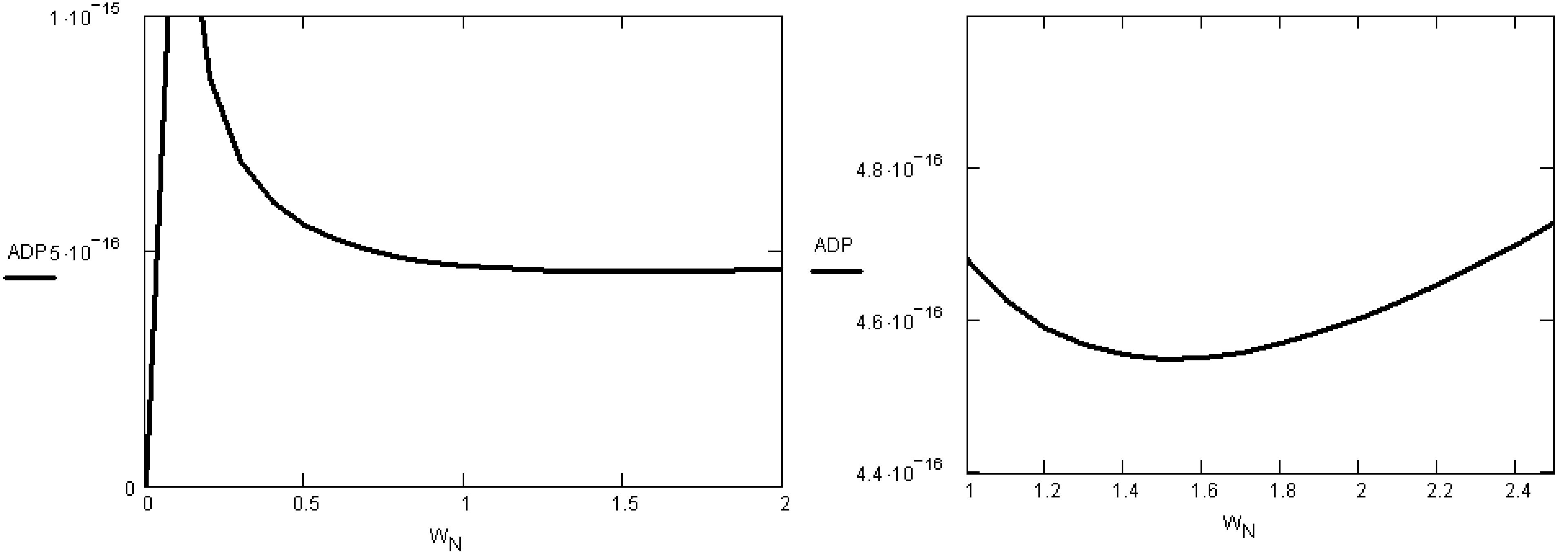
Then we calculate the area as a function of WN and WP=WN

$$A_{TOTAL} := A_{MIN} + A_{EXTRA}$$

Area vs. WN for NAND3



Area Delay Product for NAND3

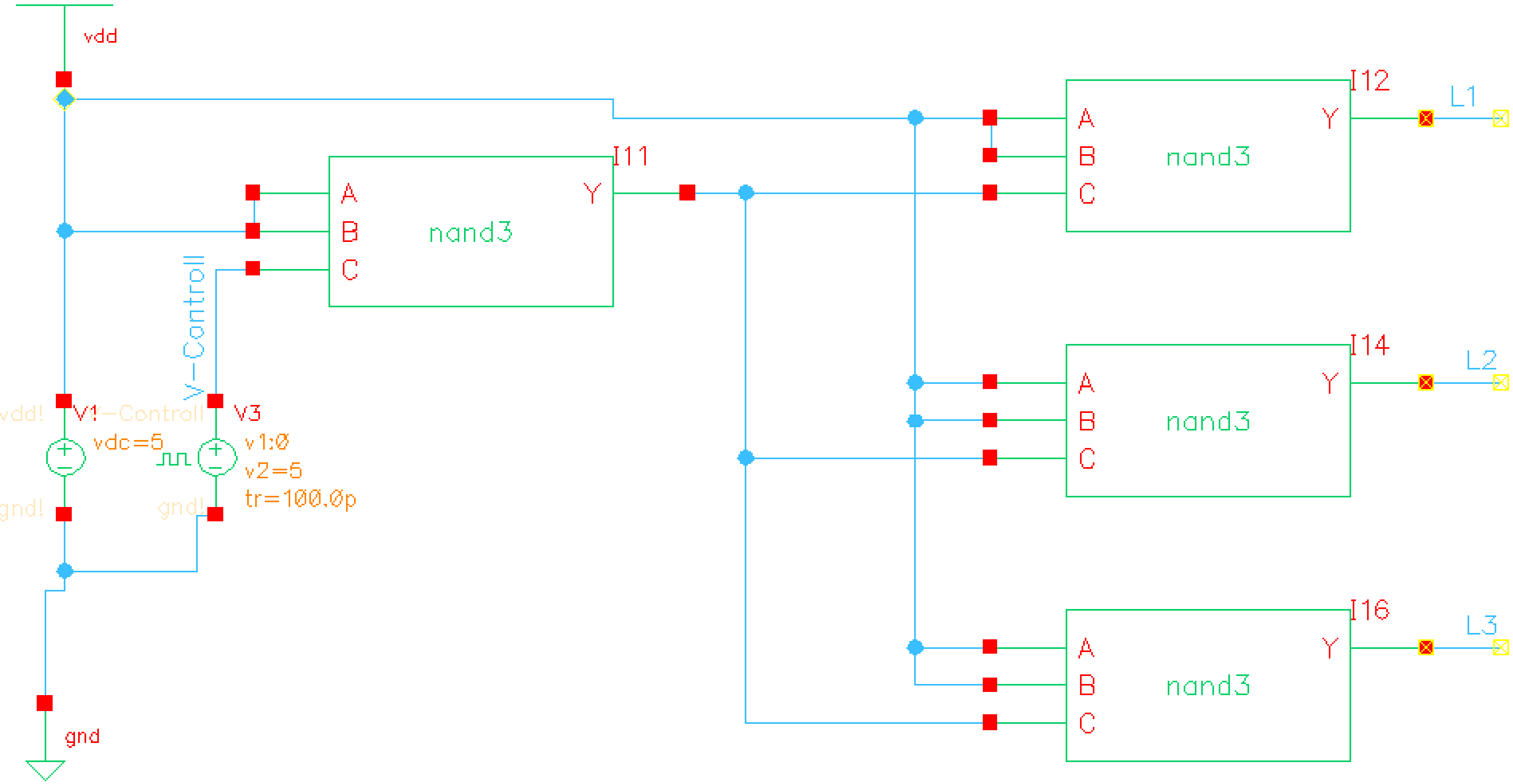


So it looks like the best width to use for ADP is 1.5μm!
Note:Anything from 1 to 3 is probably ok since the ADP is slowly varying.

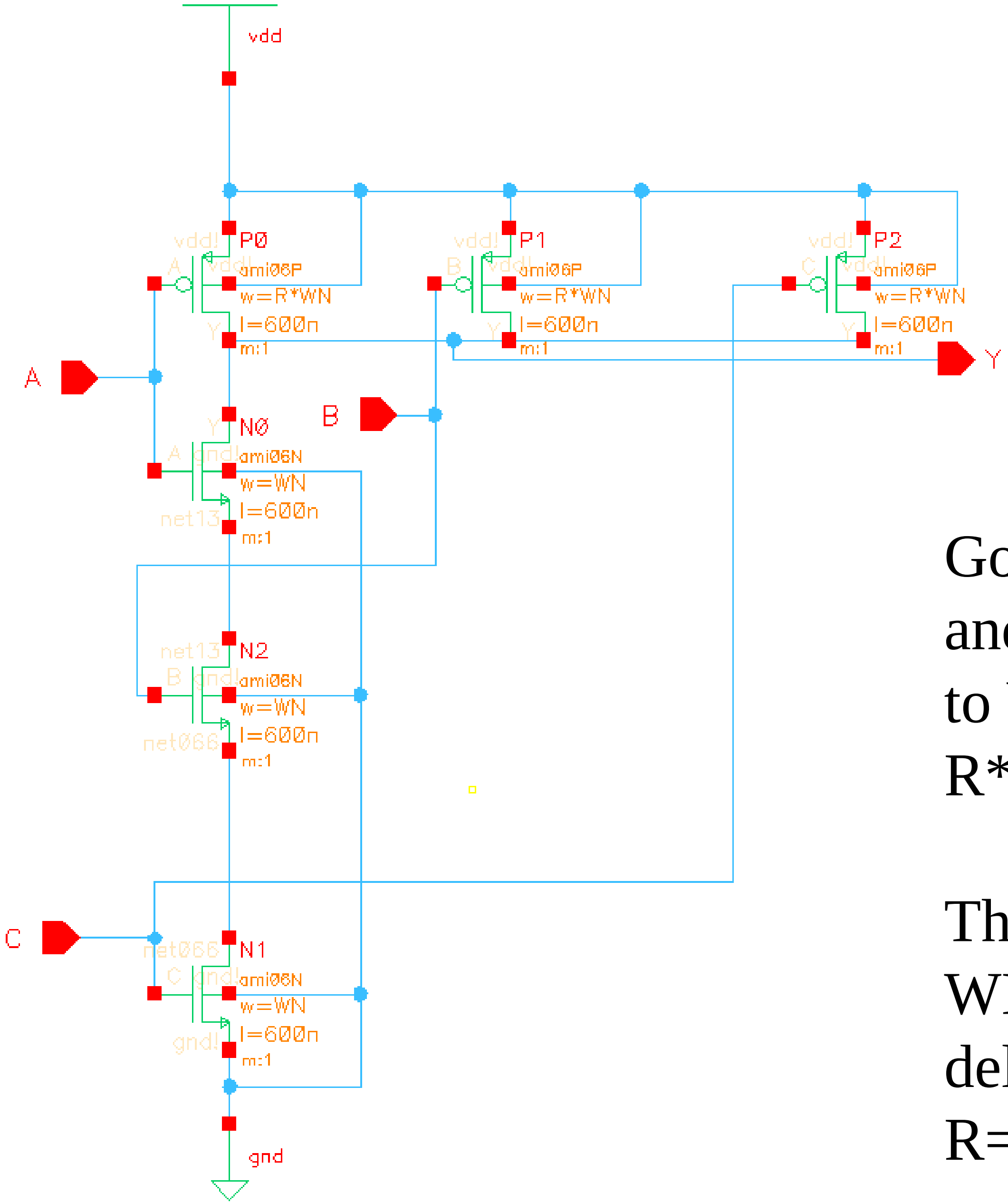
Does this match spice?

- We made a lot of assumptions for these hand calculations.
  - Capacitance is constant
  - The C constant does not change with width.
  - The inputs changed instantaneously.
- We had better run this through spice to double check.

Test Bench

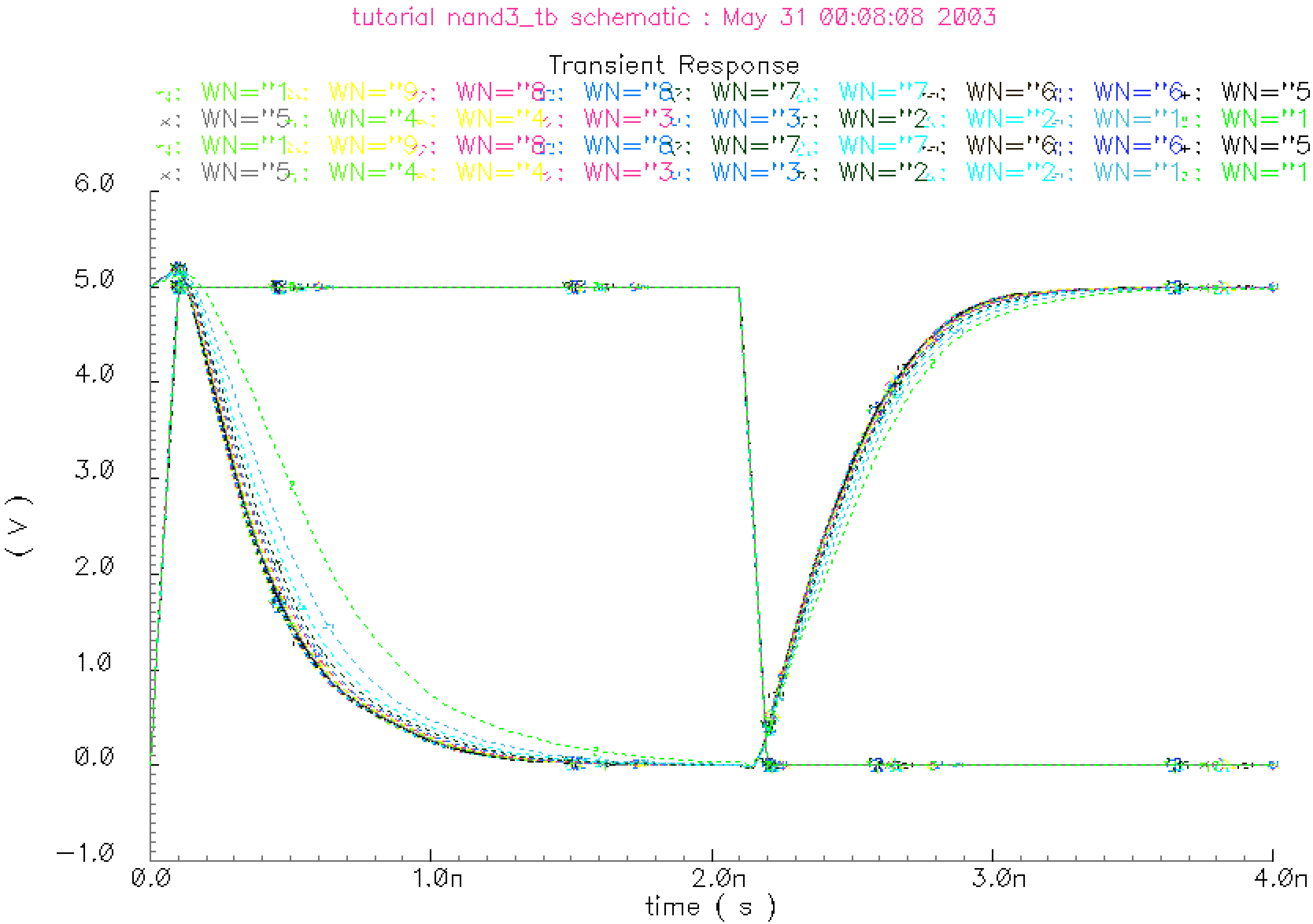


vdd
I12
L1
A
B
C
Y
nand3
I11
A
B
C
Y
nand3
I14
L2
A
B
C
Y
nand3
I16
L3
A
B
C
Y
nand3
V–Controll
vdd!
V1
V–Controll
V3
vdc=5
v1:0
v2=5
tr=100.0p
gnd!
gnd!
gnd



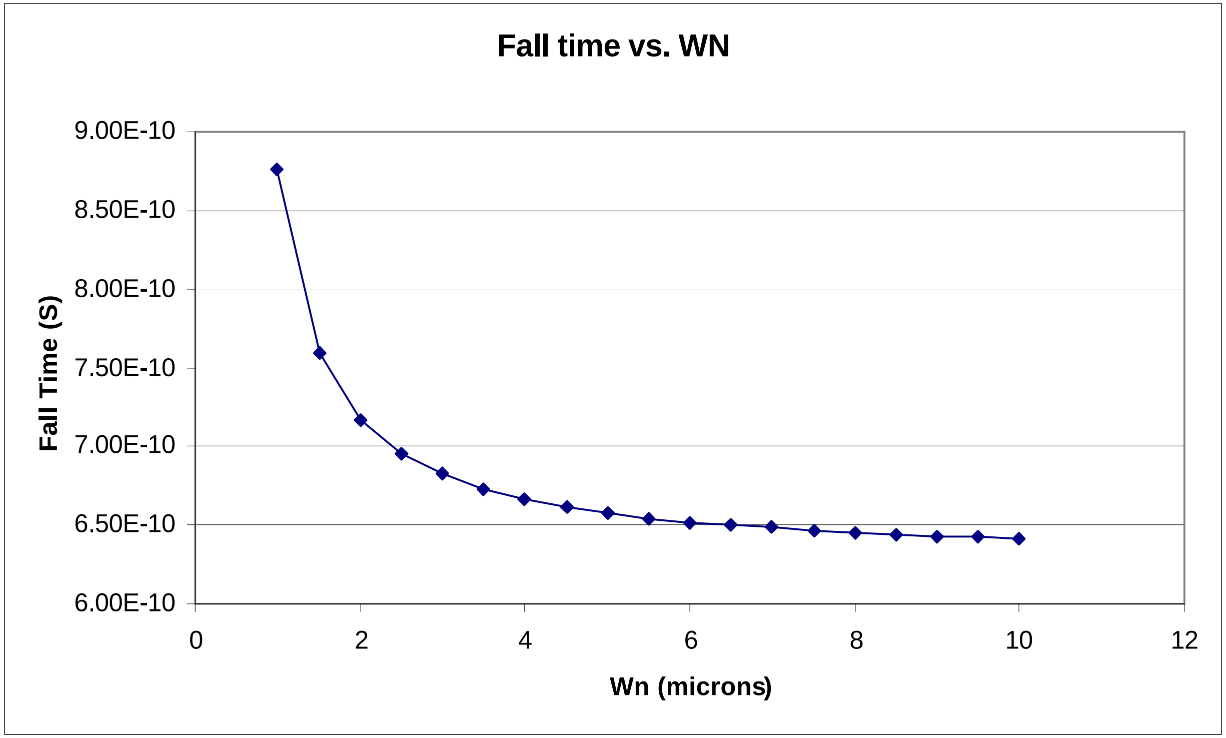
Go into the schematic and change all the widths to WN for nmos4 and R*WN for pmos4

This will allow us to sweep WN and WP and measure the delay as a function of WN
R=1

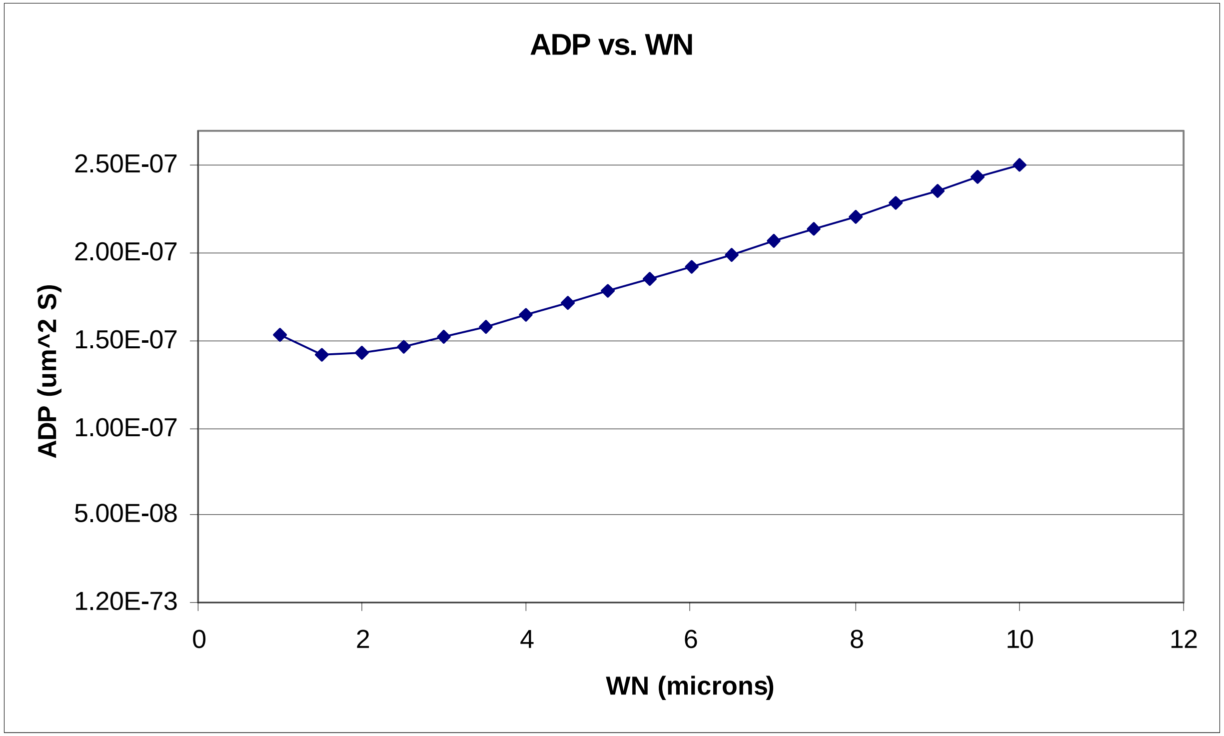

tutorial nand3_tb schematic : May 31 00:08:08 2003
Transient Response
6.0
5.0
4.0
3.0
2.0
1.0
0.0
−1.0
(V)
0.0
1.0n
2.0n
3.0n
4.0n
time (s)

Results From Spice

The maximum error is ~5% at WN=10μm.



Results From Spice



Results are the same! WN should be 1.5 for best ADP