

EE224

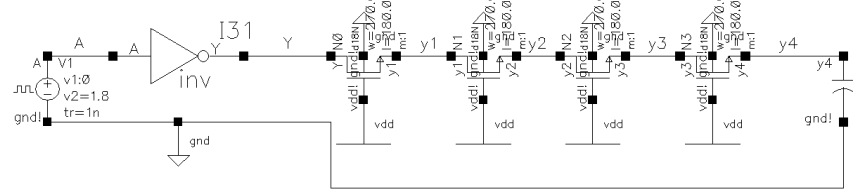
Class 4

D. W. Parent

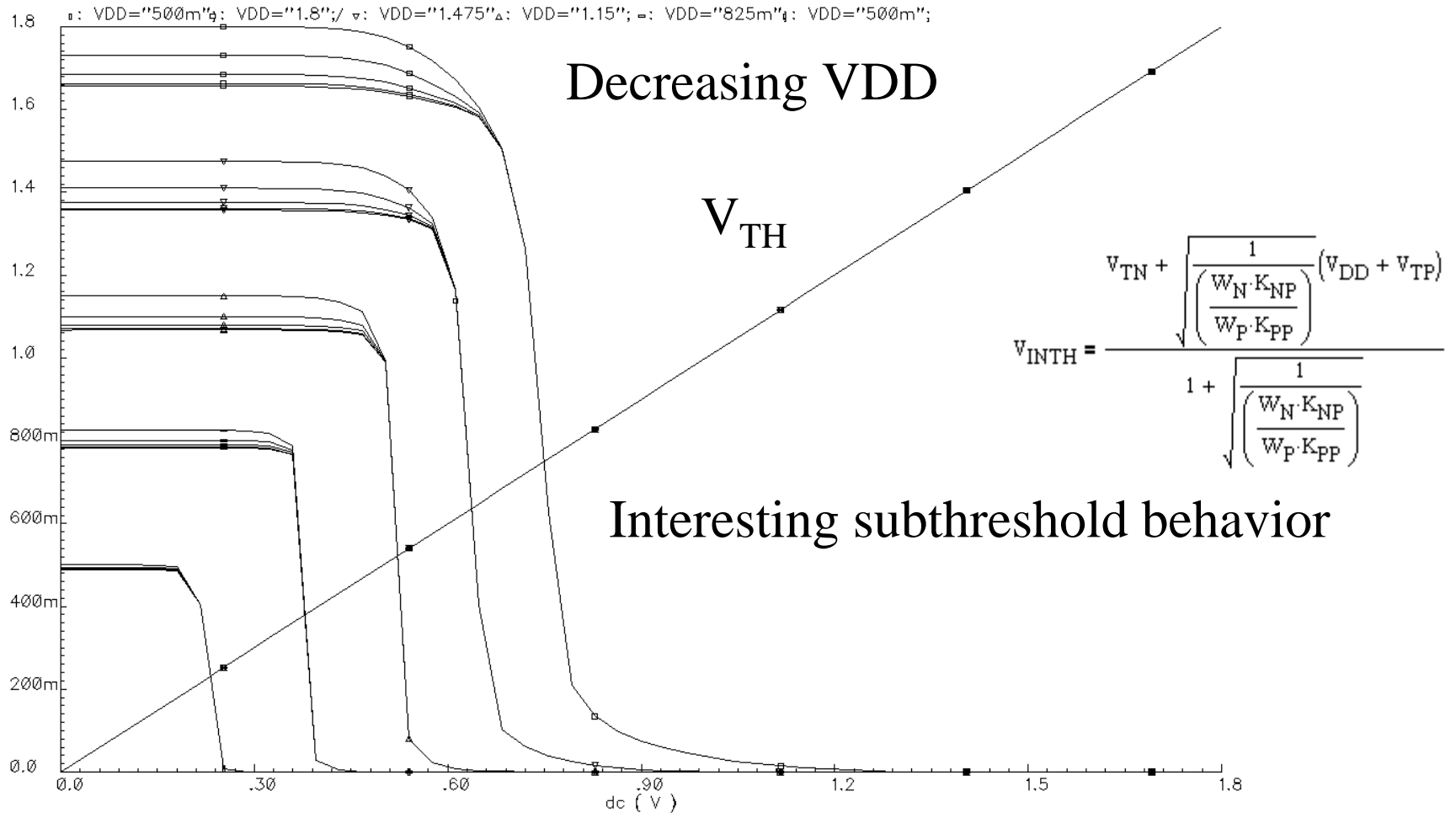
Topics

- DC Repose CMOS inverter
- Complex AOI Logic
- Pass Gates
- High Z and Contention
- Multiplexers
- Sub threshold operation

Noise?



DC Characteristics



Strength

- NMOS pass ground signals well.
 - V_{TN}
- PMOS pass power signals well.
 - V_{TP}

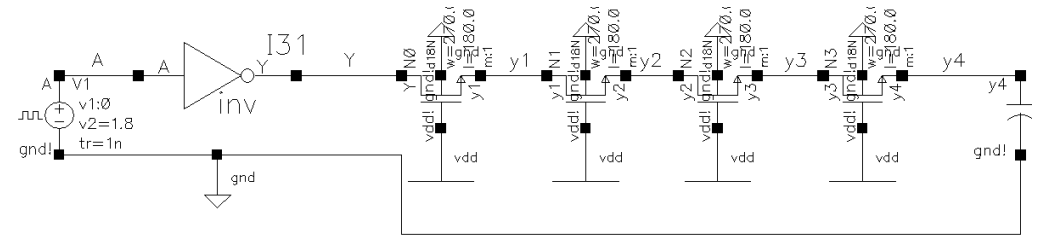
Complex Logic

- NAND series nmos, parallel pmos
- NOR parallel pmos, series nmos
- AOI (And Or Invert)
 - Examples
 - AOI321
 - AOI222
 - AOI22

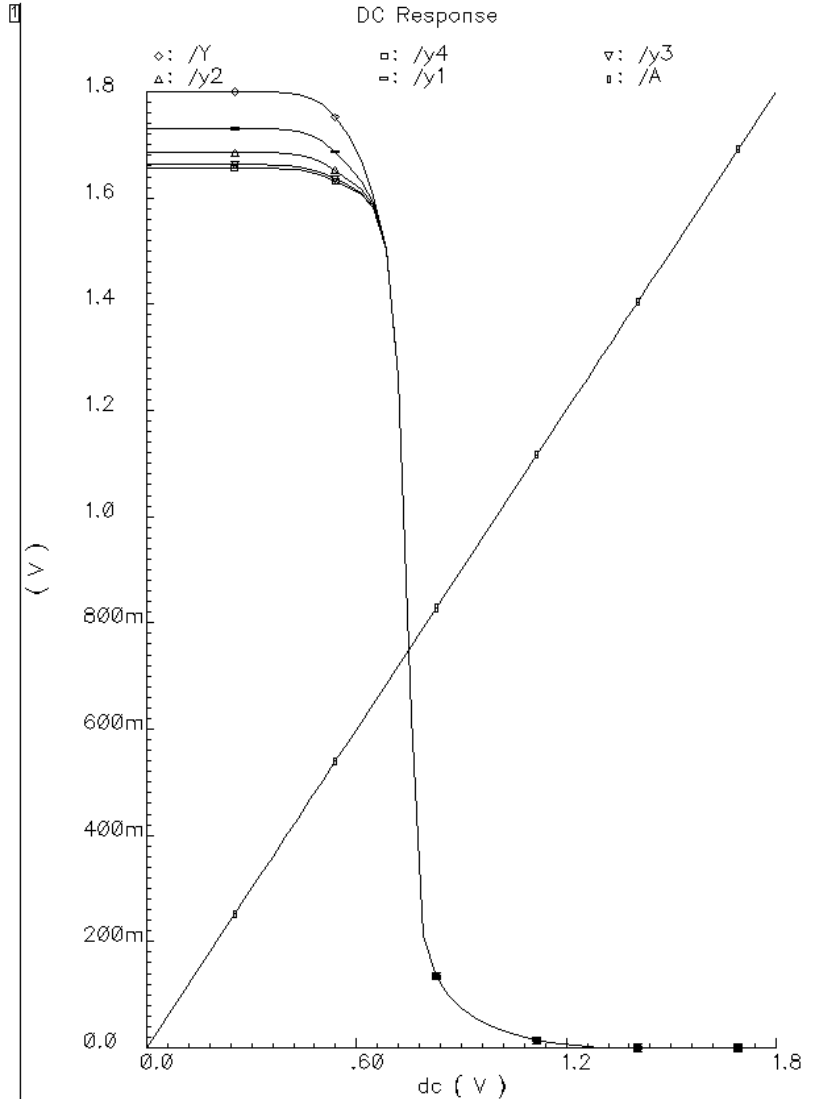
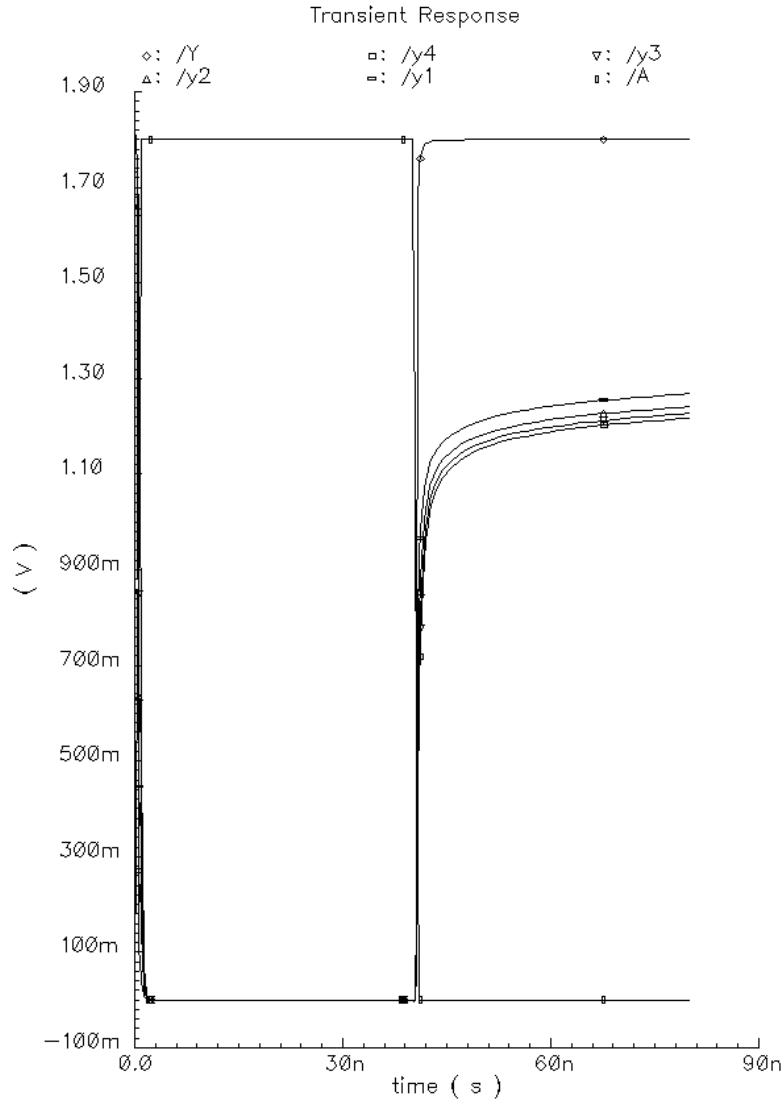
Other CMOS Configurations

- Pass Gate
- Non-Complementary
 - high Z

Pass Gate Chain



TSMC18 inv_tb2 schematic : Sep 7 17:19:23 2005

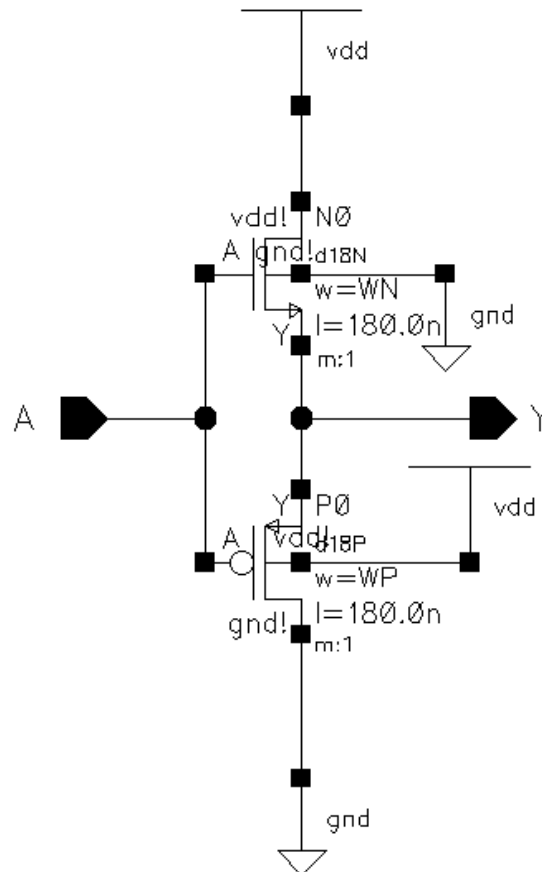


Multiplexers

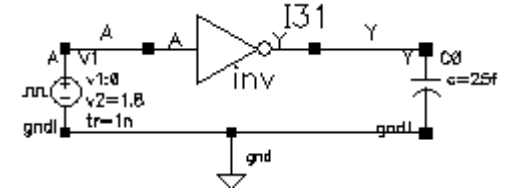
- Boolean logic gates
- AOI
- Tristates buffers

Do example from KMAP.

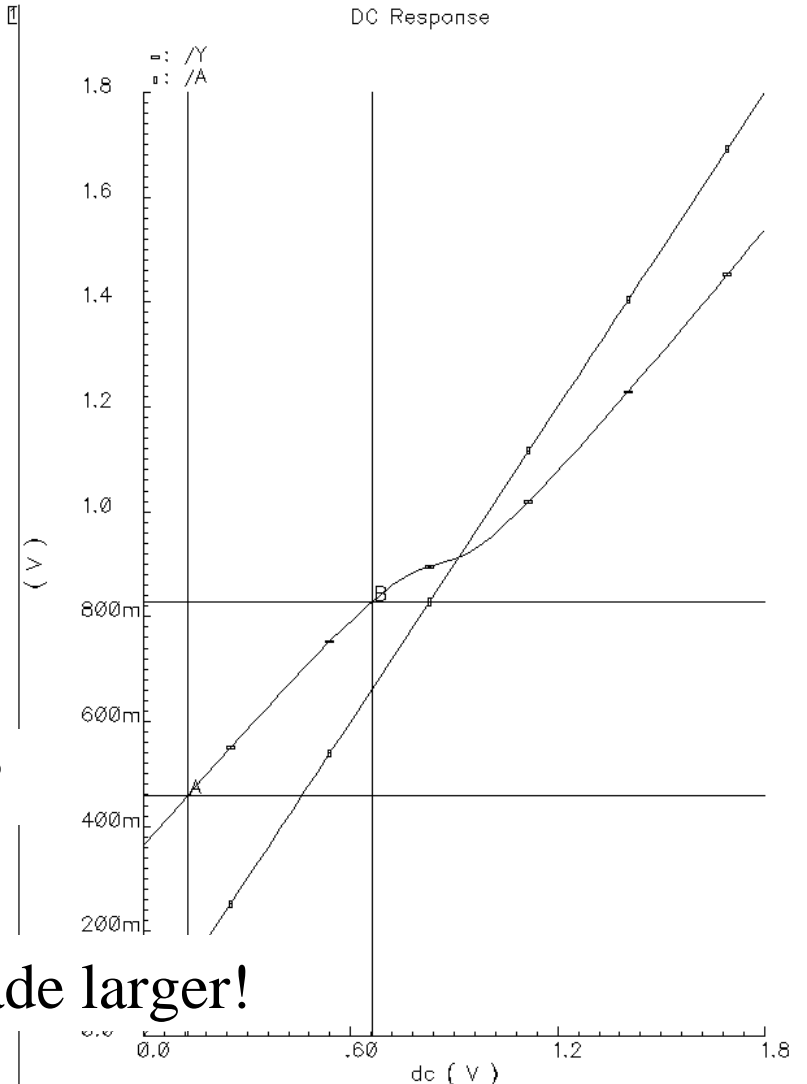
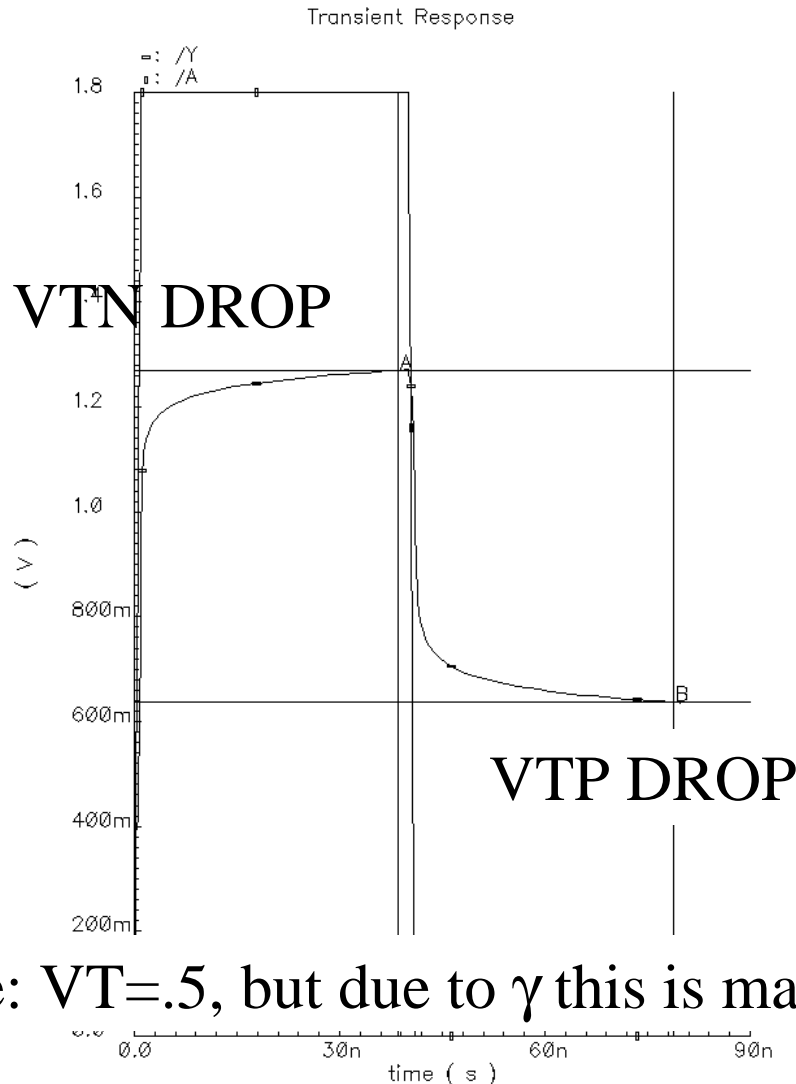
Can we make non-inverting logic?



NO GAIN!



TSMC18 inv_tb2 schematic : Sep 7 16:45:52 2005



Note: $V_T = 0.5$, but due to γ this is made larger!

A: (38.5552n 1.26951) delta: (40.2394n -833.001m)
 B: (78.7946n 636.606m) slope: -15.7309M

A: (126.853m 458.264m) delta: (535.255m 370.339m)
 B: (662.108m 828.603m) slope: 091.894m

Ring Oscillator

tsmc6to inv_tb2 schematic : Sep 7 17:31:00 zww

Transient Response

■: frequency(VT("/RO_FAST" "/export/home/staff/dparent/cadence/simulation/inv_tb2/spectreS/schematic"))

