

EE224

Class 3

D .W. Parent

# A Review of MOSFETs

- Diodes
- Symbols
- Fabrication
- Regions of Operation
- Ideal Characteristics
- Short Channel Effects
- Design Perspective

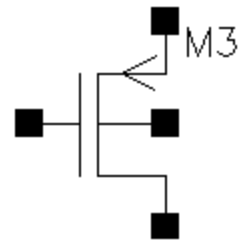
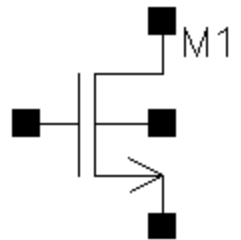
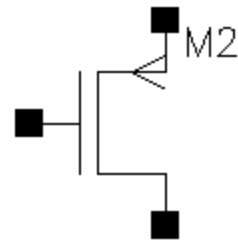
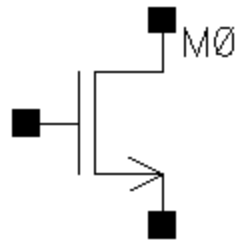
# Diodes

- N-type semiconductors have excess electrons which behave like electrons in free space with a modified mobility
- P-type semiconductors have excess vacancies which behave like electrons with a positive charge
- When a P region touches an N region the electrons and holes diffuse to the onsite regions. recombine and create a depletion region.
- This is called a diode and current passes more easily in one direction than the other.

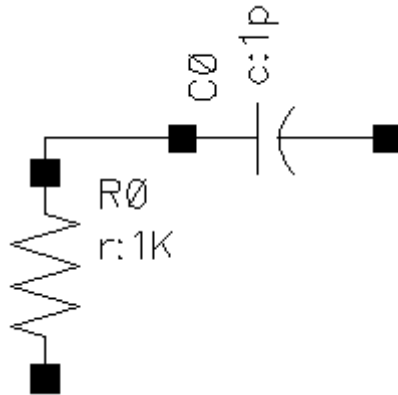
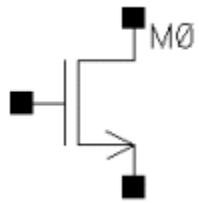
# MOSFETS

- Put two diodes back to back.
  - No current can flow
  - change the conductivity type of the material between the two connected diodes and current can flow.
  - Change it more and more current can flow.
  - We change the material by applying an electric field through a capacitance.

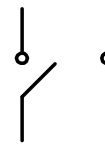
# Symbols



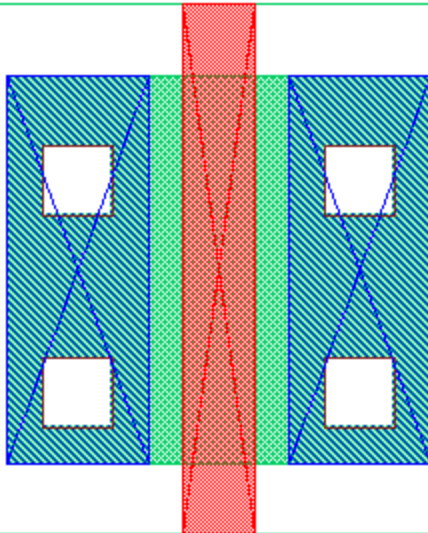
# Representations



open close



$$I_D = \frac{W}{2 \cdot L} \cdot K_{NP} \cdot (V_{GS} - V_T)^2$$

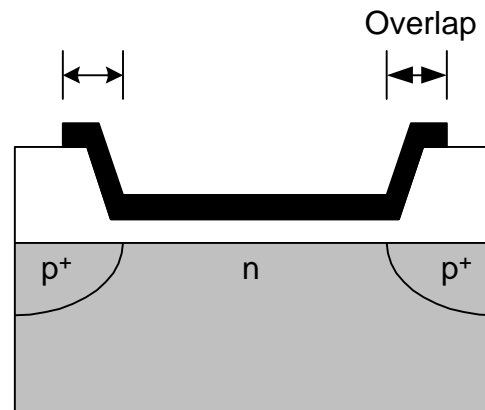


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* DATE: Aug 5/05
* LOT: T55U WAF: 4004
* Temperature_parameters=Default
.MODEL CMOSN NMOS (
+VERSION = 3.1 TNOM = 27 LEVEL = 49
+XJ = 1E-7 NCH = 2.3549E17 TOX = 4.1E-9
+K1 = 0.5911956 K2 = 3.921742E-3 K3 = 1.000151E-3
+K3B = 2.3408239 W0 = 1E-7 NLX = 1.651214E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.6194969 DVT1 = 0.4434883 DVT2 = 0.0377411
    
```

# Capacitance Effects and Self-Aligned Transistors

- There are several capacitances that limit the high frequency operation of MOSFETS.
- Non-Self Aligned is the worst case due to the metal overlapping the source and drain regions.



# Basic Fabrication Steps

- NWELL
- ACTIVE
- POLY
- NSEL
- PSEL
- CC
- METAL1

# Modern Enhancements

- Thin gates oxides
- Lightly doped drains
- High K dielectrics for gate
- Tungsten plugs
- Copper interconnect
- Low K dielectrics
- Design for manufacturability at the mask level

# Ideal MOSFET

- Cutoff, Linear and Saturation

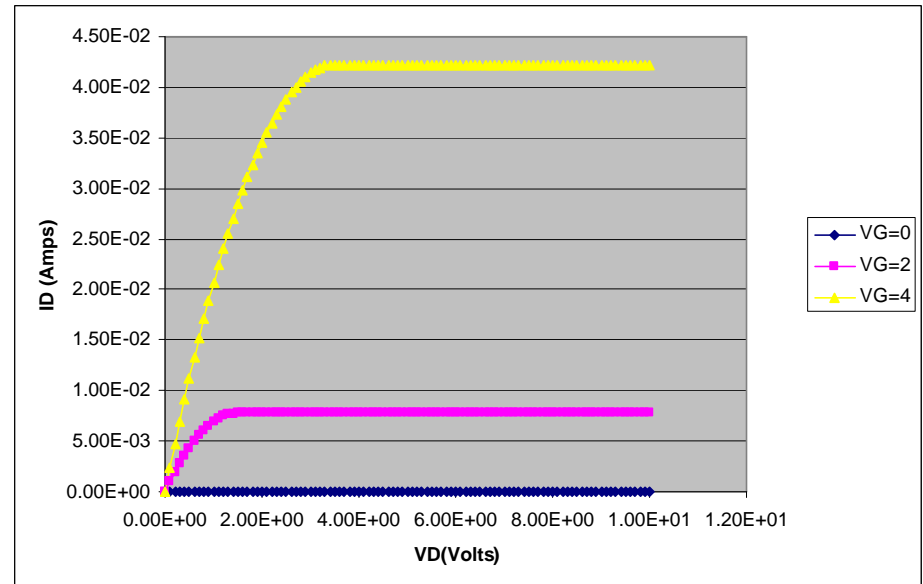
$$I_D = \beta \cdot \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

$$I = 0A$$

$$I_D = \frac{\beta}{2} (V_{GS} - V_T)^2$$

$$\beta = \mu \cdot C_{OX} \cdot \frac{W}{L}$$

$$I_{DSAT} = \frac{\beta}{2} \cdot (V_{DD} - V_T)^2$$



# Simple Gate Capacitance

- This changes with switching activity but is usually between 2/3 and 1 of below.

$$C_G = C_{ox} \cdot W \cdot L$$

# Drain Capacitance

- The drain bottom and side wall have different doping gradients and thus different depletion widths, and thus different capacitances.
  - These are lumped into CJSW and CJ parameters in the spice deck.
  - As we know depletion capacitance changes with voltage
    - We use an averaging method that reduce the drain cap about  $\frac{1}{2}$  the value when  $V_{diode}=0$

# Problems

- Reliability problems
  - electro-migration
  - hot-carrier degradation
  - oxide break down
  - electrical over stress
- Models stop working!!!!

# Short-Channel Effects

- Any MOSFET that behaves as if its channel length is short.
  - $X_j$  close to  $L_{eff}$ 
    - electron drift characteristics
    - modification of the threshold voltage
    - Large sub-threshold conduction current
  - Mobility
    - saturates if transverse electric field is more than  $10^5 \text{V/cm}$
    - degrades with increasing vertical electric field as well.
      - » Electron or holes are “squeezed” too close to the surface.

# Current

- The  $(V_{GS} - V_T)^2$  relationship changes to one of  $(V_{GS} - V_T)$

$$I_{DSAT} = W u_{dsat} C_{ox} (V_{GS} - V_T)$$

- The mobility degrades with increased gate voltage

$$m_n(eff) = \frac{m_{no}}{1 + h(V_{GS} - V_T)}$$

# Threshold Voltage

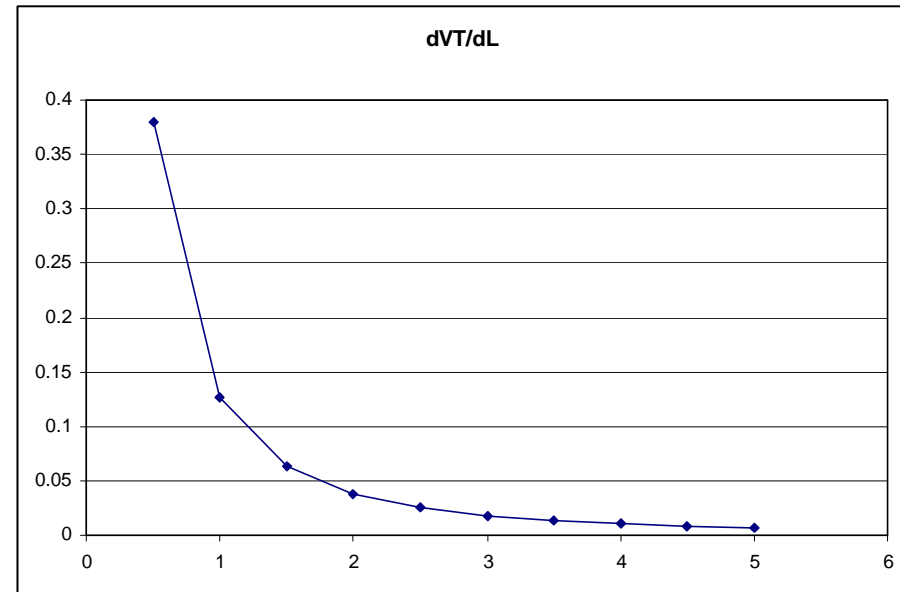
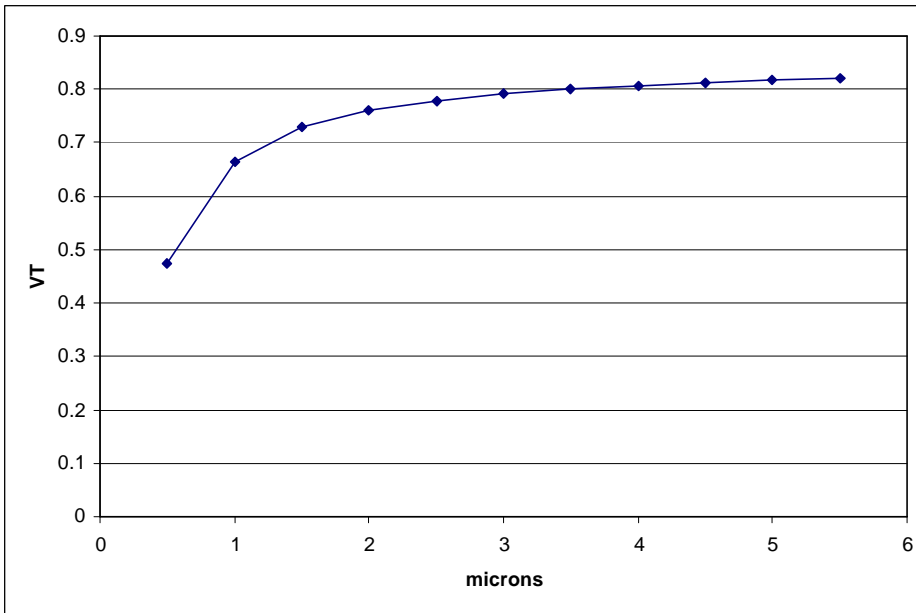
- Long Channel assumed:
  - depletion regions of the source and drain are small compared to the channel length
  - The regions are rectangular so the threshold voltage would be the same but the channel length would be effectively reduced.
- Short channel
  - depletion regions of the source and drain are large compared to the channel length
  - The regions are trapezoidal so the threshold voltage would be the same but the channel length would be effectively reduced.

$$\Delta V_{TON.C.L.} = -\frac{1}{C_{ox}} \sqrt{2q e_{Si} N_a |f_F|} \frac{x_j}{2L} \left[ \left( \sqrt{1 + \frac{2x_{ds}}{x_j}} - 1 \right) + \left( \sqrt{1 + \frac{2x_{dd}}{x_j}} - 1 \right) \right]$$

# Threshold Voltage

- In practice we use an empirical formula:

$$V_{TOSC} = V_{T0LC} - \frac{a}{L(\text{microns})}$$



# Other Small Geometry Effects

- Short Channel Width Effects

$$\Delta V_{TON.C.W.} = \frac{1}{C_{ox}} \sqrt{2q e_{si} N a |2f_F|} \frac{pxdm}{4W}$$

- Sub threshold current

$$ID(subthreshold) = \frac{qDnWx_c n_o}{L_B} e^{\frac{qfr}{kT}} e^{\frac{q}{kT}(AV_{GS} + BV_{DS})}$$

# Design Perspective

- Threshold drops
  - Pass transistors ( $V_{dd}-V_t$ ), body effect
  - Need to use complementary gates
- Leakage current
  - subthreshold
  - tunneling reduces charge storage time
  - use more power in standby
  - Increase delay

# Design Perspective

- VDD
  - Velocity saturation limits the benefits of a large VDD.
  - Decreases noise margin
- Delay
  - series transistors see less Efield so are less velocity saturation so are faster than you would expect
- Matching
  - Keep things close

# Summary