

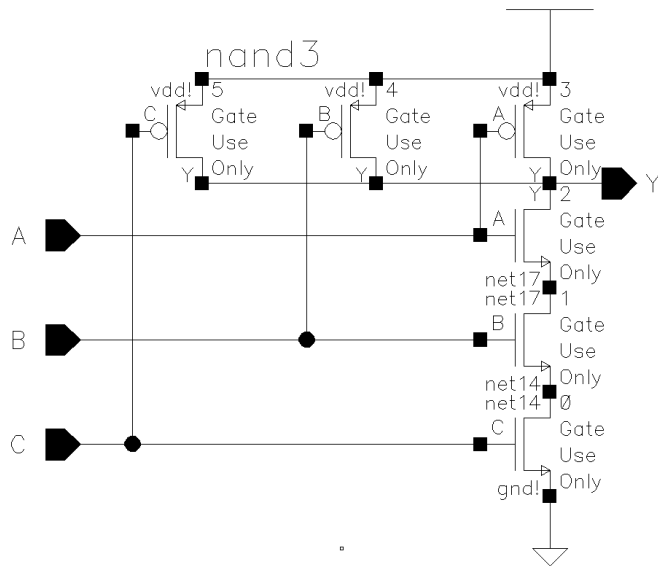
EE224 Class 2

D .W Parent
SJSU

Agenda

- We will use the quiz as a starting point for review of prerequisite concepts.
- The quiz is really some problems from the EE166 final.

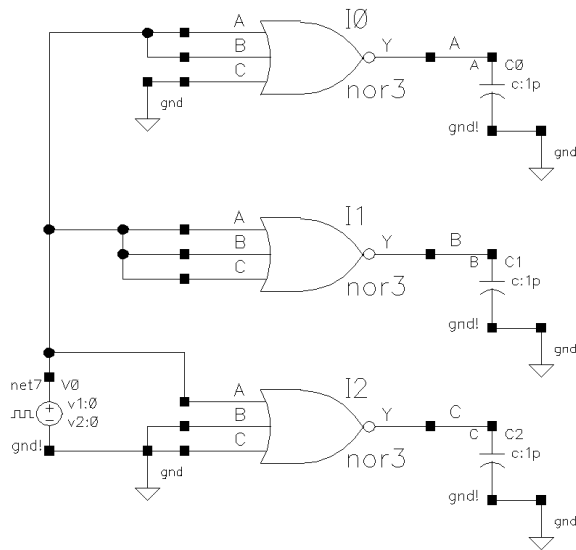
Which pins for set and reset?



During normal operation (passing D to Q) we want the delay to be as small as possible. If we use pin C as set or reset then C will normally be held high and two drain caps will be pre-discharged.

What about NOR Gates?

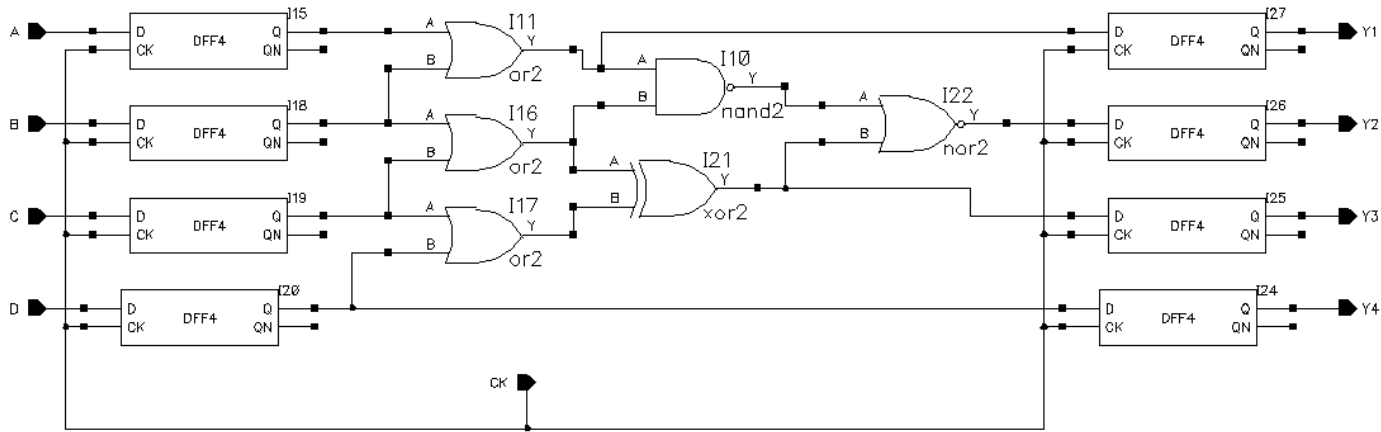
Which will have fastest/slowest fall time?



B will be the fastest because all three nmos will discharge in parallel.

A will be slowest because only one nmos will discharge.

Design a circuit for 200MHz



- Find the number of logic levels of the longest path.
 - Divide the time available (5ns) by number of logic levels.
 - Assume a C_g for the first stage to Drive
 - Calculate W_N/W_P of the next stage use W_N/W_P to calculate C_G and calculate W_N W_P of the next stage.
- Repeat until last state.

Continued

The longest path is: I26(FF-master),I22(NOR), I21(XOR), I17(OR), I20 (FF-slave)

The number of logic levels is 2(FF master)+1(NOR)+2(XOR), 2(OR), 2 (FF-master):

9 levels of logic.

propagation delay=5ns/9

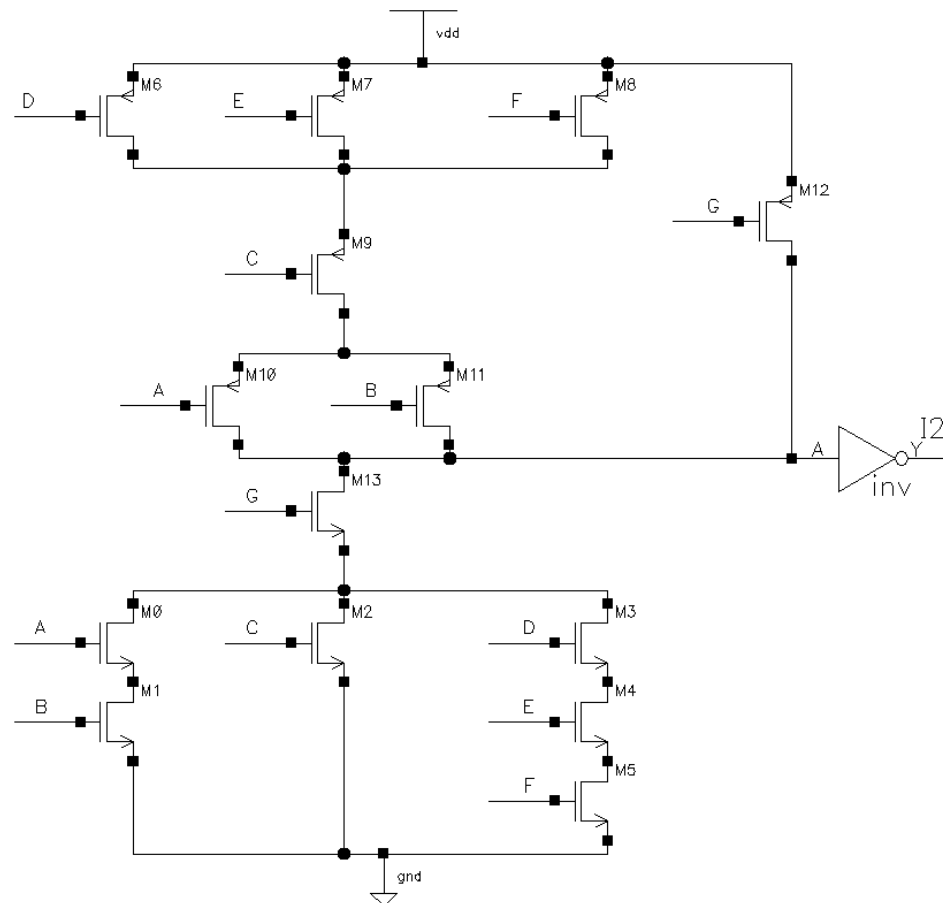
CELL	BIT#	WN Load (cm)	WP Load (cm)	Cint F	Cg or Cin of load F	Cg+Cint	τ_{phl} s	τ_{plh} s	A Ω	S	NSN	NSP	N	M	R	WN cm	WP cm
nor2	1			0.00E+00	2.0000E-14	2.0000E-14	5.56E-10	5.56E-10	1.00E+04	1.0000	1	2	2	3	3.382	3.42E-05	1.16E-04
INV XOR	2	3.42E-05	1.16E-04	0.00E+00	2.5119E-15	2.5119E-15	5.56E-10	5.56E-10	1.00E+04	1.0000	1	1	1	1	1.691	5.43E-06	9.18E-06
XOR AOI	3	5.43E-06	9.18E-06	0.00E+00	2.4513E-16	2.4513E-16	5.56E-10	5.56E-10	1.00E+04	1.0000	2	2	5	5	1.691	4.29E-05	7.26E-05
INV OR	4	4.29E-05	7.26E-05	0.00E+00	3.8757E-15	3.8757E-15	5.56E-10	5.56E-10	1.00E+04	1.0000	1	1	1	1	1.000	6.89E-06	6.89E-06
NOR OR	7	6.89E-06	6.89E-06	0.00E+00	2.3130E-16	2.3130E-16	5.56E-10	5.56E-10	1.00E+04	1.0000	1	2	2	3	3.382	7.93E-06	2.68E-05
FF NAND	3	7.93E-06	2.68E-05	0.00E+00	1.1662E-15	1.1662E-15	5.56E-10	5.56E-10	1.00E+04	1.0000	2	1	3	2	0.846	1.74E-05	1.47E-05
FF MUX	6	1.74E-05	1.47E-05	0.00E+00	5.4022E-16	5.4022E-16	5.56E-10	5.56E-10	1.00E+04	1.0000	2	2	3	3	1.691	2.13E-05	3.60E-05

Today the equations do not matter, this is just a review.

Setup and Hold time

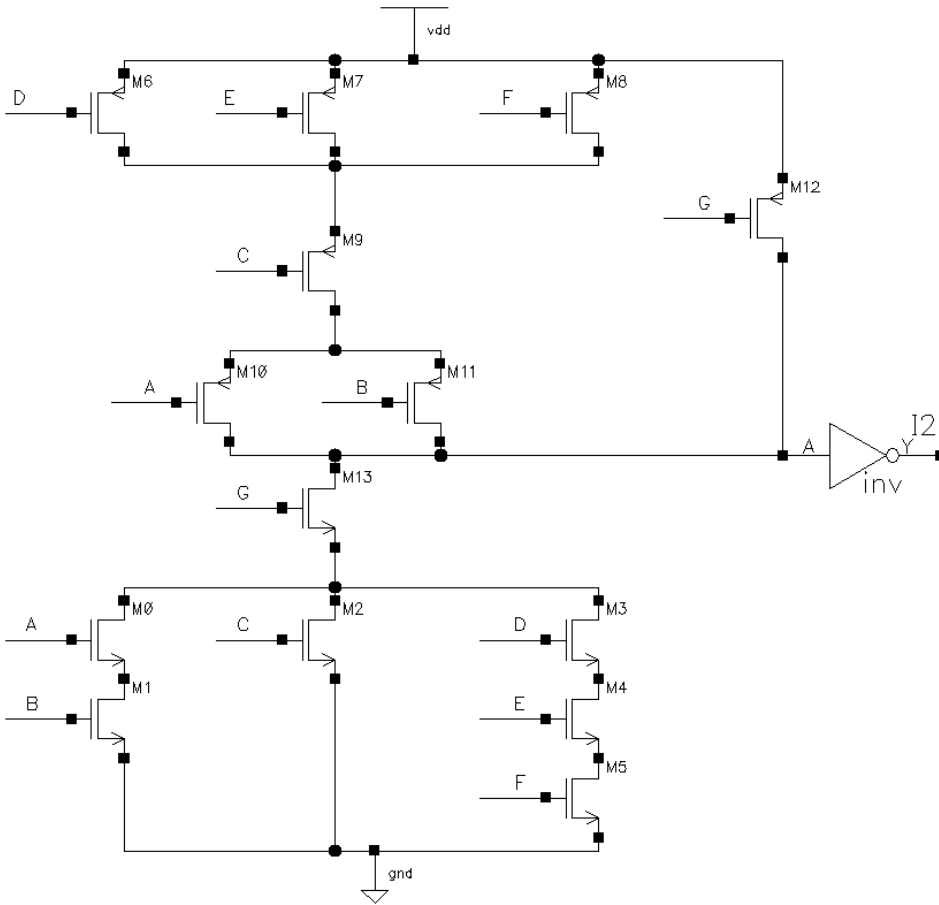
- Setup time is the minimum time that D has to be stable before the triggering edge, and is equal to the transition time of the master D latch.
- Hold time is the minimum time the clock has to remain stable after the triggering edge and is equal to the transition time of the slave D latch.

Minimize for Area and Delay

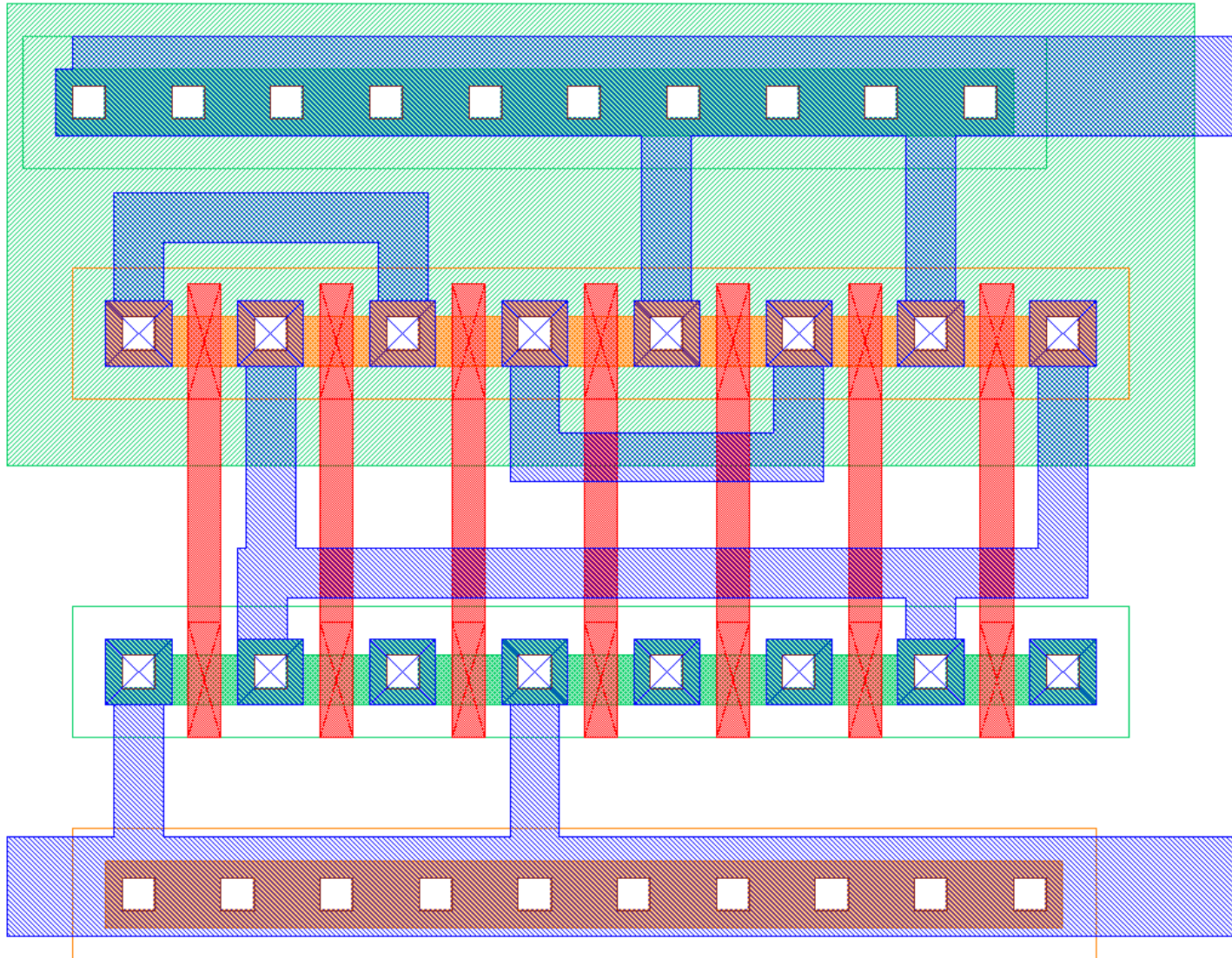


Euler Path

BACFEDG



Layout



Summary

- This quiz/homework was designed to check and see if you should stay in 224 or take 166. There will be no numeric grade, but a:
 - I think you will do fine
 - I think you need 166
- I think SJSU's 166 is one of the best full custom courses, but you do not need it, then do not take it!