

Other Logic Styles

EE224

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Why do we need other logic Styles

- Sometimes you can not meet the timing specification due to the large PMOS parasitic capacitances.
 - Design a 3 input NAND GATE with symmetric propagation delays of 50ps driving a 10fF load in $\frac{1}{4}$ micron technology.

Hand Calculations and Spice

$$A := 11950\Omega$$

$$L_N := .24 \cdot 10^{-4} \text{ cm}$$

$$C_{JSWN} := 4.44 \cdot 10^{-12} \frac{\text{F}}{\text{cm}}$$

$$C_{JN} := 1.92 \cdot 10^{-7} \frac{\text{F}}{\text{cm}^2}$$

$$L_D := .6 \cdot 10^{-4} \text{ cm}$$

$$C_{GDO} := 6.27 \cdot 10^{-12} \frac{\text{F}}{\text{cm}}$$

$$C_g := 10 \cdot 10^{-15} \text{ F}$$

$$K_{EQ} := \frac{-2\sqrt{.99}}{-2.5} \cdot (\sqrt{.99 + 2.5} - \sqrt{.99})$$

$$\tau_{PHL} := .05 \cdot 10^{-9} \text{ s}$$

$$K_{EQ} = 0.695$$

$$R := 2.322$$

$$W_N := \frac{C_g + C_{JSWN} \cdot 4L_D \cdot K_{EQ}}{\frac{\tau_{PHL}}{L_N \cdot A} - (1 + R) \cdot (C_{JSWN} \cdot 2K_{EQ} + C_{JN} \cdot L_D \cdot K_{EQ} + 2 \cdot C_{GDO})}$$

$$W_N = 1.255 \times 10^{-4} \text{ cm}$$

$$W_P := R \cdot W_N \quad W_P = 2.914 \times 10^{-4} \text{ cm}$$

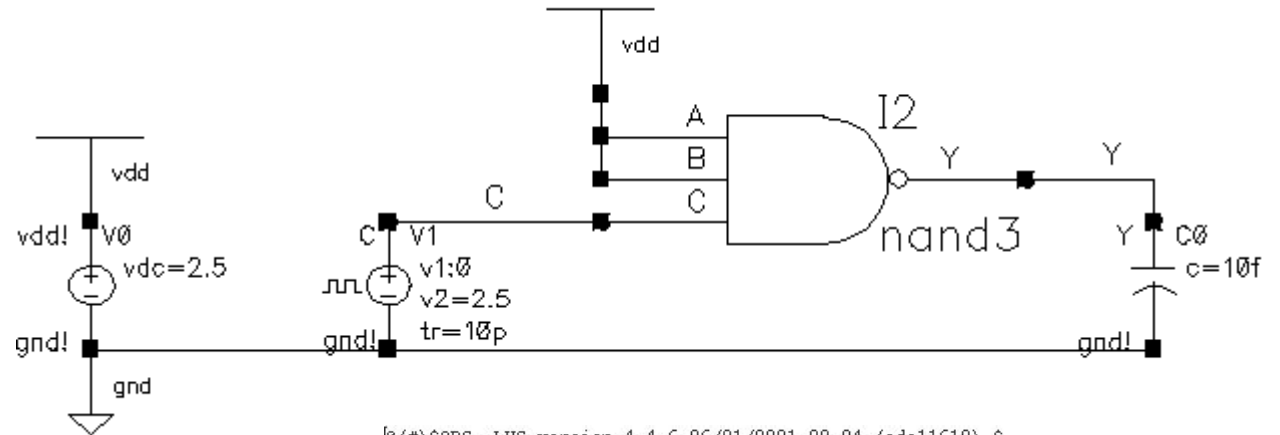
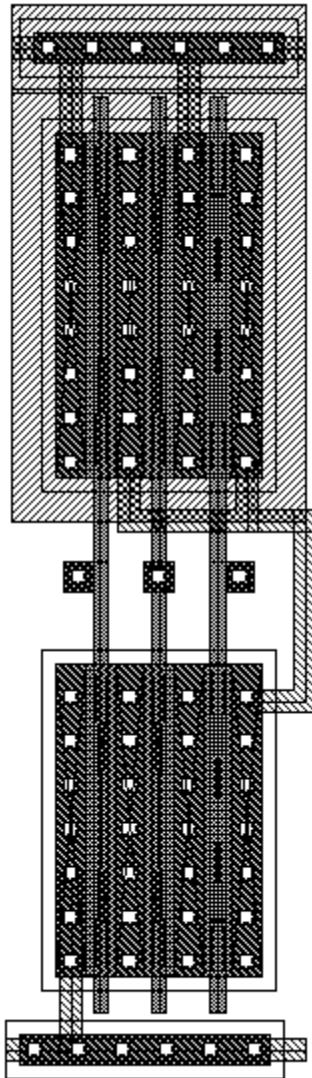
WN	WP	TPHL	TPLH
1.26	2.9	202	97
5.09	5.6	121	127
12	14	118	113

Schematic

We could not meet spec!

I tried to lay it out hoping that the parasitic caps would be lower.

My delay was still ~100ps!



@(#)\$CDS: LVS version 4.4.6 06/01/2001 20:24 (cds11612) \$

Like matching is enabled.
 Net swapping is enabled.
 Using terminal names as correspondence points.
 Compiling Diva LVS rules...

Net-list summary for /staff/dparent/cell/LVS/layout/netlist

count	
8	nets
6	terminals
3	pmos
3	rmos

Net-list summary for /staff/dparent/cell/LVS/schematic/netlist

count	
8	nets
6	terminals
3	pmos
3	rmos

Terminal correspondence points

1	A
2	B
3	C
4	Y
5	gnd!
6	vdd!

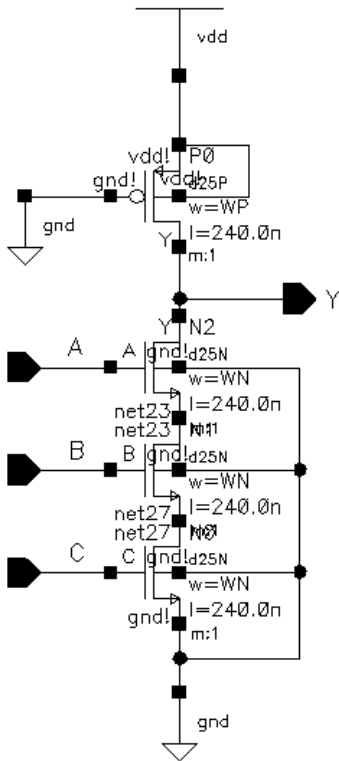
The net-lists match.

Well What Happened?

- If we look at the WN and WP we calculated for the driver and calculated its input capacitance we would find that it is greater than the original load!
 - No Gain at this speed!
 - We should have quit right then.

What about Pseudo-NMOS?

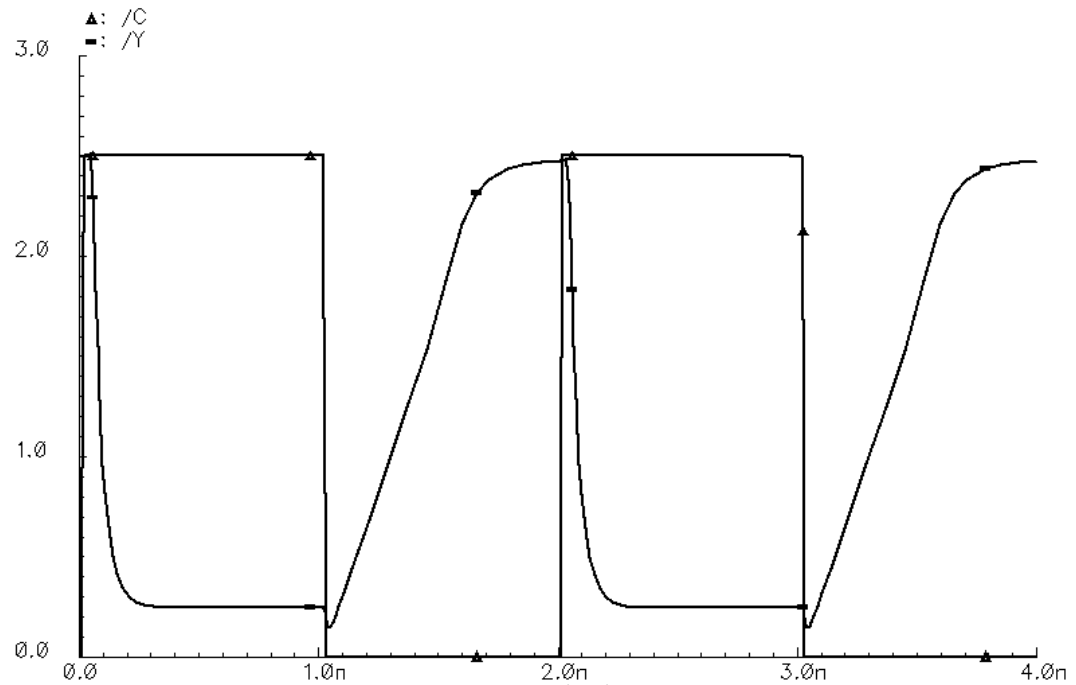
- Replace complimentary PMOS with one PMOS that has its input tied low.



Downside Pseudo-NMOS

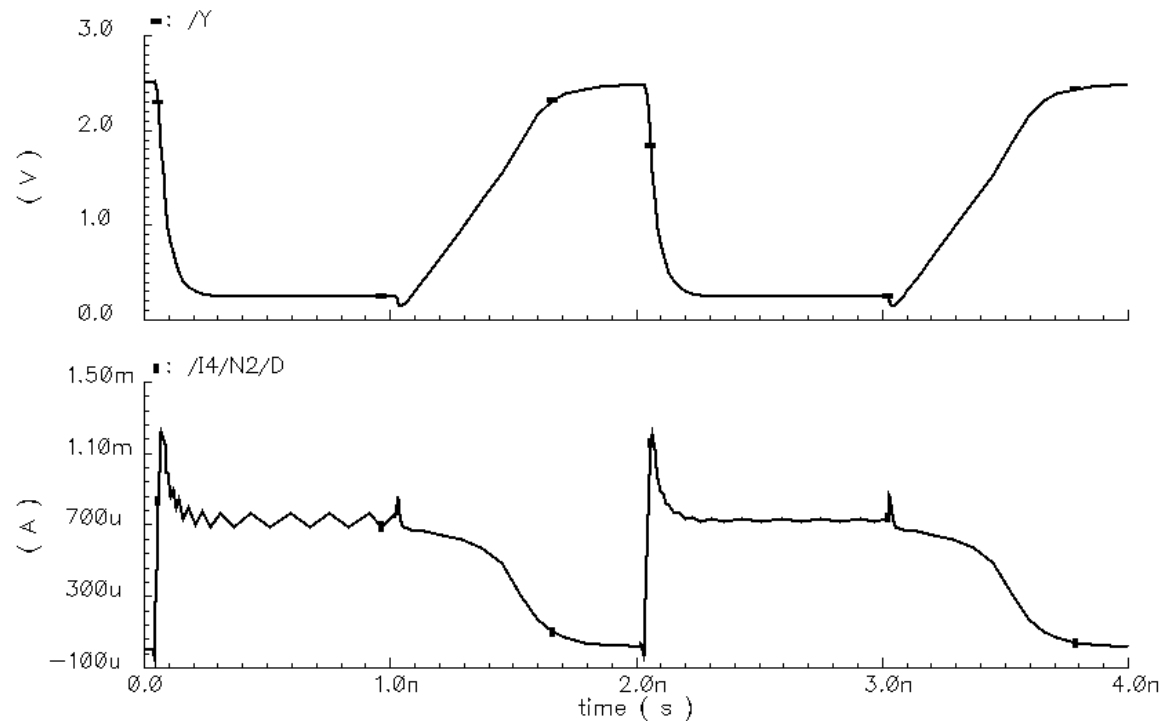
- Replace complimentary PMOS with one PMOS that has its input tied low.

The ratio of
WN/WP determine
VOL



Downside Pseudo-NMOS

Increased power
dissipation!



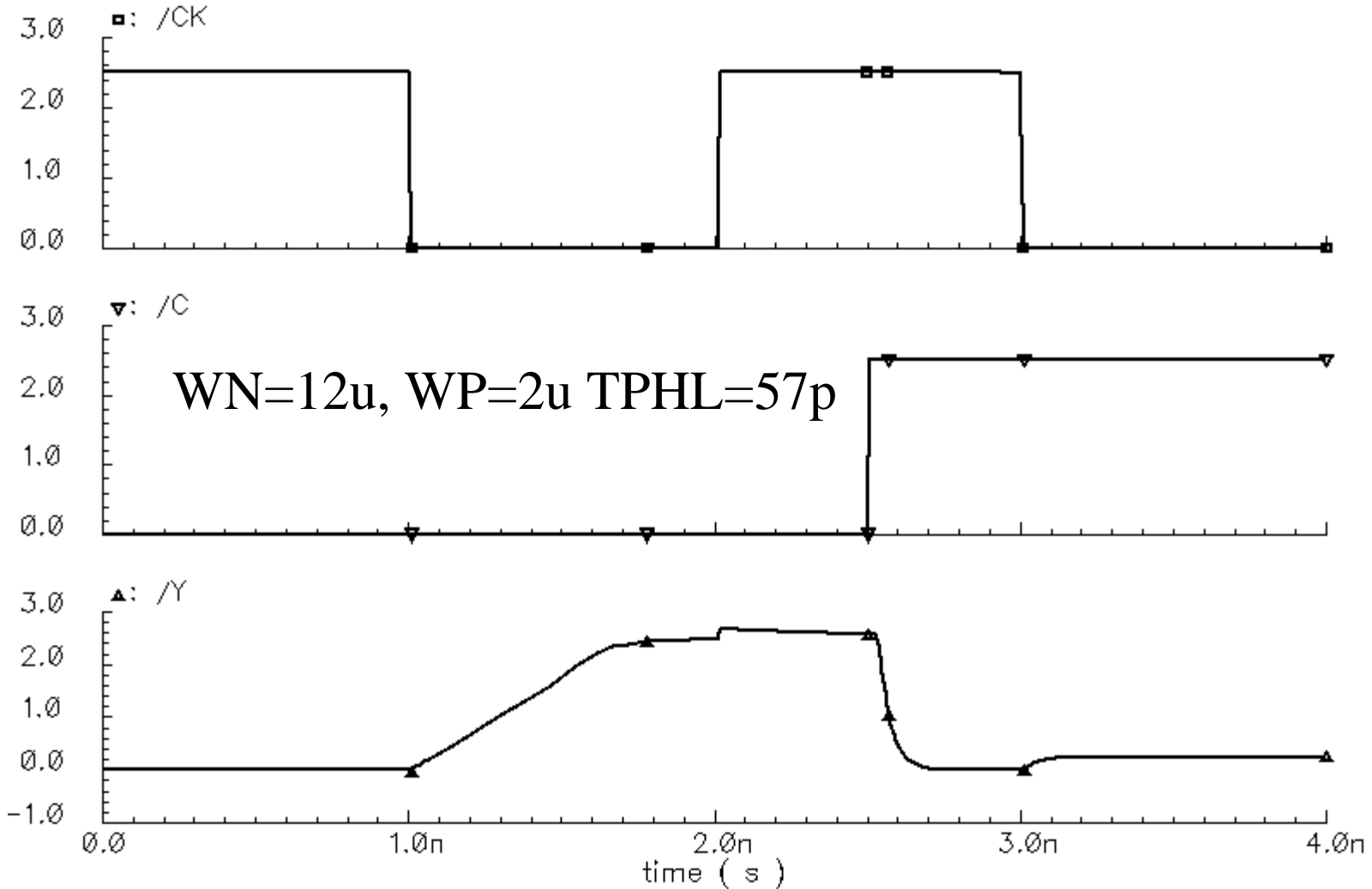
We still could not hit
specification!

Dynamic Logic

- PMOS is tied to a clock or a pre-charged to VDD, and then turned off during an evaluate phase.
 - PMOS turned off so Node is floating until next pre-charge
 - Could Leak presenting a false Zero!

Timing

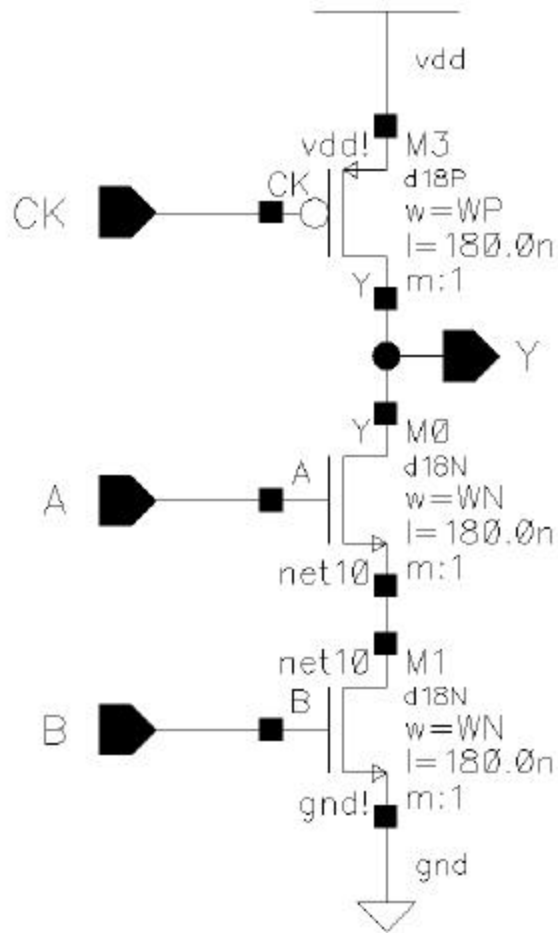
Transient Response



Notes

- footed
- keepers
- nor better than nand
- can't drive another dynamic gate
- domino

Domino Logic with no footer is the fastest since it has less serial nmos.



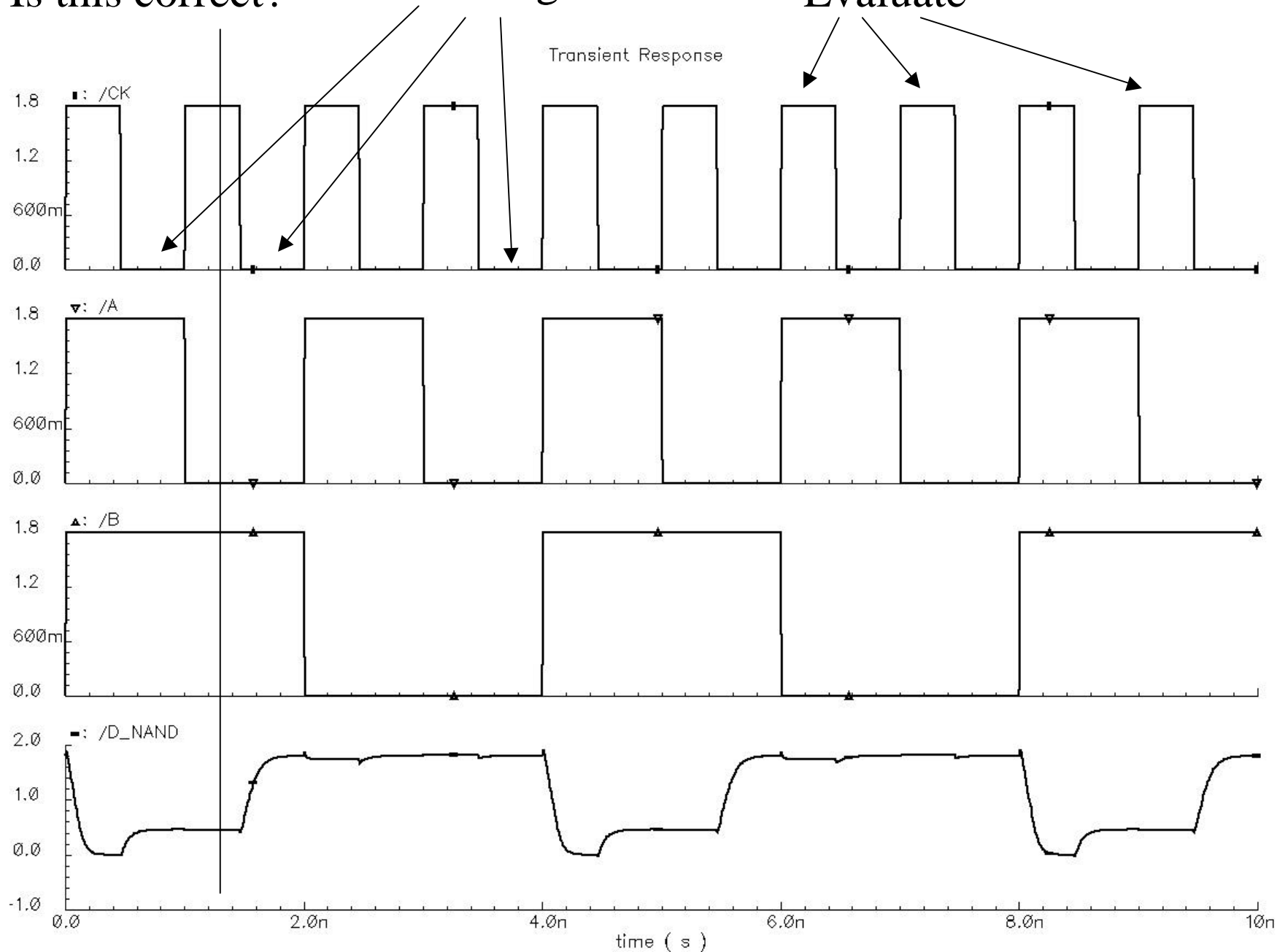
Just like a two input and gate except less pmos drain capacitance

The logic is now only valid during evaluate (When CK is high)

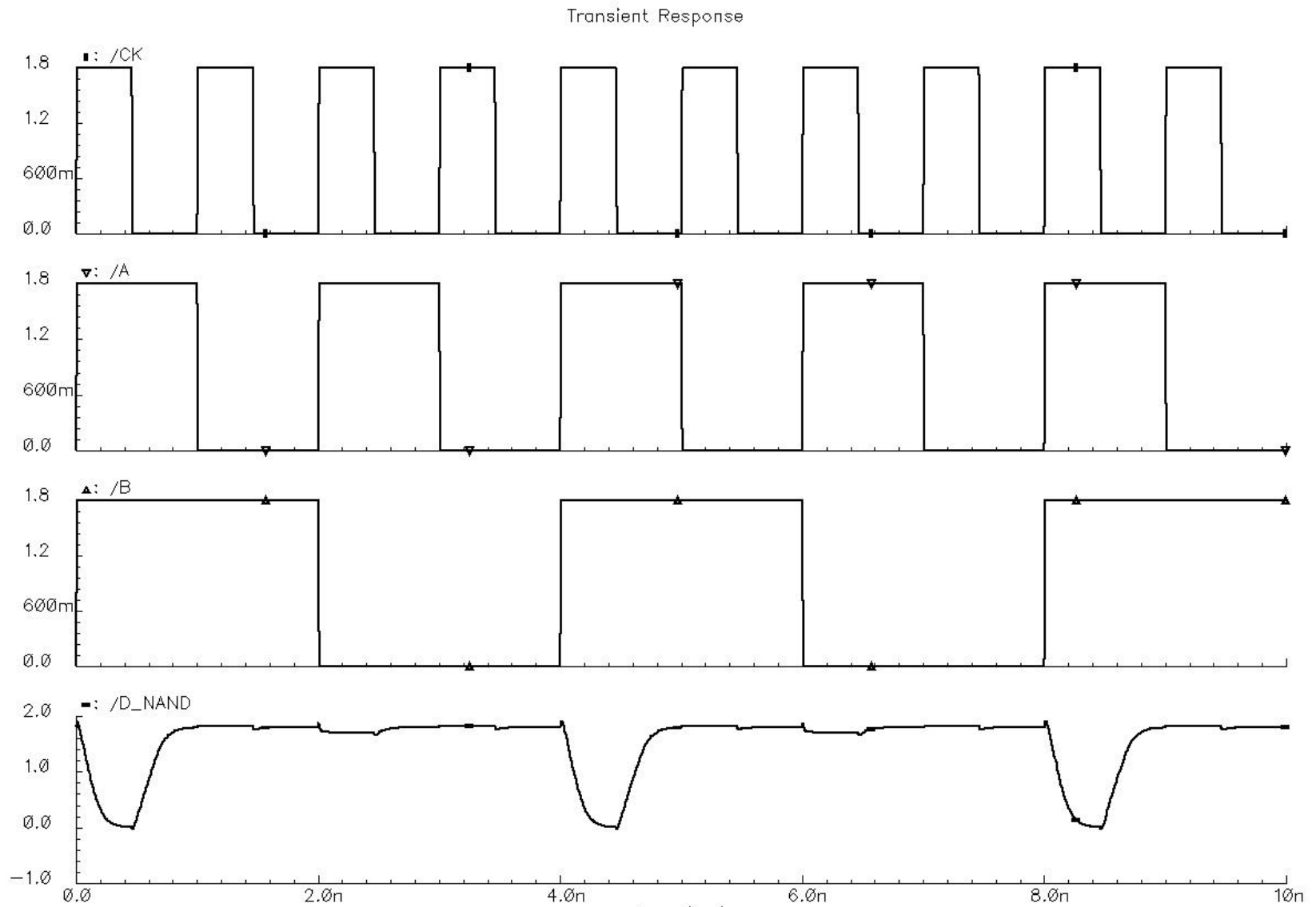
Is this correct?

PreCharge

Evaluate



Logic is valid for evaluate.



Conventional wisdom is that dynamic logic burns more power.

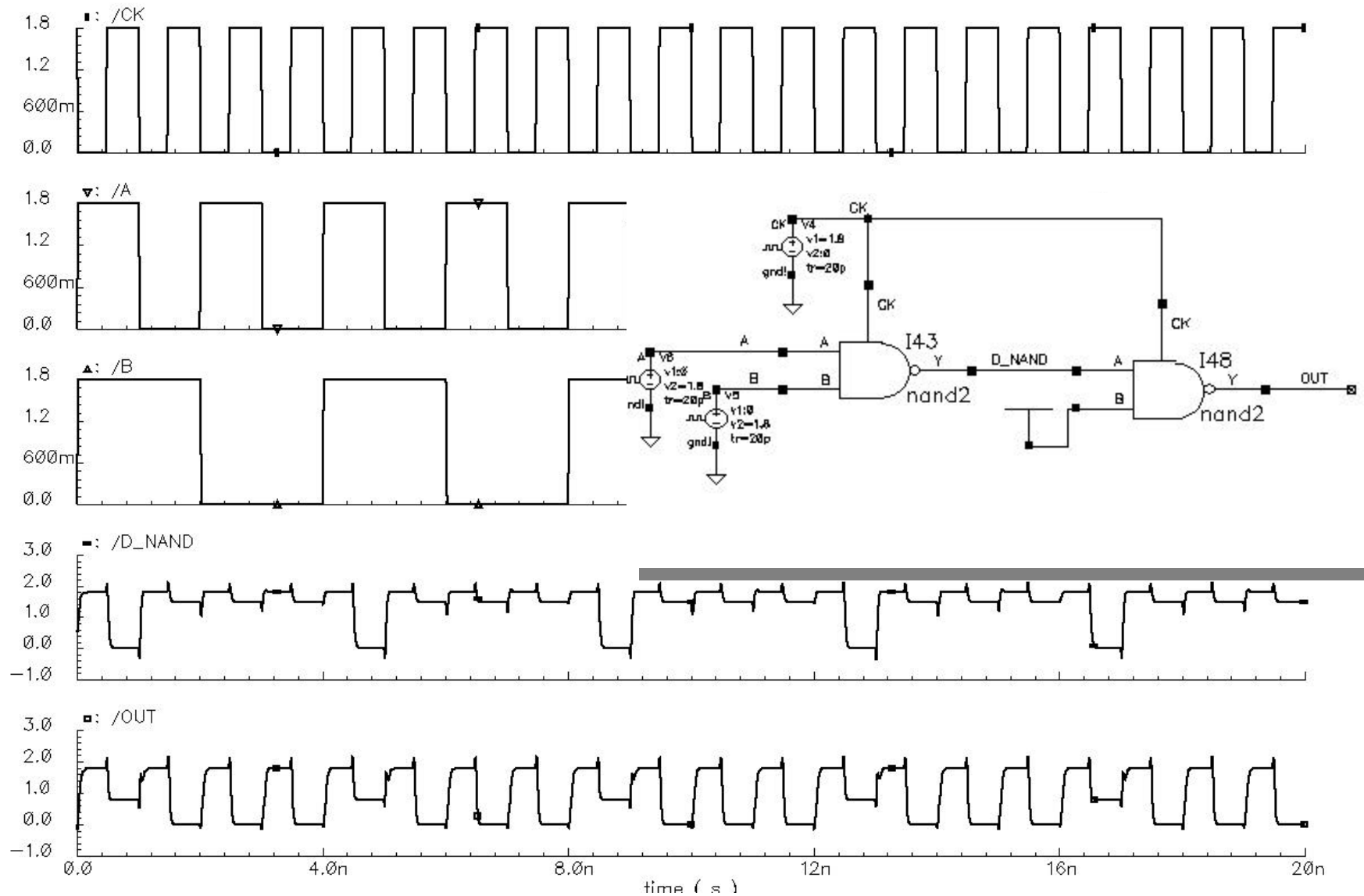
Well sure if f goes up power should go up! $P = aC_{load}fV_{dd}^2$

Clload does go down because there are less pmos drain caps.
(AOI222?)

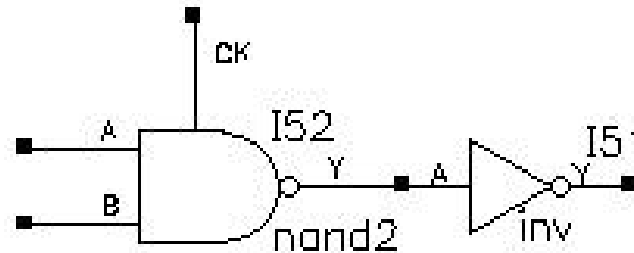
Since there is less CLOAD the widths do not have to be as big to meet timing specifications. Less means less Clload.

Non-footed logic burns more power because there can be a contention state.

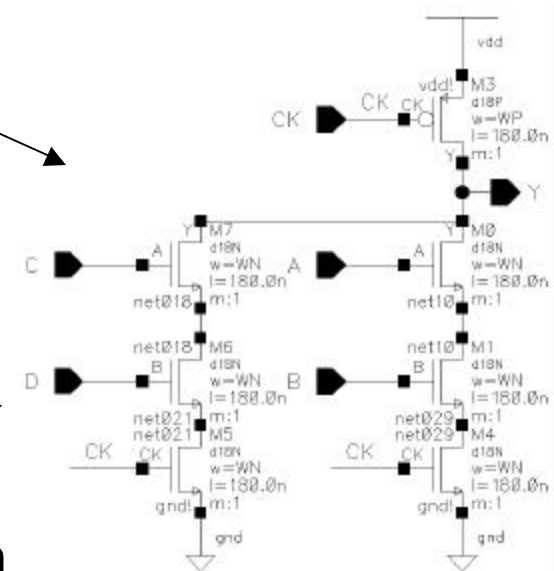
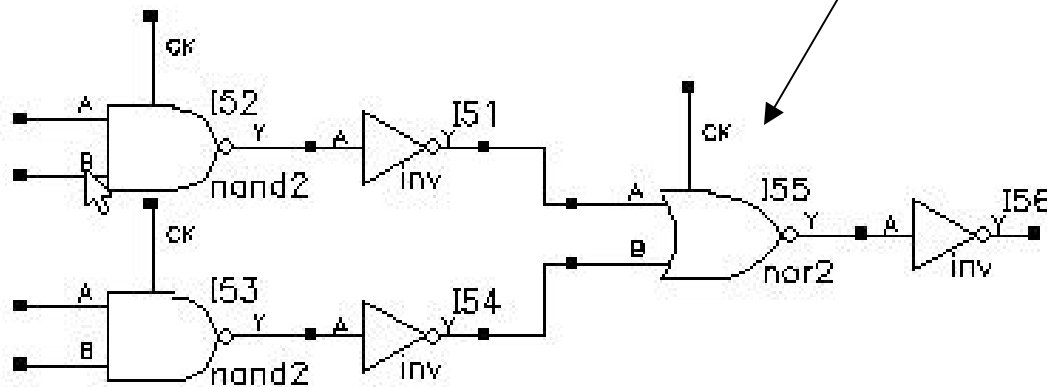
Can a Dynamic Gate Drive another Dynamic gate?



Add inverters to all gates so during pre charge all inputs to nmos are 0..

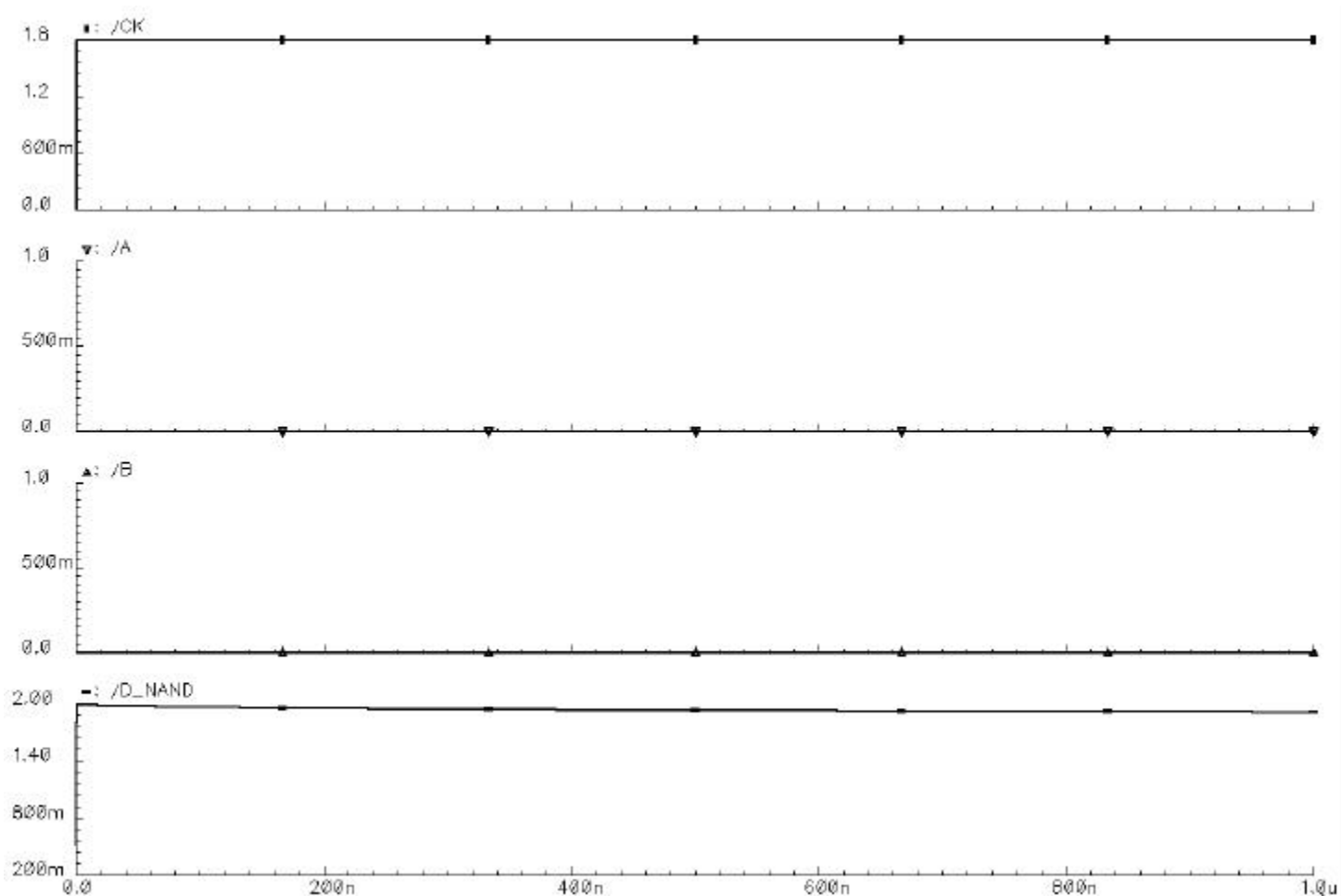


No more inverting logic! $f=ab+cd$



inv not shown.

Static testing is no longer possible because the states are only stored on a capacitance. All state info is wiped on upon Pre-Charge.

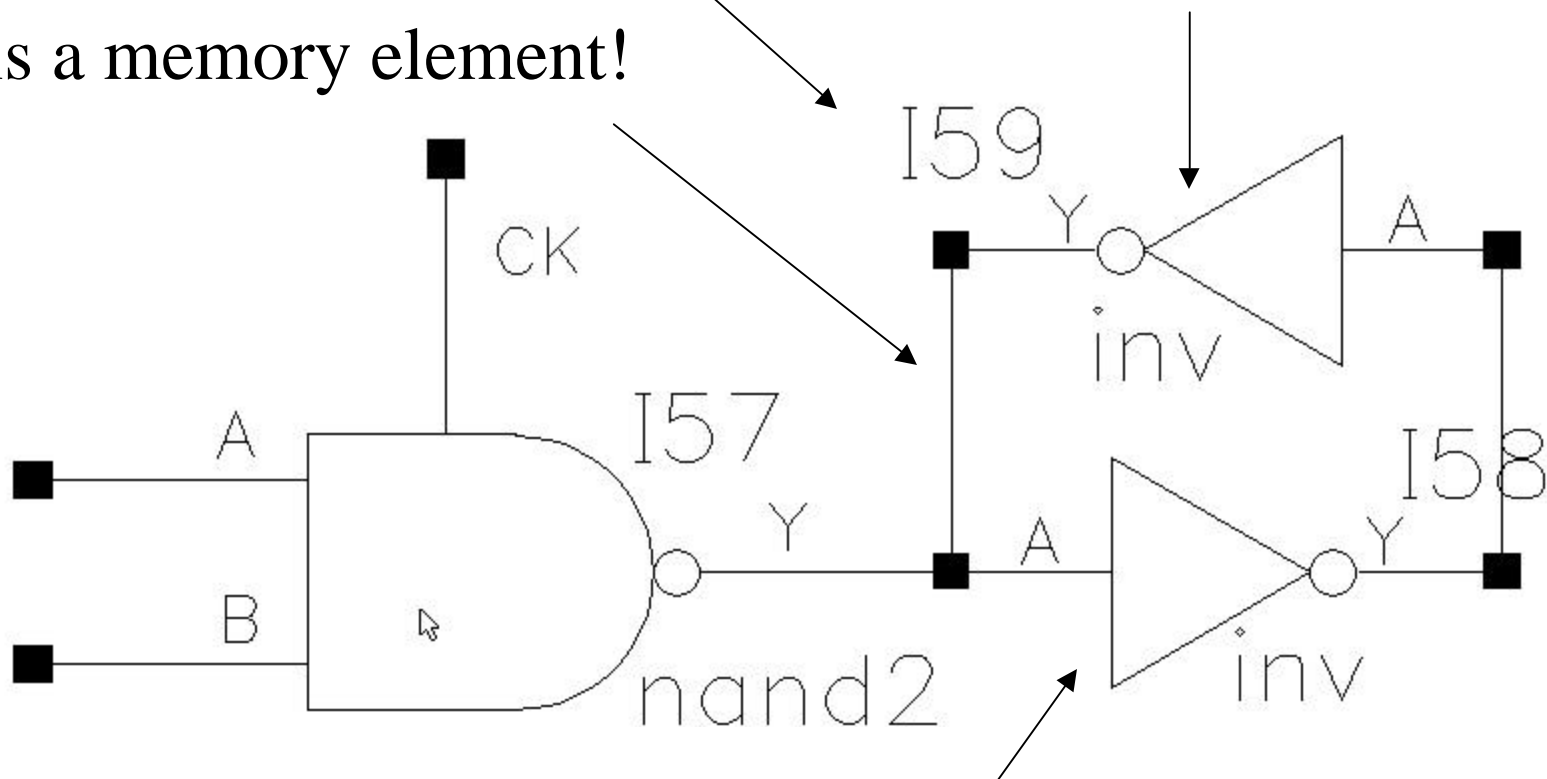


It does seem to hold for at least 1us!

Adding weak keepers can help hold values and protect against other issues

Minimum sized

This is a memory element!



Much stronger than keeper

Summary

- Non footed dynamic is the fastest, but hardest to design
- Dynamic with weak keepers is the most robust, but is slower than non- footed dynamic.
- Dynamic is harder to test when the circuit comes back. (No IDQQ test.)