

EE 224 What Should You know?

- I would like you to be a successful member of an IC design team (even with lousy support).
 - I want you to be able to pass the interview
 - See questions
 - Solid state physics (So that as technology changes, you can keep up.)
 - body effect, velocity saturation, capacitances, modes (sat and linear, cutoff) leakage (QM tunneling)
 - Model the delay of a new process

EE 224 What Should You know?

- Choose a sequencing methodology
 - Flip Flops, latches, pulsed latches
- Choose a logic style
 - Static, Dynamic, Pseudo-nmos, Pass Gate
- Choose/Understand an Architecture
 - adders (ripple, CLA, trees), multipliers, shifters, encoders etc)
 - LOGICAL EFFORT!
- Understand the relevant issues of
 - SRAM
 - Pads/ IO/ Latch-up

EE 224 What Should You know?

- Design a Static or Dynamic circuit
- Understand the noise (v_{in} vs v_{out}) of a circuit
- Know which pins to put the slow/fast early/late signals on
- Need to know about wire capacitance

Review

- Describe the operation of a transistor? What a transistor looks like when it is saturated? What a transistor looks like when it is in linear region?

Review

- List all parametric cap. and resistance for a single transistor and weight their relative value. If there is a multiple metal layer process, weight their relative resistance values for different metal layer.

Review

- Assume a 2-input dynamic NAND gate.
 - Describe how the circuit looks like and works (assume the input devices are nfets)? (Assume the clock is 50% duty cycle).
 - Assume the upper input is A and the lower one is B. Also assume the Cap. load of the NAND is 50fF and the cap. between the A & B input nfets is 25fF.
 - If input A is 1 and input B is 0, what will happen? What % of charge will be in CL? Do the same calculation with the cap. between those two input is 10fF?
If input A has equal probability to become 1 or 0, what would be the probability of the output having the charge sharing problem?

Review

- Assume the drain of a nfet connect V_{dd} and the source of the nfet connect to a very big resistor. The gate of the nfet in the input of the circuit. The output of the circuit is the node between the transistor and the resistor. If the input is 1, what is the output voltage? If the input is 0, what is the output voltage? What is the function of the circuit? Would you recommend me to use this circuit in my design? why?

Review

- Lets assume a simple CMOS inverter. If we connect the input and output together, what would be the input/output value? Please explain it in term of feedback theory. Assume a 2-input NOR gate, if we can only have one input pin and the other pin must connect to V_{dd} or ground, what should we do to make a equivalent inverter and how would you sized them?

Review

- Design a circuit that can vary the frequency of a clock signal? For example, the input of the circuit is a clock signal with period of 1ns and the output of the circuit is a clock signal with period of 0.5ns. You can use FF and any kind of logic gate as you want.

Review

- Assume there two input signals and one control signal. Design a circuit that when the control signal is 1, the output become input A and when the control signal is 0, the output become input B. Describe the circuit you design (you can use any kind of logic family but at transistor level). Describe the good and bad thing about your design. Do the same design at gate level and compare your gate level design and transistor level design.

Review

- What is short-channel effect and describe it?
- What is pipeline hazard?
- What is the setup and hold time requirement for a FF?
- What is virtual memory?
 - How much you know about Unix OS and VHDL?

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Sample intel interview questions.

1. Draw basic PLL block diagram and explain each block.
2. Explain current mirror. What is transistor matching? Why is it so important in current mirrors?
3. Explain charge sharing.
4. Describe the operation of a transistor? What a transistor looks like when it is saturated? What a transistor looks like when it is in linear region?
5. Draw the Cross section of MOSFET and explain the characteristics using Band diagram and I-V characteristics.
6. What is short-channel effect and describe it?
7. I swapped 2 transistors in CMOS inverter (put n-transistor at the top and p-transistor at the bottom). Can this circuit work as a noninverting buffer?
8. Draw V_{ds} - I_{ds} curve for a MOSFET. Now, show how this curve changes (a) with increasing V_{gs} (b) with increasing transistor width (c) considering Channel Length Modulation
9. What is Body Effect?
10. Draw the stick diagram of a NOR gate. Optimize it