

Question 1 (10pts):

In Figure 1, we see identical NAND3 gates wired. The NAND3 schematic can be seen in Figure 2. Which setup gives the smallest V_{TH} ? Which setup gives the largest V_{TH} ? Explain your answers for full credit.

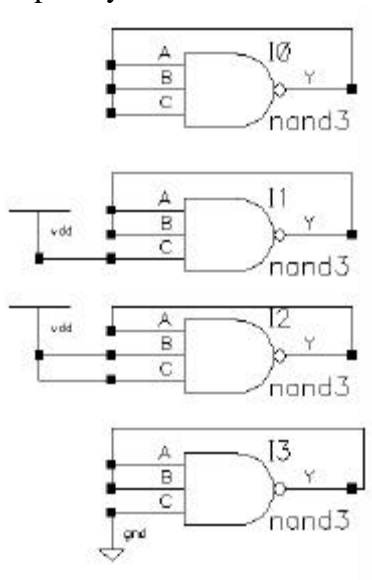


Figure 1: NAND3 Gate V_{TH} test bench.

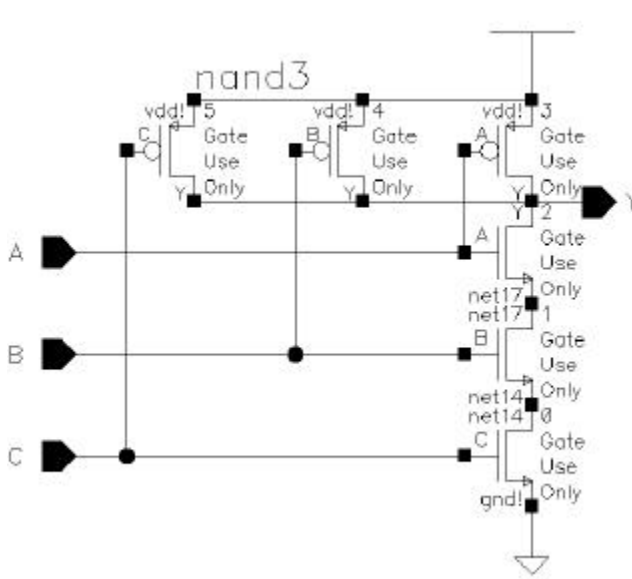


Figure 2: NOR Schematic.

Question 2(10pts):

Using Figure 3, explain why we can use a plot of DC V_{out} vs. V_{in} to explain noise margins, and switching points.

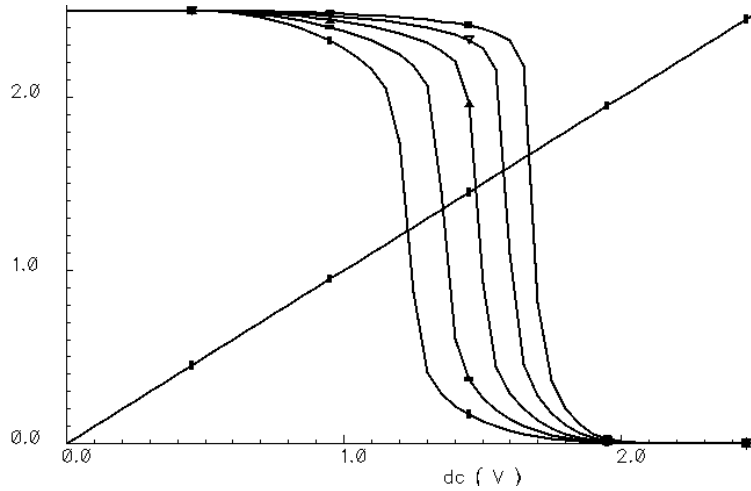


Figure 3: DC response of an inverter with WN held constant and W_P varied from $0.5\mu\text{m}$ to $10\mu\text{m}$.

Question 3 (10pts):

In Figure 4, we see a sample function implemented in domino logic. Assume that the WP and WN for all the gates have been sized properly to work at the target frequency

Draw the waveforms during pre-charge and evaluate for the nodes, G, P and SUM. Assume that the input A stays low and that B and CIN go from low to high after the clock enters into evaluate.

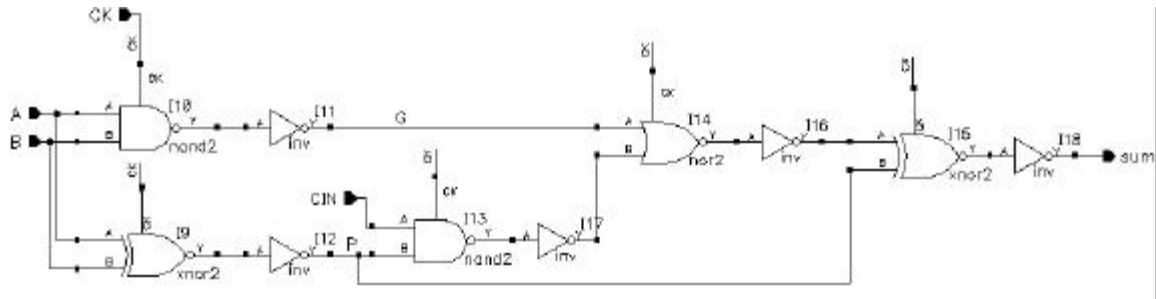


Figure 4: Sample Domino Logic Function.

Question 4 (10 pts):

In Figure 5, we see the same logic function implemented in domino logic.

Create a test bench that will show the worst-case delay for the evaluate logic.

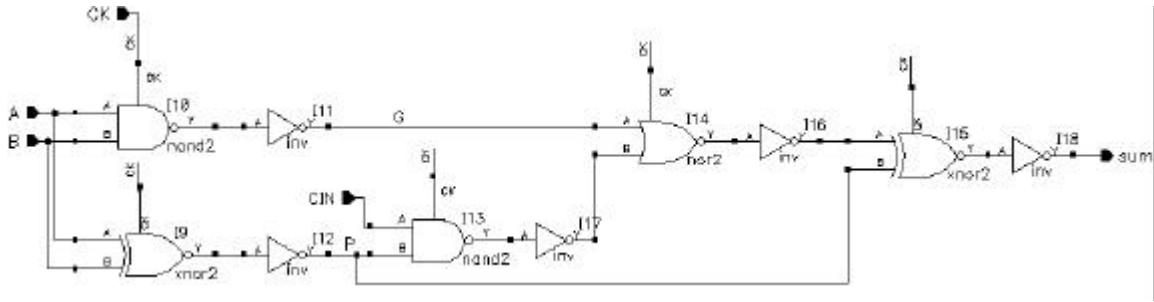


Figure 5: Another function implemented in domino logic.

Question 5(10pts):

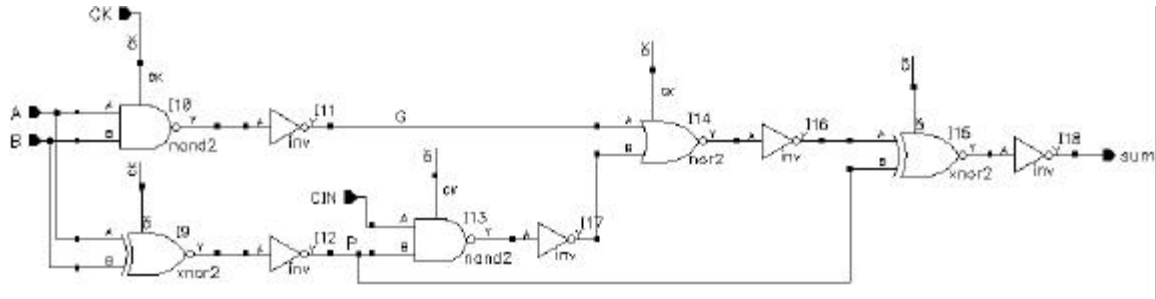
- Using Figure 5, from the previous question write out which transitions sum up to the evaluate time and which transitions sum up to the precharge time.
- Assign a reasonable precharge and evaluate ratio to make the circuit work at period of T.

Question 6(10pts):

You are to design a circuit to implement the function $f=ab+cd$. You have determined from hand calculations that a static cmos implementation will not meet your timing specification. Propose three different ways to do this in Domino/Dynamic logic. Assume that you do not need weak keepers or feet. Evaluate, using logical effort which method is fastest, given that H is somewhere between 2 and 4.

Question 7(10pts):

For each dynamic gate in the figure below decide whether it should be footed or non-footed, with weak keeper or without. Explain for full credit. State your assumptions about when the CK and data arrive.



Question 8(10pts):

Design a test bench to measure the worst case propagation delay of an AOI4321 static CMOS circuit.

Question 9(10pts):

What are LVS and DRC and why are they used?

Question 10 (10pts):

Why can't a dynamic gate drive a n other dynamic gate?

Why/when do we use a foot in dynamic logic?

How much faster is a footed domino NAND3 gate than a non-footed domino gate. Use logic effort.