NAME:

Question 1 (10pts):

In Figure 1, we see identical NOR gates wired up to measure V_{TH}. The NOR schematic can be seen in Figure 2. Which set up gives the smallest V_{TH}? Which setup gives the largest V_{TH}? Explain your answers for full credit.

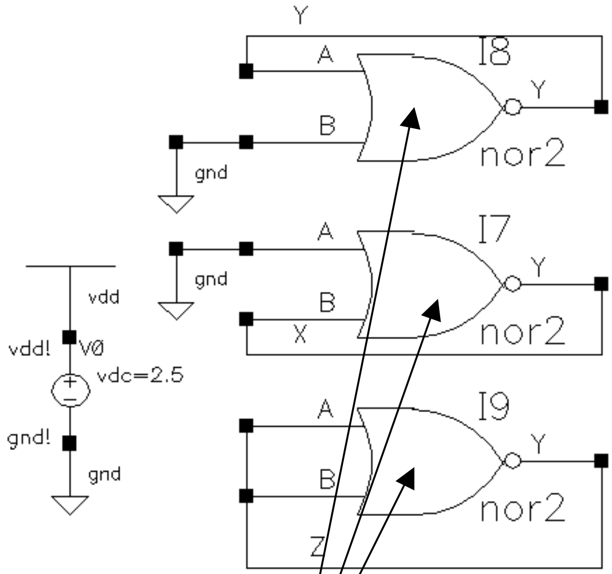


Figure 1: NOR Gate V_{TH} test bench.

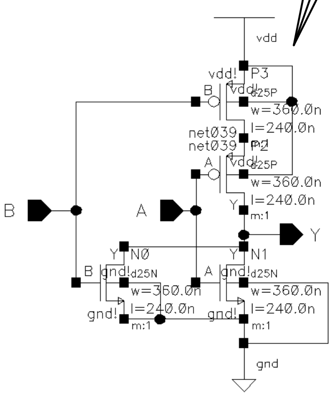


Figure 2: NOR Schematic.

I9 has the lowest VTH because both nmos are pulling in parallel. This means more voltage has to fall across the pmos chain to get the currents to balance. The vgs of the pmos and the vgs of the nmos have to sum to vdd.

The largest VTH will be the circuit that has the least amount of vgs falling across the pmos transistors. Since the magnitude of the VT of the A PMOS is larger, than the B pmos due to the body effect, I7 will need less voltage to balance the currents, and thus VTH will be the largest.

This has nothing to do with switching or capacitance.

Question 2(40pts):

In Figure 3, we see the DC response of an inverter that has WN held constant and WP is varied from .5um to 10um. Explain all answers for full credit. (Label the curves from left to right 1,2,3,4,5.)

- Which curve has the largest WP value? **5, because the larger WP the more voltage has to fall across the nmos to have the currents balance.**

- Which curve has the lowest WP value? **1, because the smaller WP the more voltage has to fall across the pmos to have the currents balance.**

- Which curve represents the WP/WN ratio that gives the best noise immunity against a noisy ground signal? **5, because a low signal can vary up to around 1.7 volts before changing the output state.**

- Which curve represents the WP/WN ratio that gives the best noise immunity against a VDD signal? **1, because a high signal can vary down to around 1.5 volts before changing the output state.**

- Which curve represents the WP/WN ratio that would give a propagation delay low to hi, much smaller than a propagation delay high to low. **5 because WP>WN.**

- Which curve represents the WP/WN ratio that you would use to prevent a false change of state in a domino logic gate due to a leaking dynamic gate's node voltage during the evaluate cycle? **1, because a high signal can vary down to around 1.5 volts before changing the output state.**

- Which curve represents the WP/WN ratio that you would use to prevent a false change of state in a domino logic gate due to charge sharing on the dynamic gate's node voltage during the evaluate cycle? **1, because a high signal can vary down to around 1.5 volts before changing the output state.**

- Which curve has the most even noise immunities? **Curve 1 since it is closest to VDD/2**

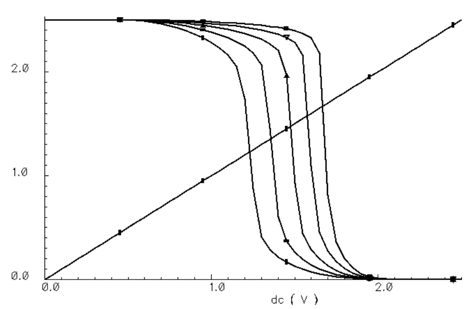


Figure 3: DC response of an inverter with WN held constant and WP varied from .5um to 10um.

Question 3 (10pts):

In Figure 4, we see a sample function implemented in domino logic. Assume that the WP and WN for all the gates have been sized properly to work at 500MHz with the evaluate and precharge times having a ratio of 2:1.

Draw the waveforms during precharge and evaluate for the nodes, Y, YBAR, f1, f1bar, f2, and f2bar. Assume that the input at A changes from low to high after the CK goes high.

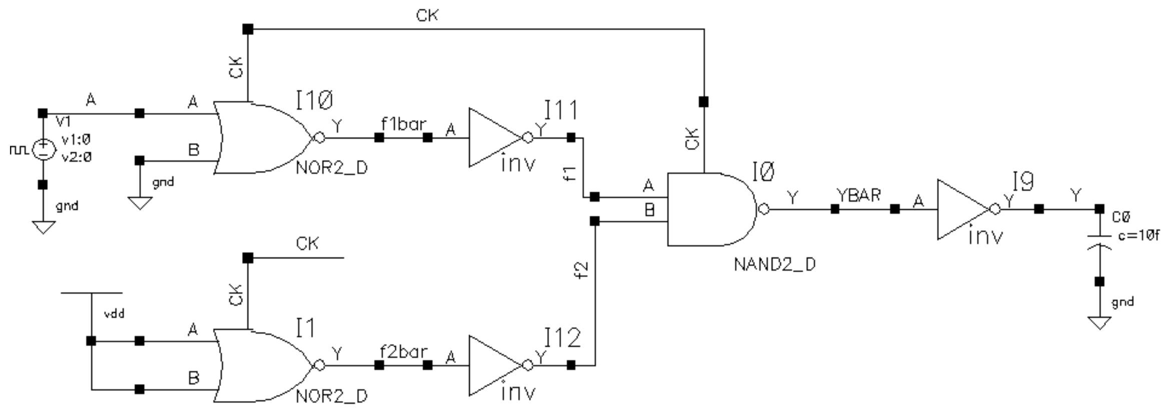
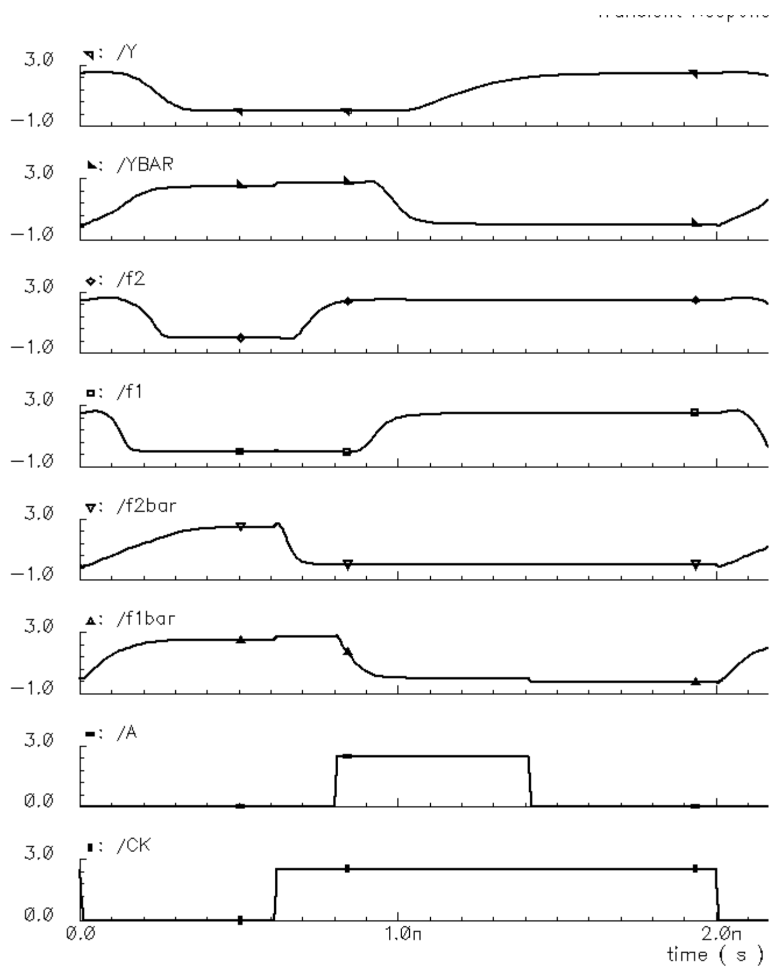


Figure 4: Sample Domino Logic Function.



The important part of these waveforms are:

- CK is low for less time than the clock is high
- f1,f2, and Y go low and f1b, f2b, and yb go high during precharge is parallel
- f2bar should go low before f1bar (and thus f2 should lead f1) because the inputs on f2bar are already high while we waited for A on f1 to rise at least with the clock edge during evalaute.
- y should be the lst signal to go high during evaluate.
- Notice that when A goes back down, f1bar does not go back up!

Question 4 (10 pts):

In Figure 5, we see another logic function implemented in domino logic.

Create a test bench that will show the worst-case delay for the evaluate logic.
(Pick A, B, and C to be high or low before the clock goes high.)

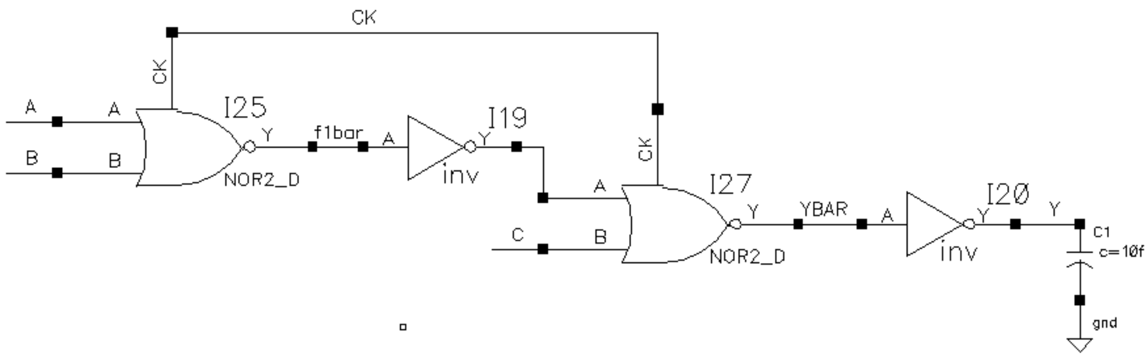


Figure 5: Another function implemented in domino logic.

Set A high, and B and C low. This will cause the circuit to evaluate through the whole chain. C high would cause Ybar to discharge earlier. Both A and B high would cause I25 to discharge faster than just one input going high.

Question 5(10pts):

- Using Figure 5, from the previous question write out which transitions sum up to the evaluate time and which transitions sum up to the precharge time.
- Assign a reasonable precharge and evaluate ratio to make the circuit work at 1GHz.

Teval=tphl_I25+tplh_I19+ tphl_I27+tplh_I20
Tpre= tplh_I25+tphl_I19= tplh_I27+tphl_I20

Any reasonable Teval>tpre would have sufficed.

Question 6(10pts):

In Figure 6, we see two ways of calculating a 6 input NAND function. Using the method of logical effort, find the implementation that produces the minimum delay. Assume that the Cin is 8 for both structures.

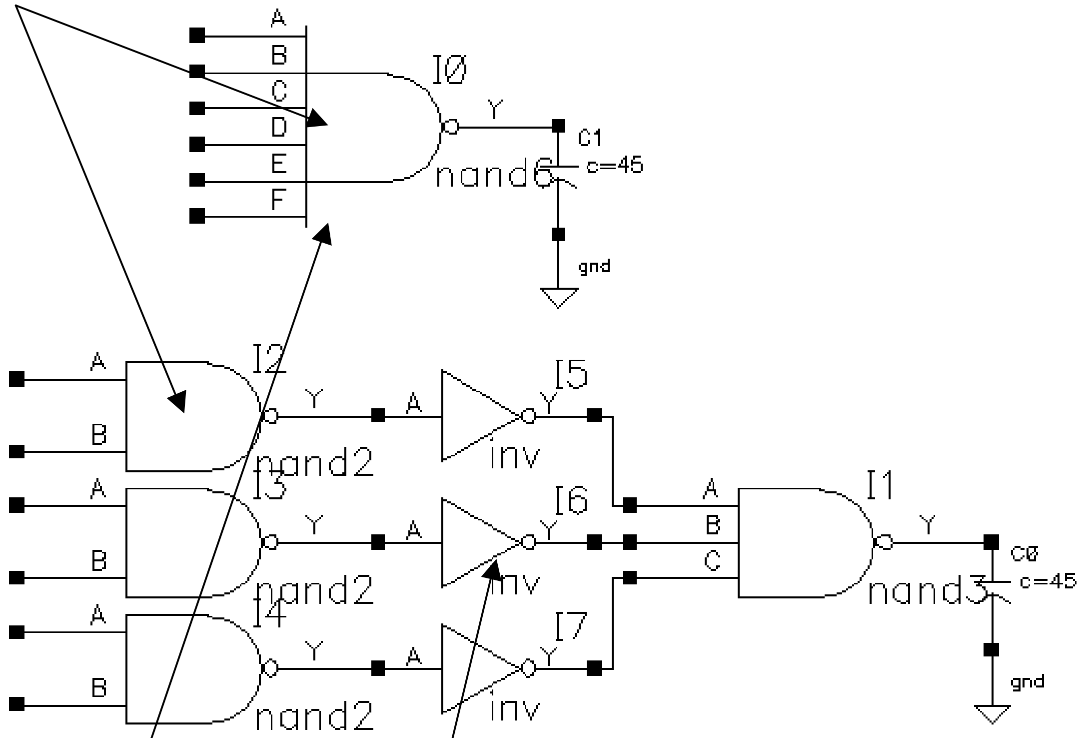


Figure 6: Equivalent Logic functions.

$C_{IN} := 8$

$C_{OUT} := 45$

$F := \frac{8}{3} \cdot 1 \cdot \frac{C_{OUT}}{C_{IN}}$ $F = 15$

$P := 6$

$N := 1$

$D := N \cdot F^{\frac{1}{N}} + P$ $D = 21$

$N := 3$

$F := \frac{4}{3} \cdot 1 \cdot \frac{5}{3} \cdot 1 \cdot \frac{C_{OUT}}{C_{IN}}$

$P := 3 + 1 + 2$

$D := N \cdot F^{\frac{1}{N}} + P$ $D = 12.962$

Figure 6 has the min delay.

Question 7(10pts):

We used the equation below to calculate WP and WP for a given Cg and propagation delay.

What does it mean when you calculate a negative WN? How do you fix it?

$$W_N = \frac{C_g + C_{int} + C_{JSWN} \cdot 2 \cdot D_{Drain} \cdot (N + M)}{\frac{\tau_{PHL}}{N_{SN} \cdot L_N \cdot A} - (N + M \cdot R) \cdot \left(C_{JSWN} \cdot 2 + C_{JN} \cdot D_{Drain}\right)}$$

$$W_P = R \cdot W_N \qquad R = \frac{S \cdot R \cdot N_{SP}}{N_{SN}}$$

N is the number of NMOS drain capacitances in the complex gate.

M is the number of PMOS drain capacitances in the complex gate.

If WN is negative then there is a no real WN that will allow you to meet the prop delay spec (for any Cg). What is happening is that the parasitic capacitance limits the ultimate speed of the circuit. Changing Cg will not help! The only thing that you can do is increase the propagation delay or choose a circuit configuration with lower N,M, and R values. One could switch to a faster technology, but usually you cannot do this. The only practical thing is to increase the delay and borrow time from a circuit with a lower parasitic capacitance value.