NAME:

Question 1 (10pts):

In Figure 1, we see identical NOR gates wired up to measure V_{TH}. The NOR schematic can be seen in Figure 2. Which set up gives the smallest V_{TH}? Which setup gives the largest V_{TH}? Explain your answers for full credit.

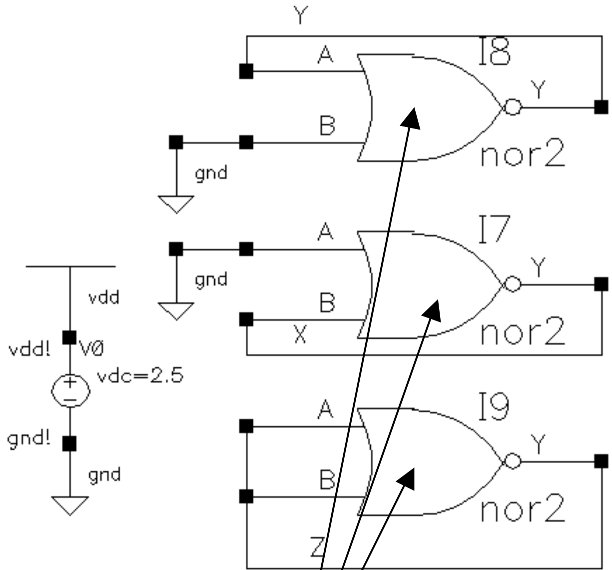

Figure 1: NOR Gate V_{TH} test bench.

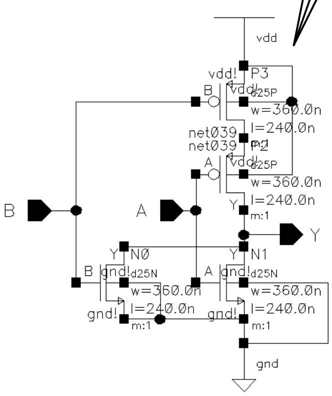

Figure 2: NOR Schematic.

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Question 2(40pts):

In Figure 3, we see the DC response of an inverter that has WN held constant and WP is varied from .5um to 10um. Explain all answers for full credit. (Label the curves from left to right 1,2,3,4,5.)

- Which curve has the largest WP value?

- Which curve has the lowest WP value?

- Which curve represents the WP/WN ratio that gives the best noise immunity against a noisy ground signal?

- Which curve represents the WP/WN ratio that gives the best noise immunity against a VDD signal?

- Which curve represents the WP/WN ratio that would give a propagation delay low to hi, much smaller than a propagation delay high to low.

- Which curve represents the WP/WN ratio that you would use to prevent a false change of state in a domino logic gate due to a leaking dynamic gate's node voltage during the evaluate cycle?

- Which curve represents the WP/WN ratio that you would use to prevent a false change of state in a domino logic gate due to charge sharing on the dynamic gate's node voltage during the evaluate cycle?

- Which curve has the most even noise immunities?

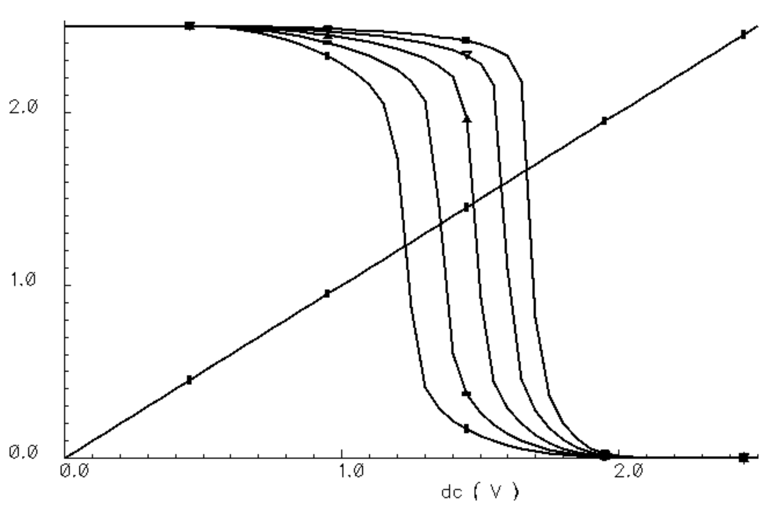

Figure 3: DC response of an inverter with WN held constant and WP varied from .5um to 10um.

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Question 3 (10pts):

In Figure 4, we see a sample function implemented in domino logic. Assume that the WP and WN for all the gates have been sized properly to work at 500MHz with the evaluate and precharge times having a ratio of 2:1.

Draw the waveforms during precharge and evaluate for the nodes, Y, YBAR, f1, f1bar, f2, and f2bar. Assume that the input at A changes from low to high after the CK goes high.

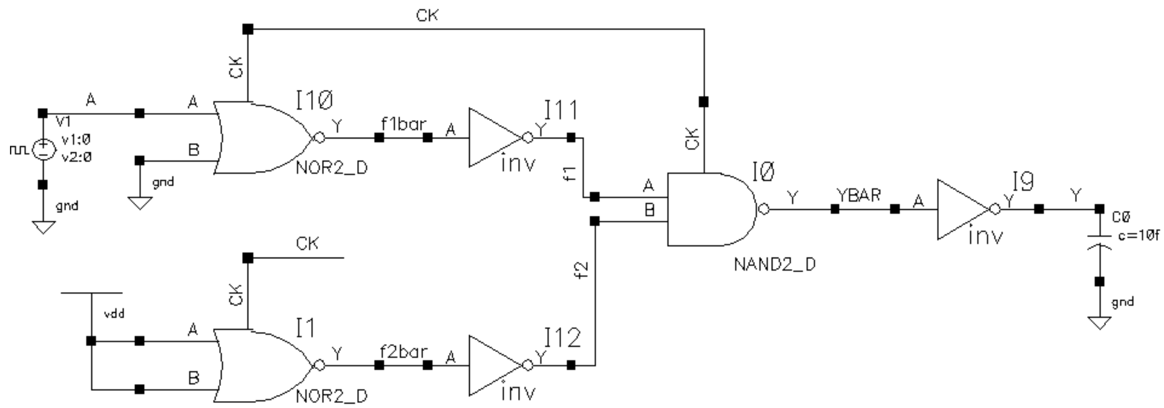

Figure 4: Sample Domino Logic Function.

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Question 4 (10 pts):

In Figure 5, we see another logic function implemented in domino logic.

Create a test bench that will show the worst-case delay for the evaluate logic. (Pick A, B, and C to be high or low before the clock goes high.)

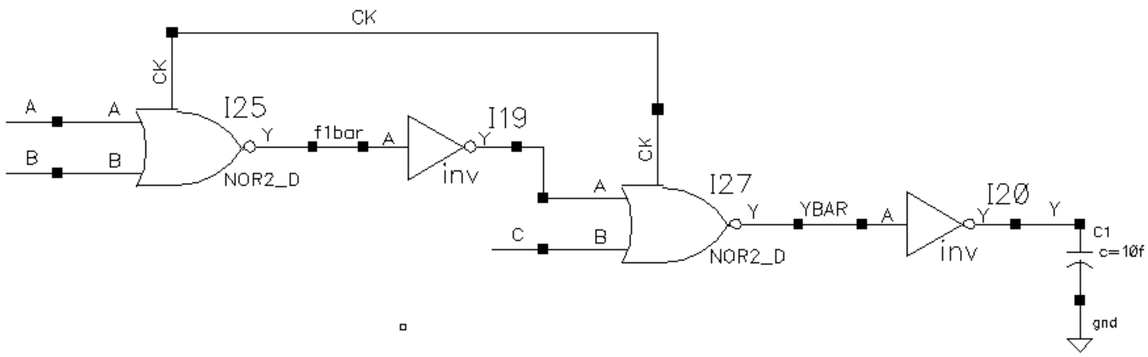

Figure 5: Another function implemented in domino logic.

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Question 5(10pts):

- Using Figure 5, from the previous question write out which transitions sum up to the evaluate time and which transitions sum up to the precharge time.
- Assign a reasonable precharge and evaluate ratio to make the circuit work at 1GHz.

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Question 6(10pts):

In Figure 6, we see two ways of calculating a 6 input NAND function. Using the method of logical effort, find the implementation that produces the minimum delay. Assume that the Cin is 8 for both structures.

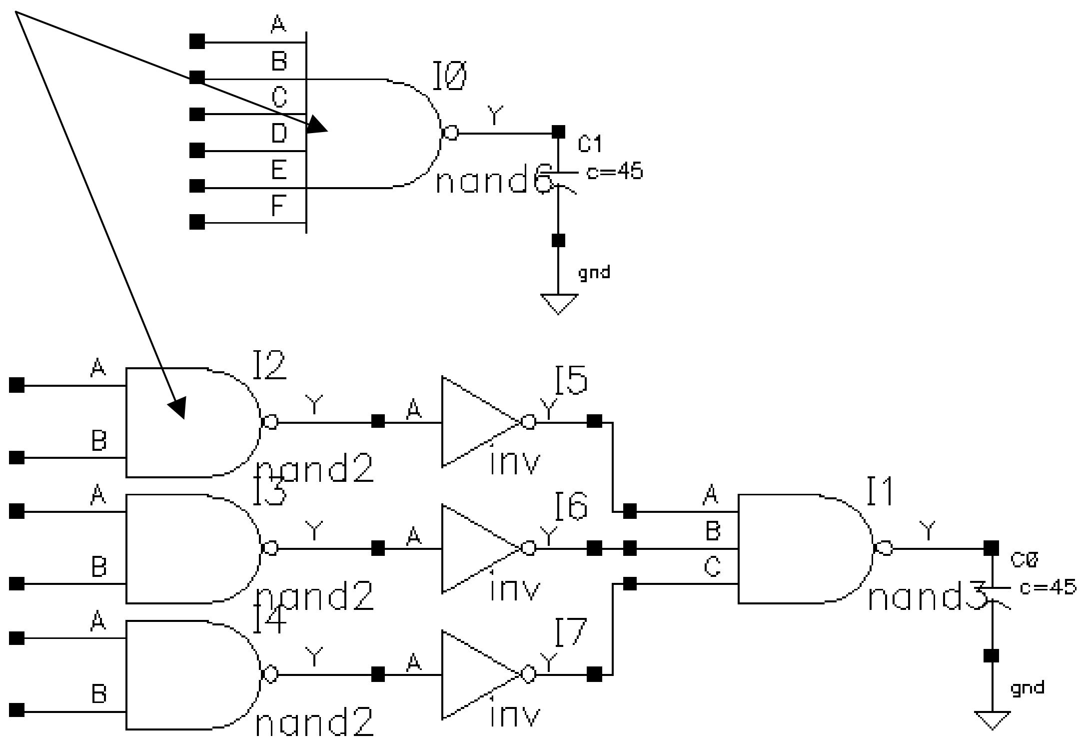

Figure 6: Equivalent Logic functions.

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Question 7(10pts):

We used the equation below to calculate WP and WP for a given Cg and propagation delay.

What does it mean when you calculate a negative WN? How do you fix it?

$$W_N = \frac{C_g + C_{int} + C_{JSWN} \cdot 2 \cdot D_{Drain} \cdot (N + M)}{\frac{\tau_{PHL}}{N_{SN} \cdot L_N \cdot A} - (N + M \cdot R) \cdot \left(C_{JSWN} \cdot 2 + C_{JN} \cdot D_{Drain}\right)}$$

$$W_P = R \cdot W_N \qquad R = \frac{S \cdot R \cdot N_{SP}}{N_{SN}}$$

N is the number of NMOS drain capacitances in the complex gate.

M is the number of PMOS drain capacitances in the complex gate.