

Problem 1(40PTS):

Do the online tutorials:

<http://www.engr.sjsu.edu/~dparent/ICGROUP/UNIX.pdf>

and

http://www.engr.sjsu.edu/~dparent/ICGROUP/CDS_1.pdf

to either learn the basics of the tool or refresh your memory.

Problem 2(50PTS):

Design a CMOS inverter in **the tsmc .18 deep process** with the following specification:

$t_{phl}=t_{plh}=30\text{ps}$ (with in 10%)

$C_g=60\text{fF}$

No layout required.

Problem 3(10PTS):

Develop a Model for a 2 input NAND gate (worst or slowest case) for **the tsmc .18 deep process**.

Find A and R.

Verify the model for various load and a 3 input NAND gate.

Explain why A and R are different for from the inverter.

Problem 3(10PTS):

Label each section of the ID graph as being in sub threshold, saturation, and velocity saturation.

Write down the generic equations for each area of operation.

Describe why each area of the graph follows the generic equation.

Redraw the graph if L was increased by 3 times.

