

#1: Do Problem 8.13 from the book.

Essentially we have to calculate the processing cost of the old die and the new die and compare them.

$$\text{Area}_{\text{DIE_OLD}} := 4 \cdot 10^{-3} \text{ m} \cdot 4 \cdot 10^{-3} \text{ m} \quad \text{Area}_{\text{DIE_OLD}} = 1.6 \times 10^{-5} \text{ m}^2$$

$$\text{Area}_{\text{DIE_NEW}} := 3.3 \cdot 10^{-3} \text{ m} \cdot 3.3 \cdot 10^{-3} \text{ m} \quad \text{Area}_{\text{DIE_NEW}} = 1.089 \times 10^{-5} \text{ m}^2$$

$$Y_w := .8 \quad Y_{pa} := .98 \quad D := 8.254 \cdot 10^{-3} \text{ m} \quad D = 0.203 \text{ m} \quad r := \frac{D}{2}$$

$$W_{\text{OLD}} := 2200 \quad W_{\text{NEW}} := 3000$$

$$N := \pi \cdot \left(\frac{r^2}{\text{Area}_{\text{DIE_OLD}}} - \frac{2r}{\sqrt{2 \cdot \text{Area}_{\text{DIE_OLD}}}} \right) \quad N = 1.914 \times 10^3$$

$$R_{\text{Process}} := \frac{W_{\text{OLD}}}{N \cdot Y_w \cdot Y_{pa}} \quad R_{\text{Process}} = 1.466$$

$$N := \pi \cdot \left(\frac{r^2}{\text{Area}_{\text{DIE_NEW}}} - \frac{2r}{\sqrt{2 \cdot \text{Area}_{\text{DIE_NEW}}}} \right) \quad N = 2.841 \times 10^3$$

$$R_{\text{Process}} := \frac{W_{\text{NEW}}}{N \cdot Y_w \cdot Y_{pa}} \quad R_{\text{Process}} = 1.347$$

We see that the new process is more cost effective. We must remember that we assumed Y_w and Y_{ps} did not change. From the text Y_w is from 70-90% for a mature process. What if the yield dropped to 70%?

$$Y_w := .7 \quad R_{\text{Process}} := \frac{W_{\text{NEW}}}{N \cdot Y_w \cdot Y_{pa}} \quad R_{\text{Process}} = 1.539$$

The cost will be worse until the process matures!

#2: Do Problem 2.2 from the book.

We are to prove that a two transistors in series will produce the same amount of current as a single transistor with twice the length. We use this all the time when we use the “effective length” and “effective width” of a NAND, NOR or AOI Gate to make an equivalent inverter, so we can estimate propagation delay and VTH.

$$I_{DS1} = \frac{\beta}{2} \left[(V_{DD} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Set up the equations in the linear mode.

$$I_{DS2} = \frac{\beta}{2} \left[(V_{DD} - V_T) \cdot V_1 - \frac{V_1^2}{2} \right]$$

$$I_{DS2} = \beta \left[(V_{DD} - V_T) \cdot V_1 - \frac{V_1^2}{2} \right]$$

$$I_{DS2} = \beta \left[(V_{DD} - V_1 - V_T) \cdot (V_{DS} - V_1) - \frac{(V_{DS} - V_1)^2}{2} \right]$$

Solve for V1 and get a huge mess that no one can understand.

$$\beta \left[(V_{DD} - V_1 - V_T) \cdot (V_{DS} - V_1) - \frac{(V_{DS} - V_1)^2}{2} \right] = \beta \left[(V_{DD} - V_T) \cdot V_1 - \frac{V_1^2}{2} \right]$$

$$\left[\begin{array}{l} -V_T + V_{DD} + \frac{1}{2} \cdot \left(4V_T^2 - 8V_T \cdot V_{DD} + 4V_{DD}^2 - 4V_{DD} \cdot V_{DS} + 2V_{DS}^2 + 4V_T \cdot V_{DS} \right)^{\frac{1}{2}} \\ -V_T + V_{DD} - \frac{1}{2} \cdot \left(4V_T^2 - 8V_T \cdot V_{DD} + 4V_{DD}^2 - 4V_{DD} \cdot V_{DS} + 2V_{DS}^2 + 4V_T \cdot V_{DS} \right)^{\frac{1}{2}} \end{array} \right]$$

$$[(V_{DD} - V_1 - V_T) \cdot (V_{DS} - V_1)] = [(V_{DD} - V_T) \cdot V_1]$$

Realize that squared terms are very small.

$$[(V_{DD} - V_T) \cdot (V_{DS} - V_1) - V_1(V_{DS} - V_1)] = [(V_{DD} - V_T) \cdot V_1]$$

Realize that there is still a very small term with v1 squared.

$$[(V_{DD} - V_T) \cdot (V_{DS} - V_1)] = [(V_{DD} - V_T) \cdot V_1]$$

$$\frac{1}{2} \cdot V_{DS}$$

Solve for V1

$$I_{DS1} = \frac{\beta}{2} [(V_{DD} - V_T) \cdot V_{DS}]$$

$$I_{DS2} = \beta [(V_{DD} - V_T) \cdot V_1]$$

$$I_{DS2} = \beta [(V_{DD} - V_T) \cdot \frac{1}{2} V_{DS}]$$

Using the linear approximation they are equal. I tried this with MATHCAD and the mess of an equation. It could not simplify the equation, but numerically it did show that they were equivalent.

#3: Do Problem 2.3 from the book.

In the previous exercise the body effect was ignored. V_T of the top transistor is larger than the V_T of the bottom transistor due to the fact the V_{SB} of the top transistor is not zero volts. If we rewrite the equation for the top transistor to have a $V_{T2} > V_T$

Then:

$$[(V_{DD} - V_{T2}) \cdot (V_{DS} - V_1)] = [(V_{DD} - V_T) \cdot V_1]$$

new V1

$$(-V_{DD} + V_{T2}) \cdot \frac{V_{DS}}{(-2 \cdot V_{DD} + V_{T2} + V_T)}$$

We see that the new V_1 is smaller than the old V_1 and that the current will be less. This means that when we scale W_N by 2 for a 2 input NAND gate we will need to scale it a little bit more than two because less current will flow than an inverter with a W_N that is doubled. (Velocity saturation also plays a role in reducing the accuracy of the equivalent inverter model.)

#4: Do Problem 2.7 from the book.

Does the body effect limit the number of transistors that can be placed in series at low frequencies?

At high frequencies the parasitic drain caps will slow down the circuit making W_N larger and larger (which makes the drain caps larger.). As seen from question 2.3 less current will flow in a series of transistors, thus they need to be larger. This increases the delay. What about low frequencies? If the circuit is slow, then delay is not a big problem and the output will eventually settle at the correct value. The problem is that the switching threshold of an n -input NAND gate will keep getting larger (or the lower for an n -input NOR) until the noise margins are unacceptable skewed.

Start with a CMOS inverter in

TSMC24 Deep $W_N: 1\mu\text{m}$ and $W_P = 2.34\mu\text{m}$. Measure V_{inh} .

Start stacking nmos in series and measure. The noise margins change rapidly up to $N=5$.

The rule of thumb is stack no more than 4.

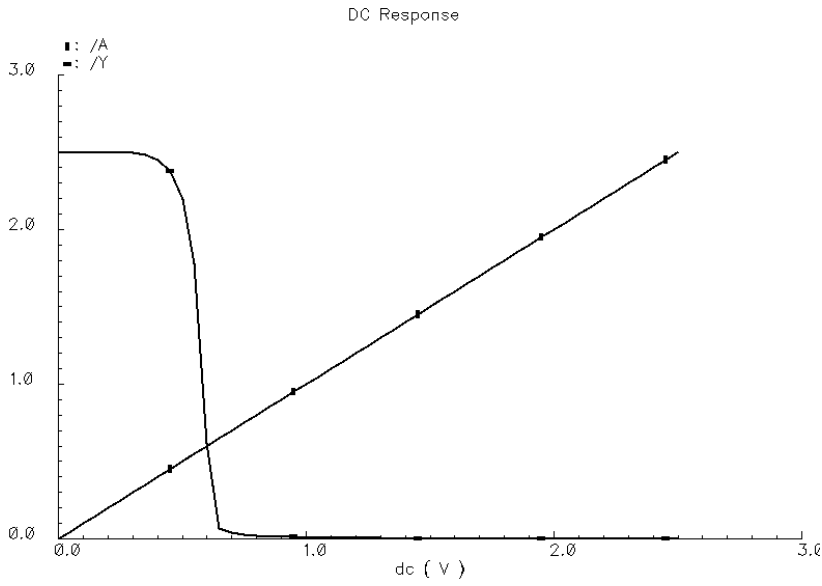


Figure 1: Inverter with $W_P=2.34\mu\text{m}$, $W_N=1\mu\text{m}$, 1 NMOS in Series

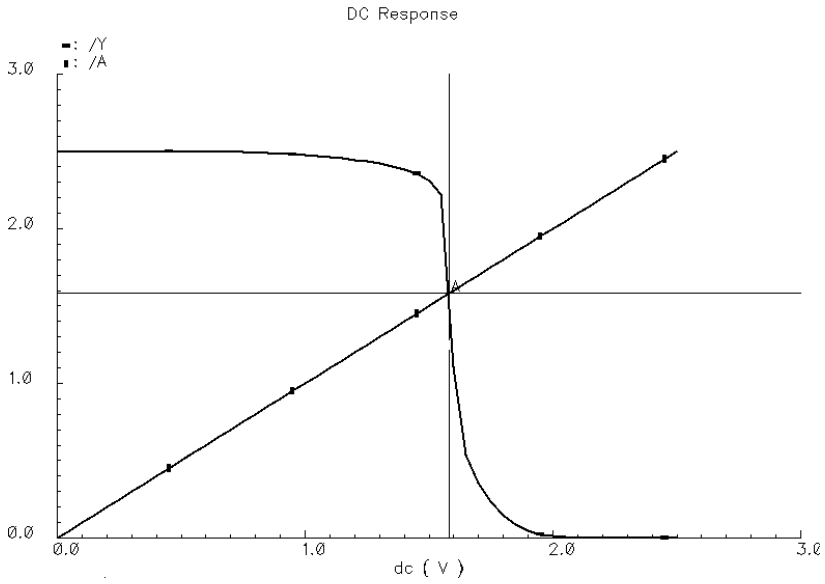
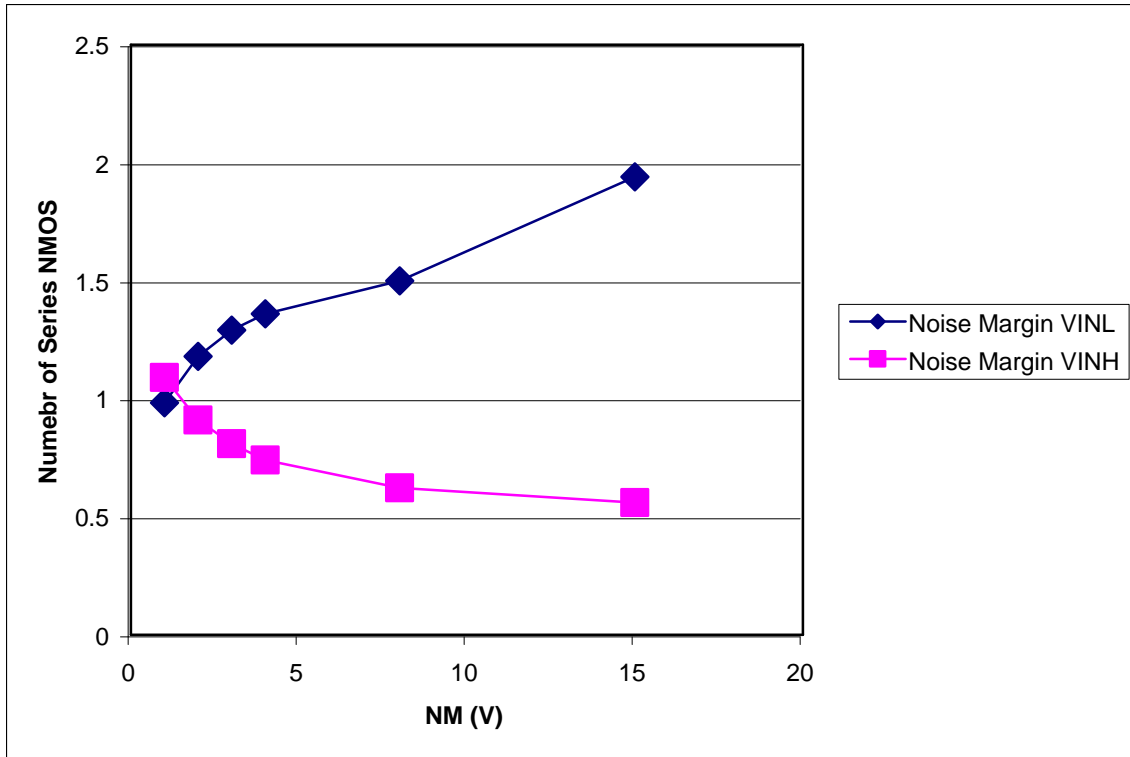


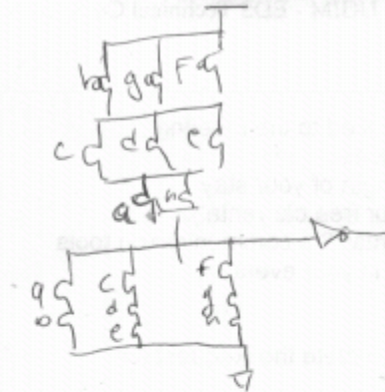
Figure 2: Inverter with $W_P=2.34\mu\text{m}$, $W_N=1\mu\text{m}$, 8 NMOS in Series



#5: Do Problem 2.8 from the book.

To have fast transistors sometime the process engineers set design the transistors to have a V_T of 0Volts. These transistors have a lot of sub-threshold leakage current. In standby you would want to raise V_T electrically to prevent this leakage. This is done by setting V_{SB} greater than Zero Volts in the NMOS case. If V_{SB} is now greater than zero, but the source is still connected to ground, the body voltage has to be set lower than zero, or negatively biased.

#6: Design the schematic for $f=ab+cde+fgh$



$$f = ab + cde + fgh$$

h g f c d e b a

x	x	x	x	x	x	x	x	x
x			x			x		x
			n	o	f	c	d	e
						b	a	

