

Area Delay Product

EE224

SJSU

David Parent

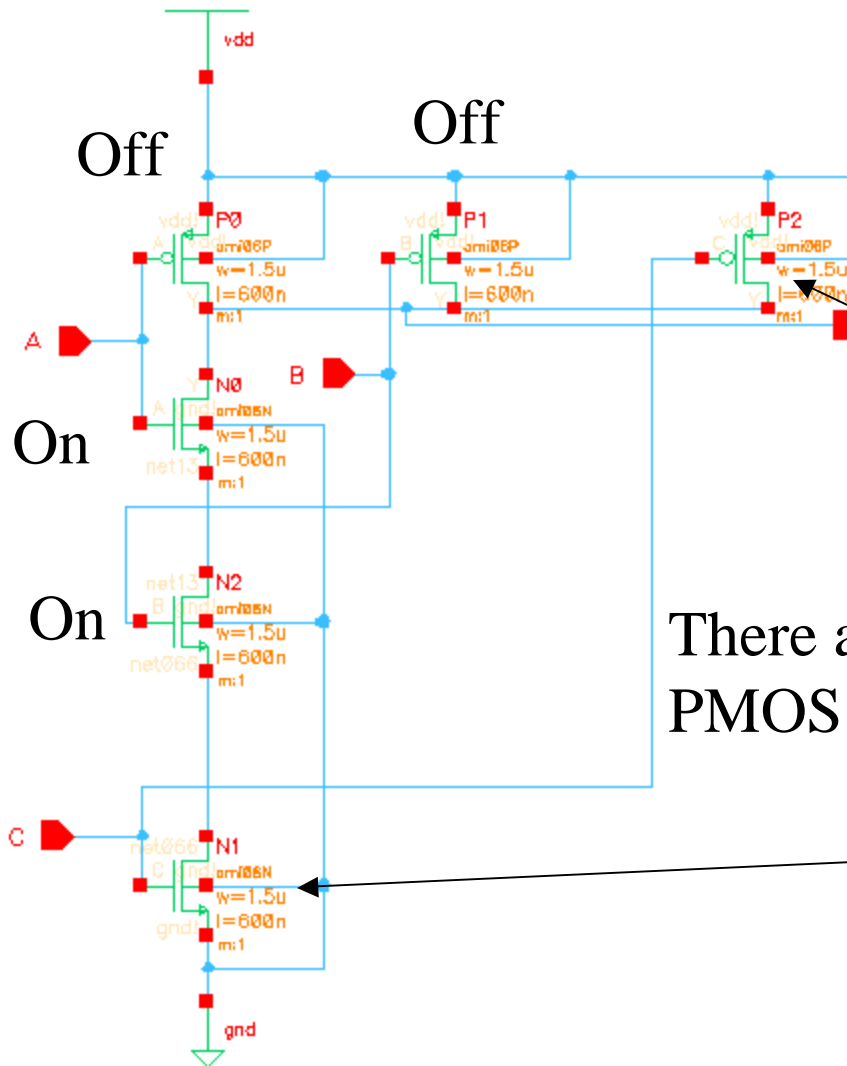
NAND Example

- We want to design an optimized 3 input NAND gate with symmetric rise and fall time for the worst case transitions. (The load will be 3 NAND3 gates)
 - We want to optimize for **speed** and **area**.
 - Of course these are opposing criteria.
 - **Area goes up, when you increase the width of the transistors to have smaller (faster) delay times.**
 - Note: Symmetric rise and fall times leads to better noise performance.

What are the “worst-case” transitions?

- Rise time or propagation delay low to high:
 - Only one PMOS is available to charge to VDD
- Fall time or propagation delay high to low:
 - Does it make a difference both NMOS transistors have to be on to discharge?
 - Yes! If the bottom most NMOS turn on after the other NMOS in the tree, then the output load capacitance is composed of all the drain caps in the tree!

Low to High Worst Case



Turns On

Only one PMOS conducts

There are 5 NMOS drain caps and three PMOS drain caps to charge

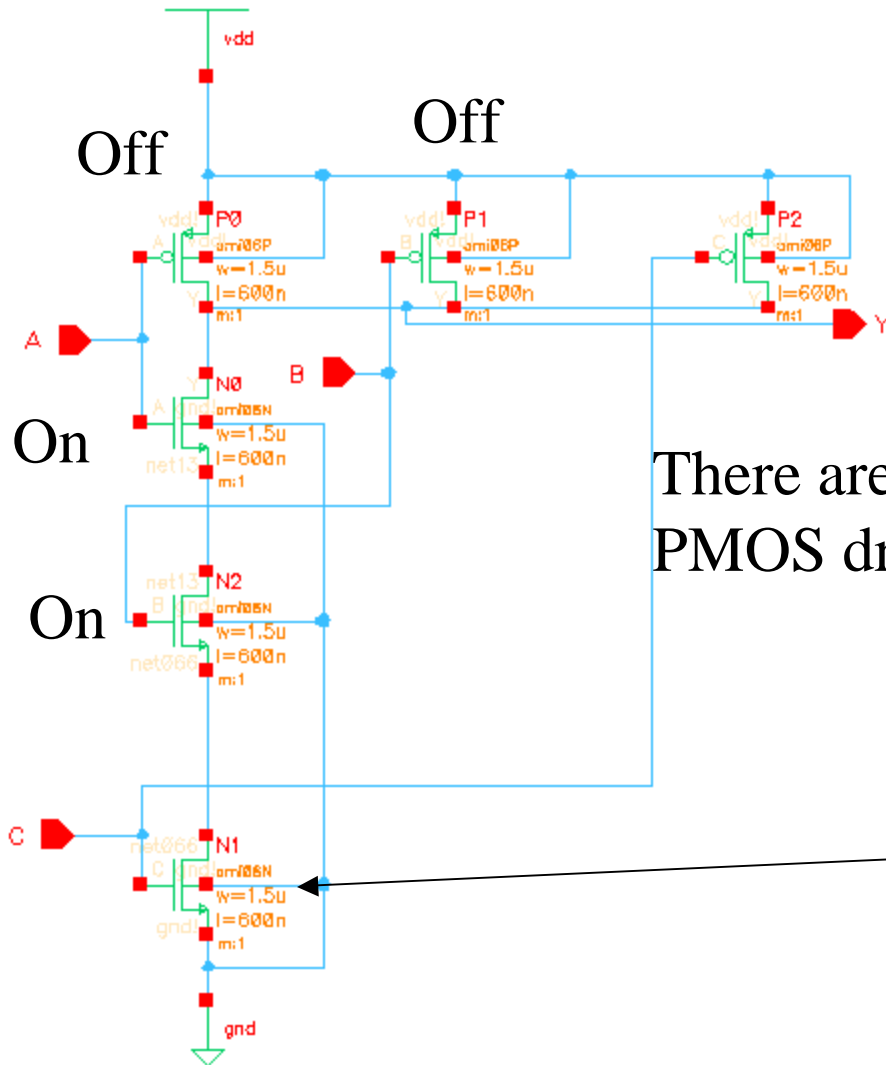
Turns Off

High to low Worst Case

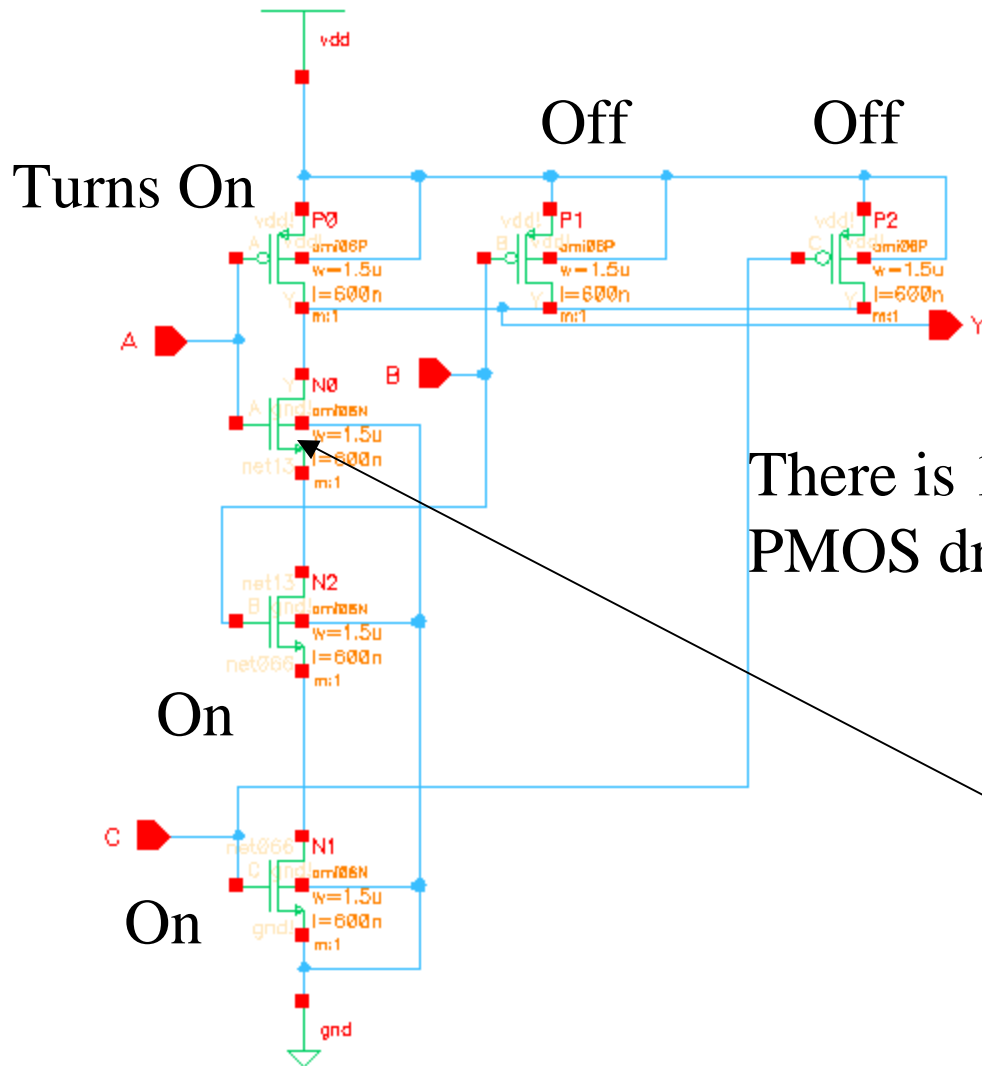
Turns Off

There are 5 NMOS drain caps and three PMOS drain caps to charge

Turns On



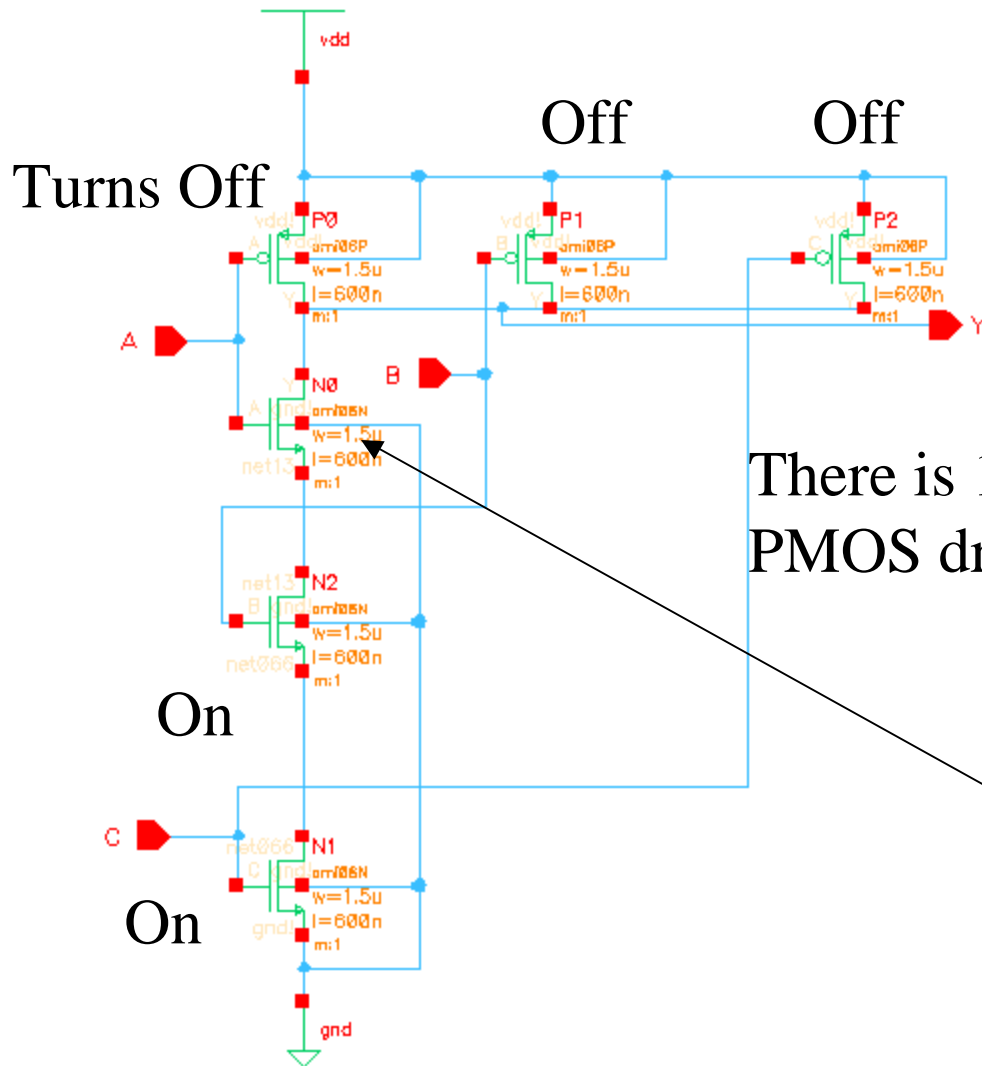
Low to High Better Case



There is 1 NMOS drain cap and three PMOS drain caps to charge

Turns Off

High to Low Best Case



There is 1 NMOS drain cap and three PMOS drain caps to discharge

Turns On

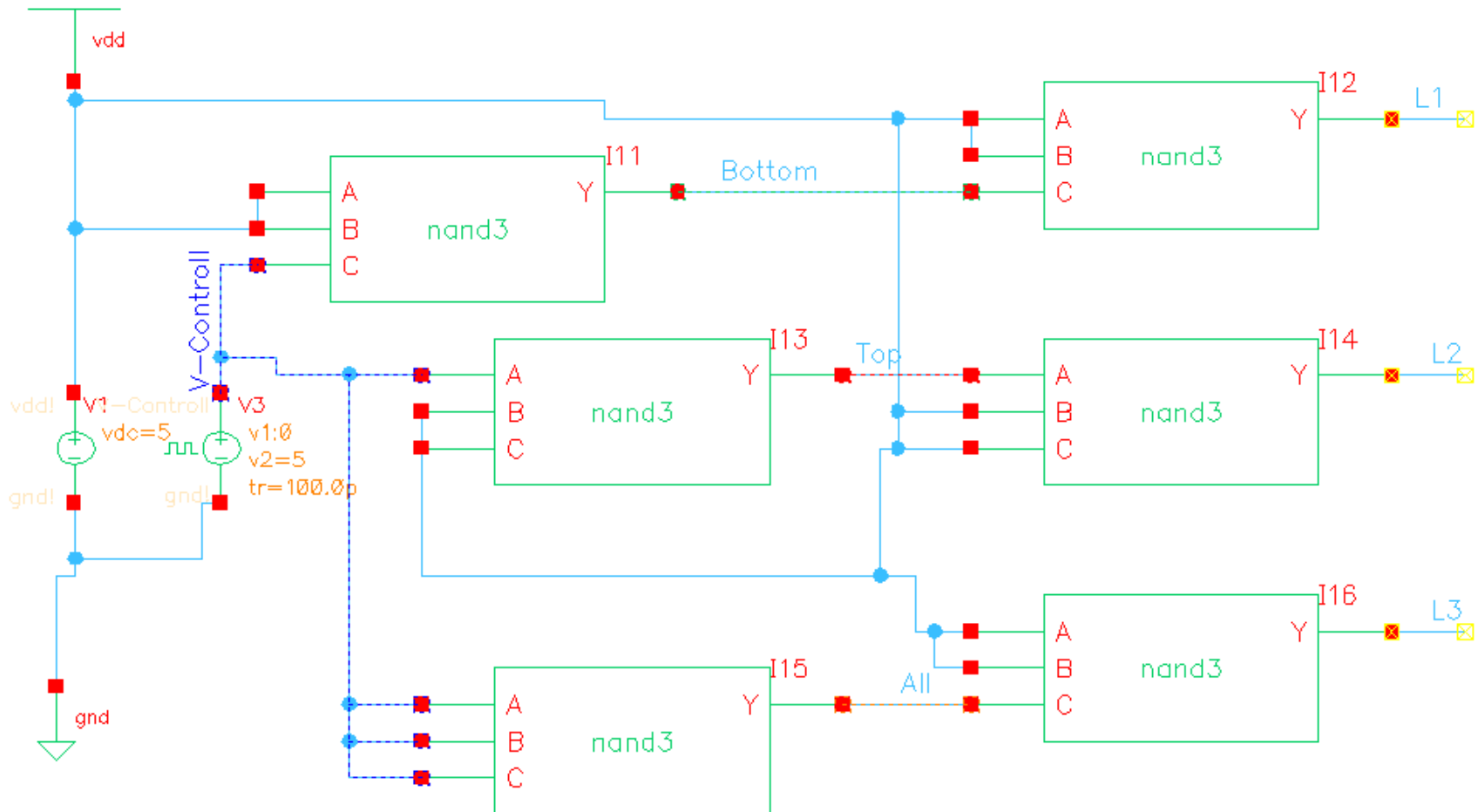
What if all the inputs were tied together?

- The charge times would be the fastest
- The discharge time would in fact be slower because more PMOS would be trying to charge until they are turned off!
- More feedback capacitances would be seen.

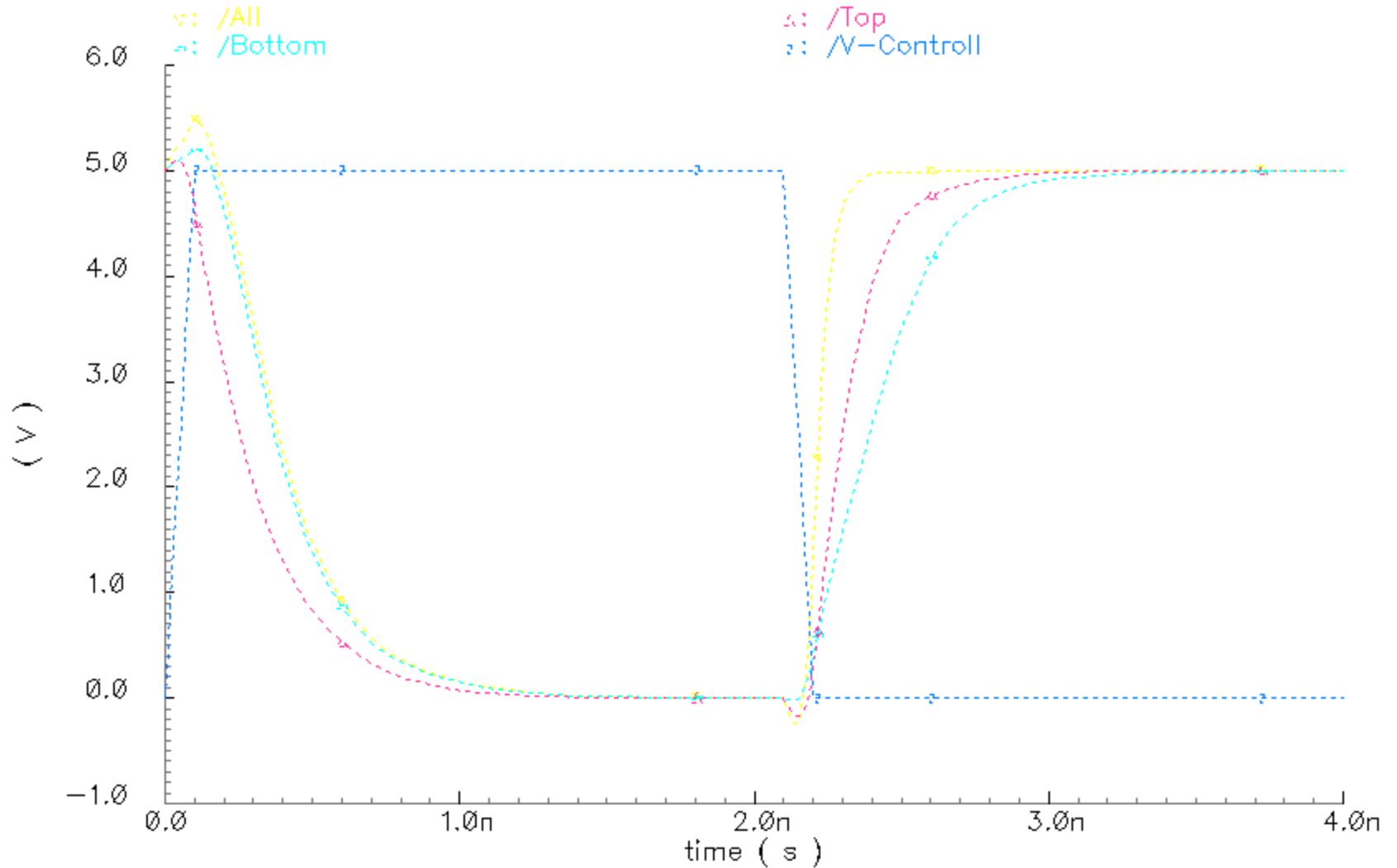
What to do?

- If possible have the signal that controls the gates state closest to the output node.
- Make sure that you realize that the noise performance will change depending on how many PMOS transistors are conducting.
 - The more PMOS transistors conduct the higher the switching threshold in an NAND configuration.

Setting up a NAND3 test bench



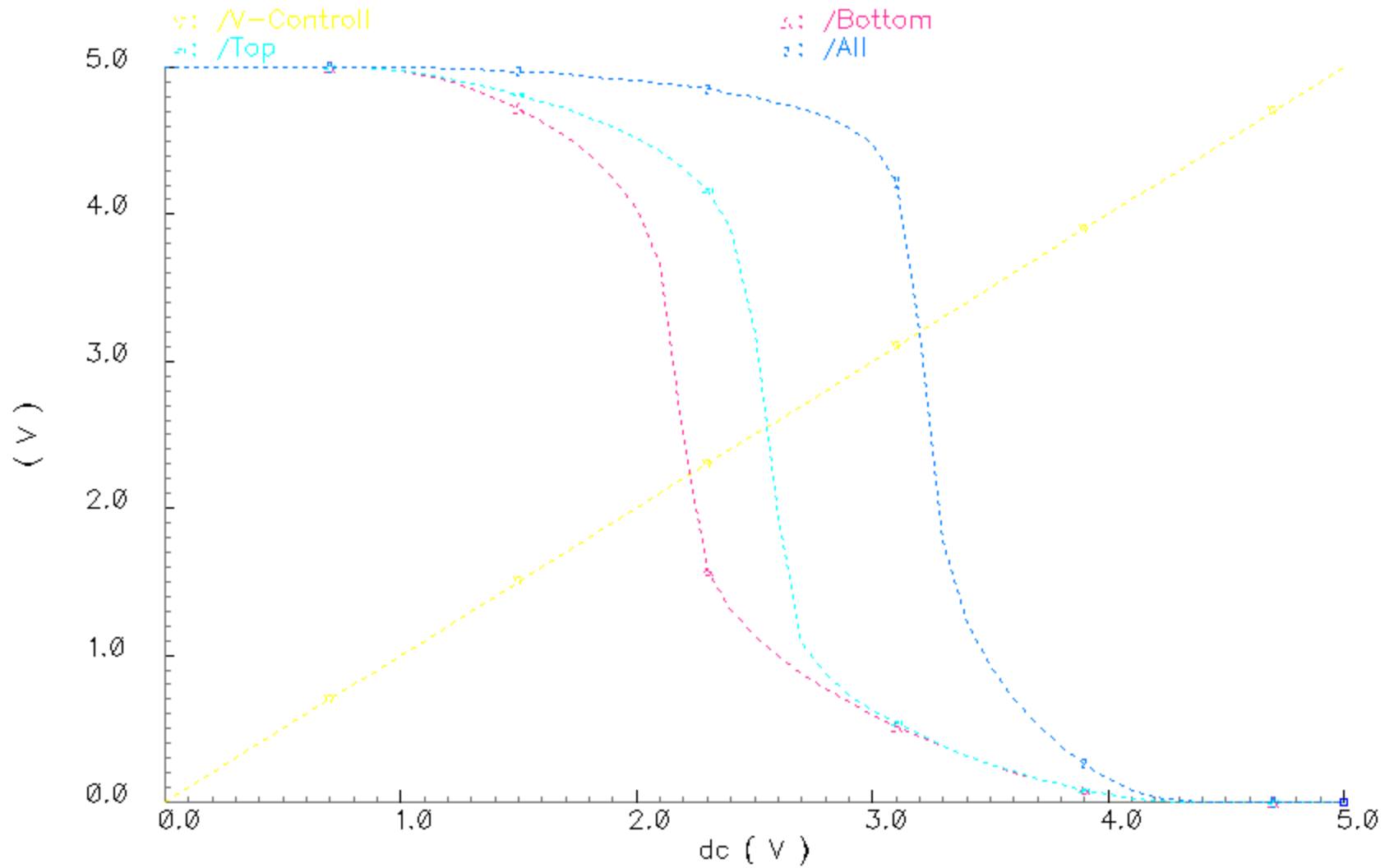
Transient Response



Summary

- Having the top NMOS transistor control the signal is faster than having the bottom transistor control the signal.
- Having all the inputs toggle at the same time improves the rise time, but degrades the fall time.
- Having all the inputs toggle is no more than having an inverter (logically), so why bother?
 - Maybe you need an inverter with a different noise performance.

DC Response



Estimating the delay

- We now know which test vectors will produce the slowest delay
- Now we need to:
 - Calculate the input and output capacitances of a NAND3 gate, assuming that the NAND3 will drive 3 identical NAND3 gates and that $W_P = W_N$.
 - Then we calculate the fall time vs. W_N .

Calculating Input Capacitance

$$\begin{aligned}
 W_N &:= 1.5 \cdot 10^{-4} \text{ cm} & L_N &:= .6 \cdot 10^{-4} \text{ cm} & C_{GN} &:= \frac{3.9 \cdot 8.85 \cdot 10^{-14} \cdot \frac{\text{F}}{\text{cm}}}{.014 \cdot 10^{-4} \text{ cm}} \cdot W_N \cdot L_N \\
 W_P &:= W_N & L_P &:= L_N & L_D &:= 1.5 \cdot 10^{-4} \text{ cm} & C_{GP} &:= \frac{3.9 \cdot 8.85 \cdot 10^{-14} \cdot \frac{\text{F}}{\text{cm}}}{.014 \cdot 10^{-4} \text{ cm}} \cdot W_P \cdot L_P \\
 K_{NP} &:= 46.3 \cdot 10^{-6} \frac{\text{A}}{\text{V}^2} & K_{PP} &:= 30 \cdot 10^{-6} \frac{\text{A}}{\text{V}^2} \\
 V_{DD} &:= 5\text{V} & V_{TP} &:= -.82\text{V} & V_{TN} &:= .6\text{V} \\
 C_{GDOP} &:= 2.4 \cdot 10^{-12} \frac{\text{F}}{\text{cm}} & C_{FBP} &:= C_{GDOP} \cdot W_P \\
 C_{GDON} &:= 1.99 \cdot 10^{-12} \frac{\text{F}}{\text{cm}} & C_{FBN} &:= C_{GDON} \cdot W_N & C_{IN} &:= 5.1 \times 10^{-15} \text{ F} \\
 C_{IN} &:= C_{GN} + C_{GP} + C_{FBN} + C_{FBP}
 \end{aligned}$$

Calculating Output Capacitance

$$C_{JSWN} := 3.83 \cdot 10^{-12} \frac{\text{F}}{\text{cm}}$$

$$C_{JN} := 4.23 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$C_{JSWP} := 3.11 \cdot 10^{-12} \frac{\text{F}}{\text{cm}}$$

$$C_{JP} := 7.27 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$C_{DP} := C_{JP} \cdot W_P \cdot L_D + 2 \cdot C_{JSWP} \cdot (W_P + L_D)$$

$$C_{DN} := C_{JN} \cdot W_N \cdot L_D + 2 \cdot C_{JSWN} \cdot (W_N + L_D)$$

$$C_{DP} = 3.5 \times 10^{-15} \text{ F}$$

$$C_{DN} = 3.25 \times 10^{-15} \text{ F}$$

The factor of 2 comes from
the Miller Effect

$$C_{\text{OUT}} := 3 \cdot C_{DP} + 5 \cdot C_{DN} + 2C_{\text{FBN}} + 2C_{\text{FBP}}$$

$$C_{\text{OUT}} = 2.81 \times 10^{-14} \text{ F}$$

Load Capacitance and Delay

$$C_{\text{LOAD}} := C_{\text{OUT}} + 3 \cdot C_{\text{IN}} \quad \leftarrow \text{Remember we are driving 3 NAND3's}$$

$$C_{\text{LOAD}} = 4.34 \times 10^{-14} \text{ F}$$

$$C := \frac{1}{(V_{\text{DD}} - V_{\text{TN}}) \cdot K_{\text{NP}}} \cdot \left[\frac{2(V_{\text{TN}} - .1 \cdot V_{\text{DD}})}{V_{\text{DD}} - V_{\text{TN}}} + \ln \left[\frac{(1.9 \cdot V_{\text{DD}} - 2 \cdot V_{\text{TN}})}{.1 \cdot V_{\text{DD}}} \right] \right]$$

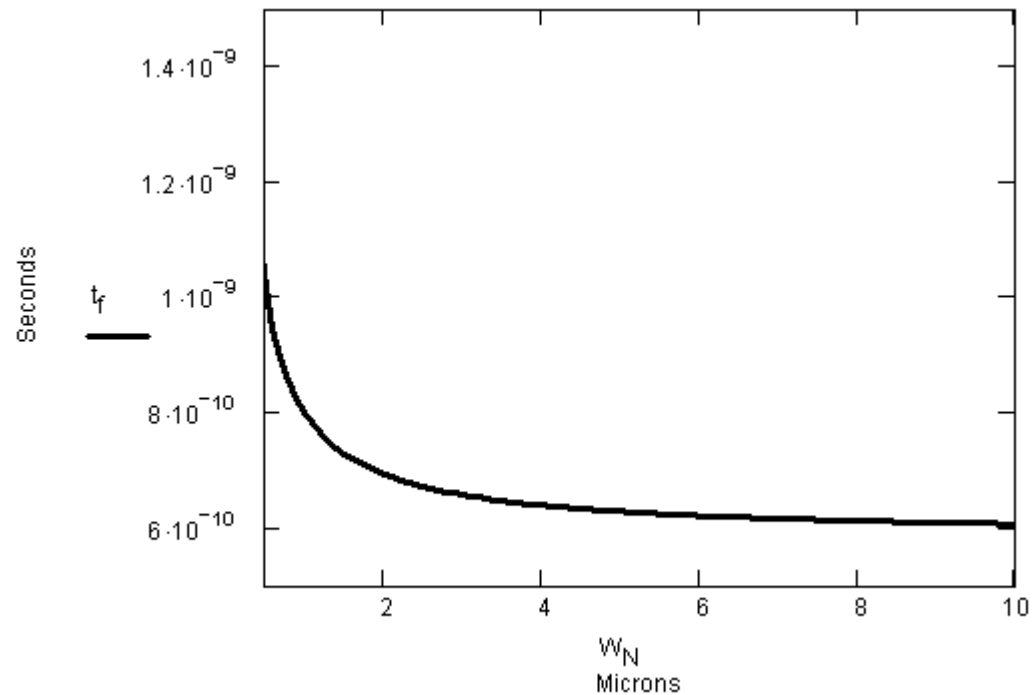
$$C = 1.4 \times 10^4 \Omega$$

$$t_f := \frac{C_{\text{LOAD}} \cdot 3 \cdot L_{\text{N}}}{W_{\text{N}}} \cdot C \quad t_f = 7.29 \times 10^{-10} \text{ s}$$

Note: This matches spice to within 4% error.

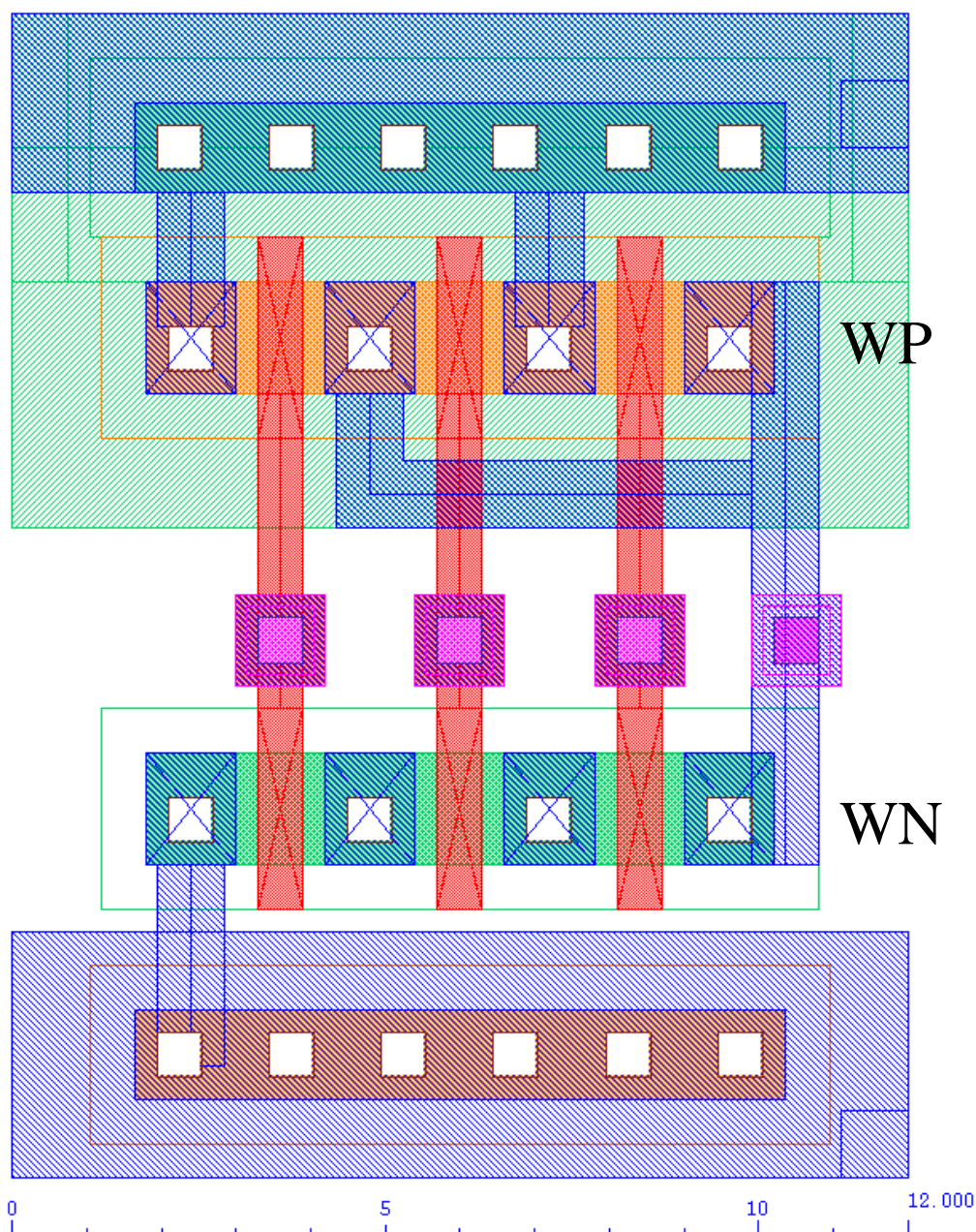
Delay vs. Width

- We need to plot delay vs. W_N (Assuming $W_P=W_N$)



Area vs. Width

- We need to come up with an equation for the area of a NAND3 Gate vs. width.
- Since you have to lay it out any way the easiest thing to do is layout the minimum sized NAND3 and come up with how much the area increases with W_N and W_P



First we calculate the area of the NAND3 if WP and WN=0

$$A_{\text{MIN}} := 15.6 \cdot 12 - 1.5 \cdot 12 - 1.5 \cdot 12$$

$$A_{\text{MIN}} = 1.51 \times 10^2$$

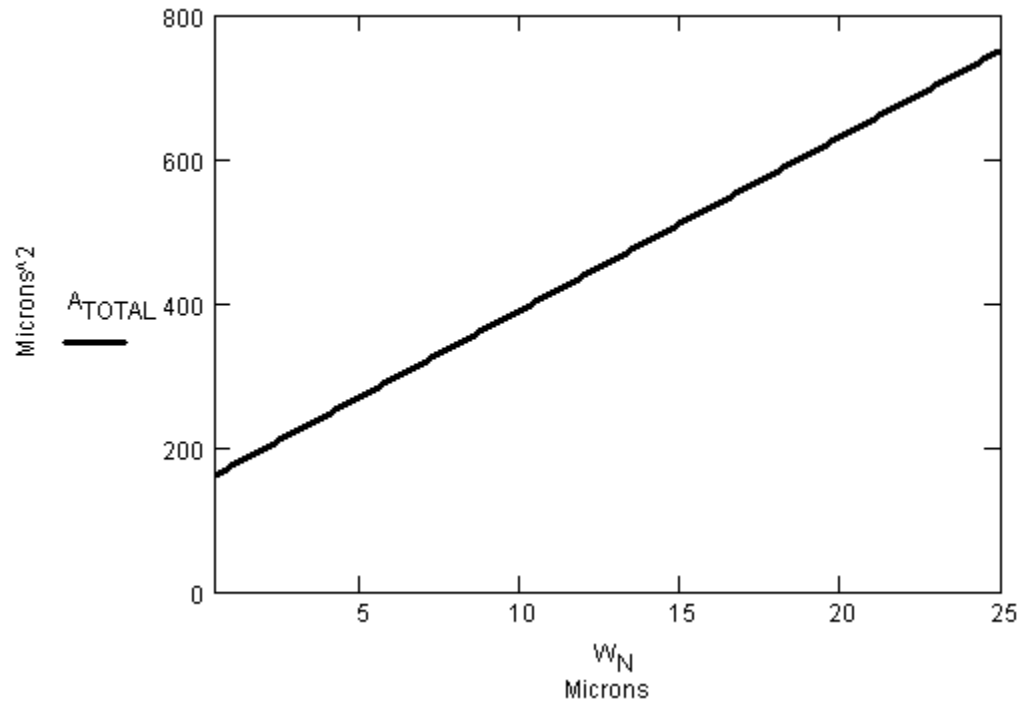
Then we calculate the extra area per WN.

$$A_{\text{EXTRA}} := (W_N + W_P) \cdot 12$$

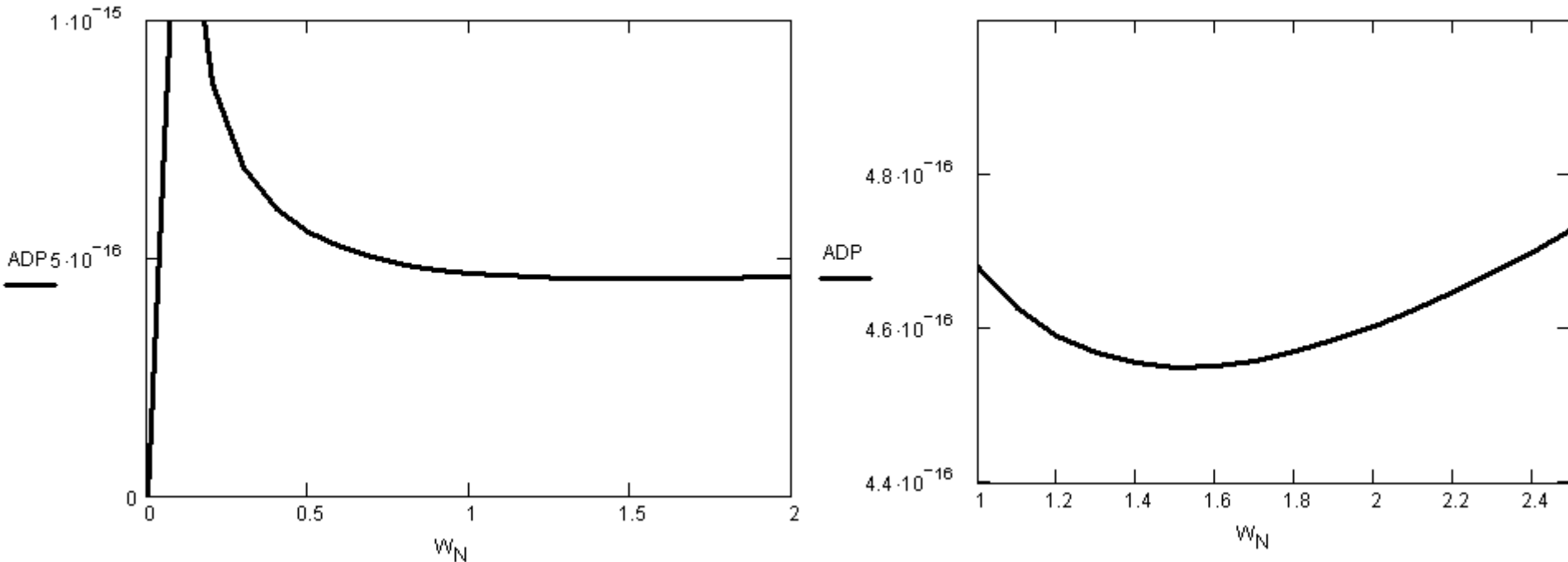
Then we calculate the area as a function of WN and WP=WN

$$A_{\text{TOTAL}} := A_{\text{MIN}} + A_{\text{EXTRA}}$$

Area vs. W_N for NAND3



Area Delay Product for NAND3

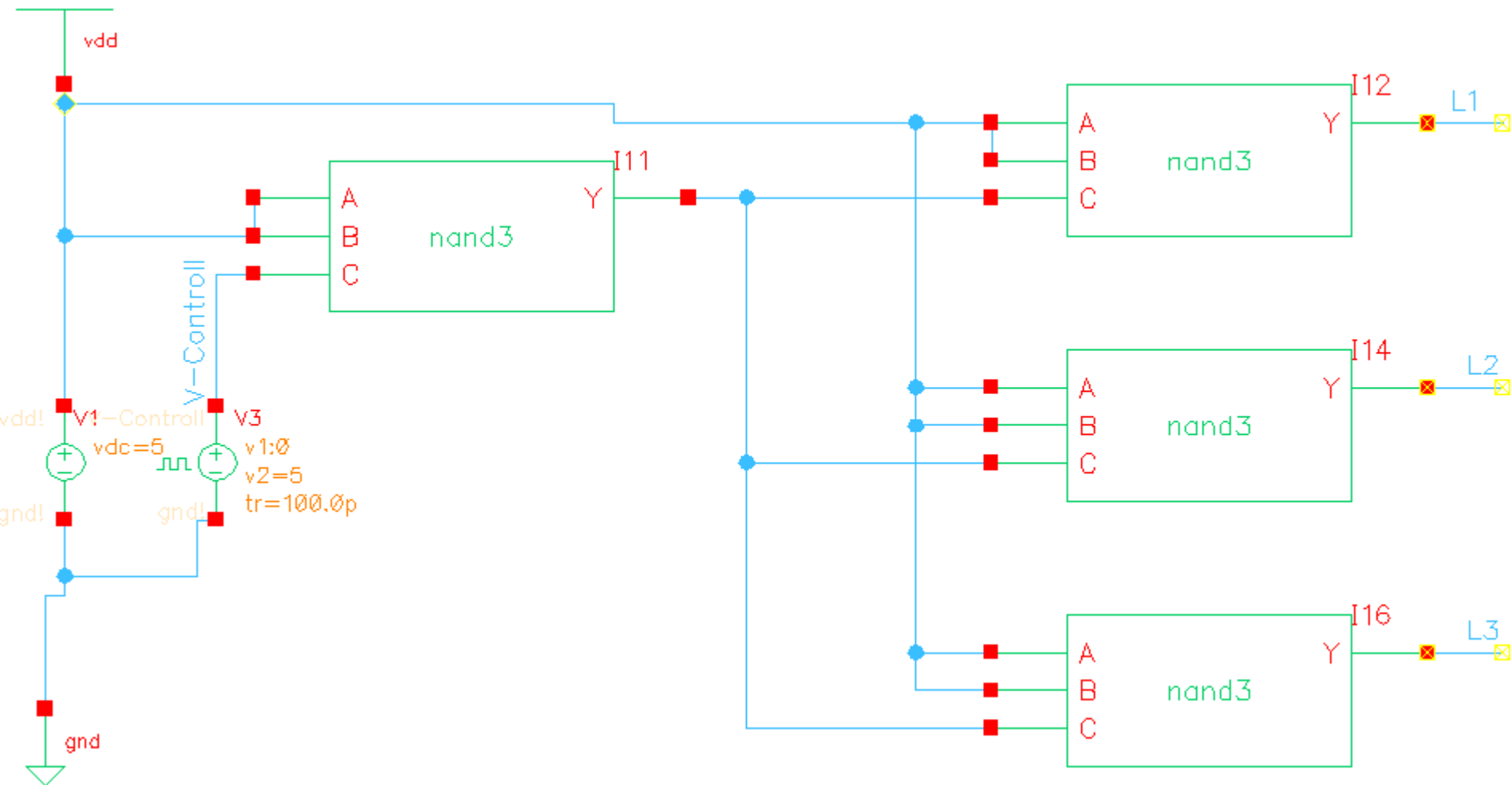


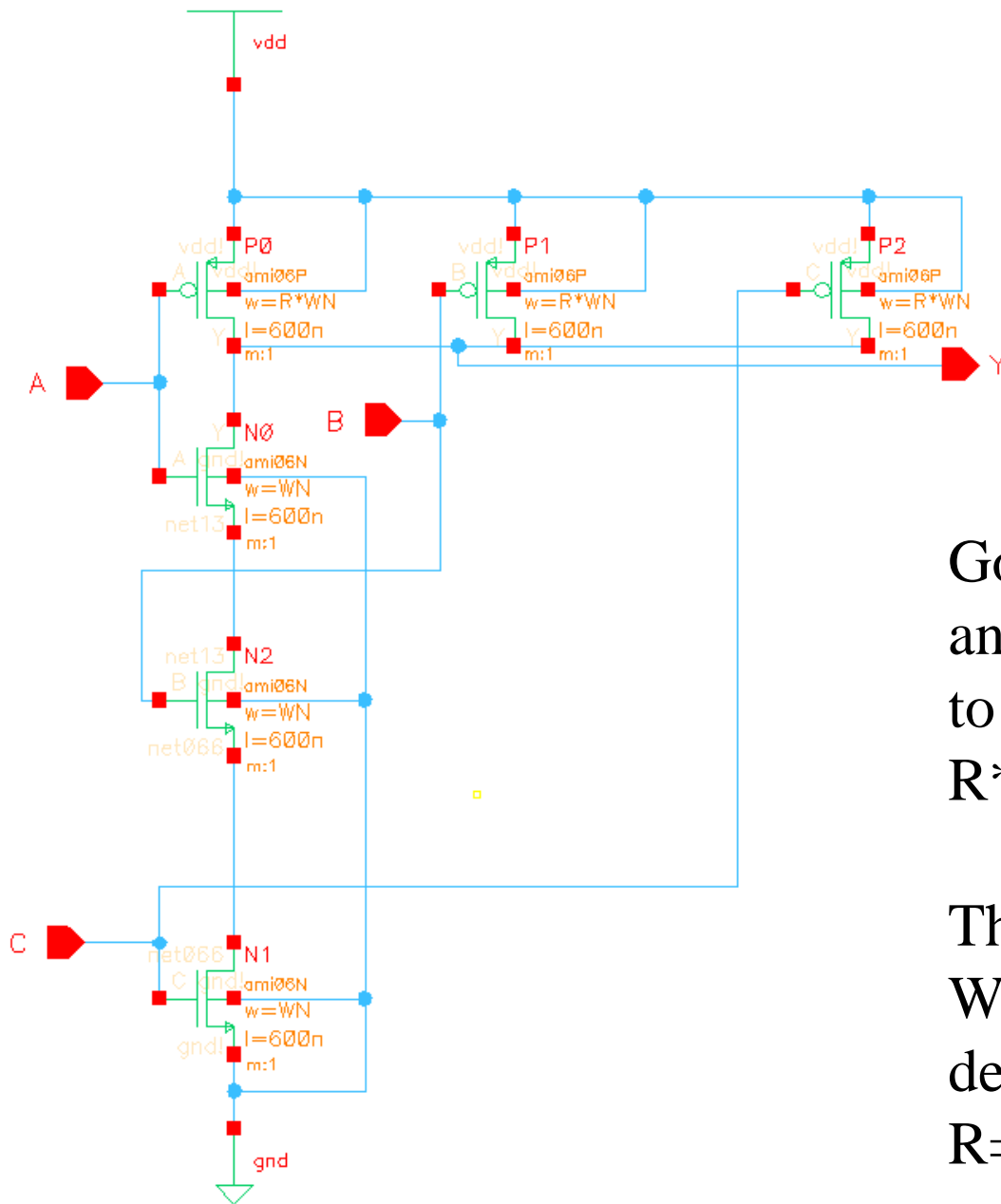
So it looks like the best width to use for ADP is $1.5\mu\text{m}$!
Note: Anything from 1 to 3 is probably ok since the ADP is slowly varying.

Does this match spice?

- We made a lot of assumptions for these hand calculations.
 - Capacitance is constant
 - T C constant does not change with width.
 - The inputs changed instantaneously.
- We had better run this through spice to double check.

Test Bench



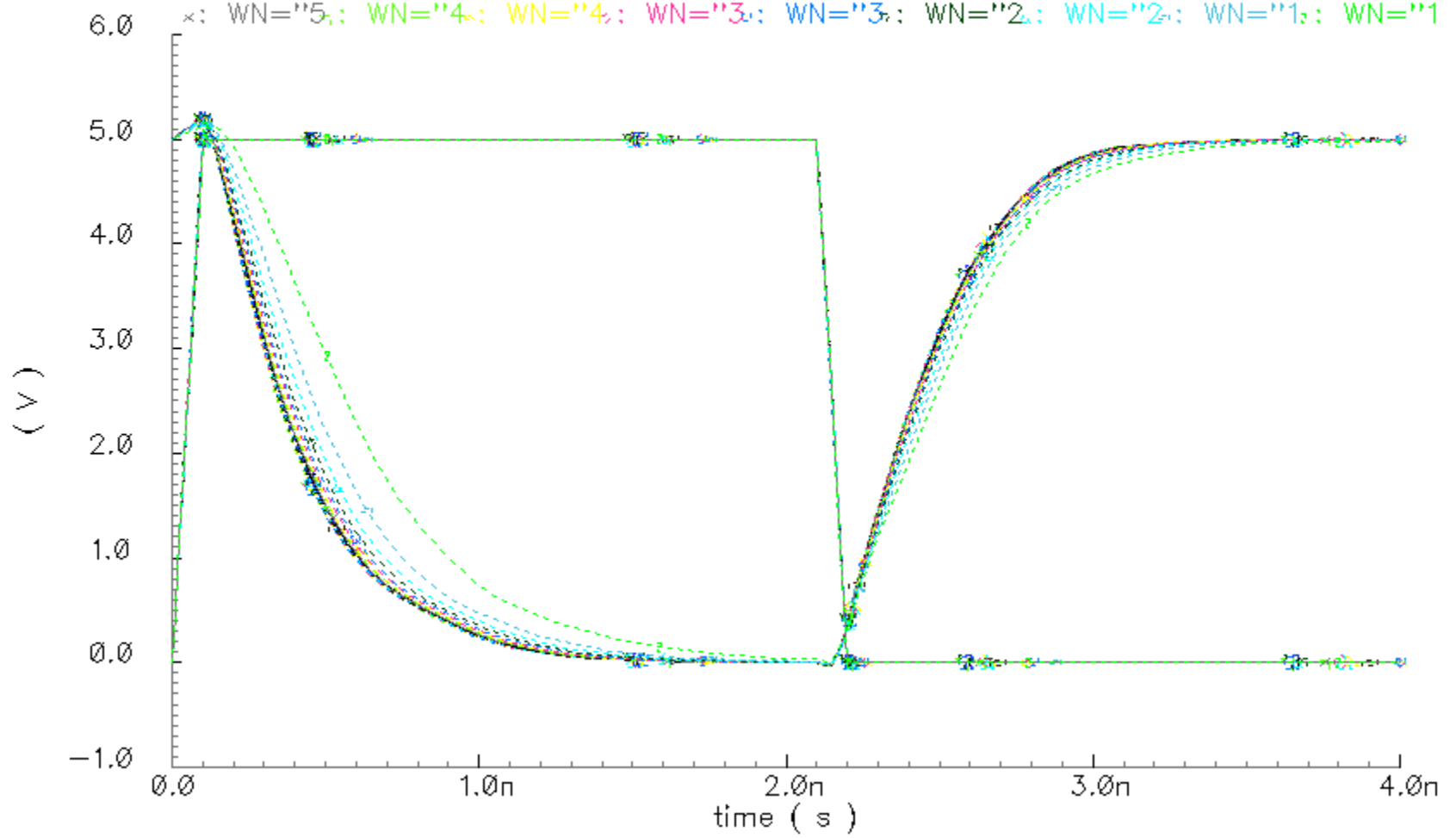


Go into the schematic and change all the widths to WN for nmos4 and $R \cdot WN$ for pmos4

This will allow us to sweep WN and WP and measure the delay as a function of WN
 $R=1$

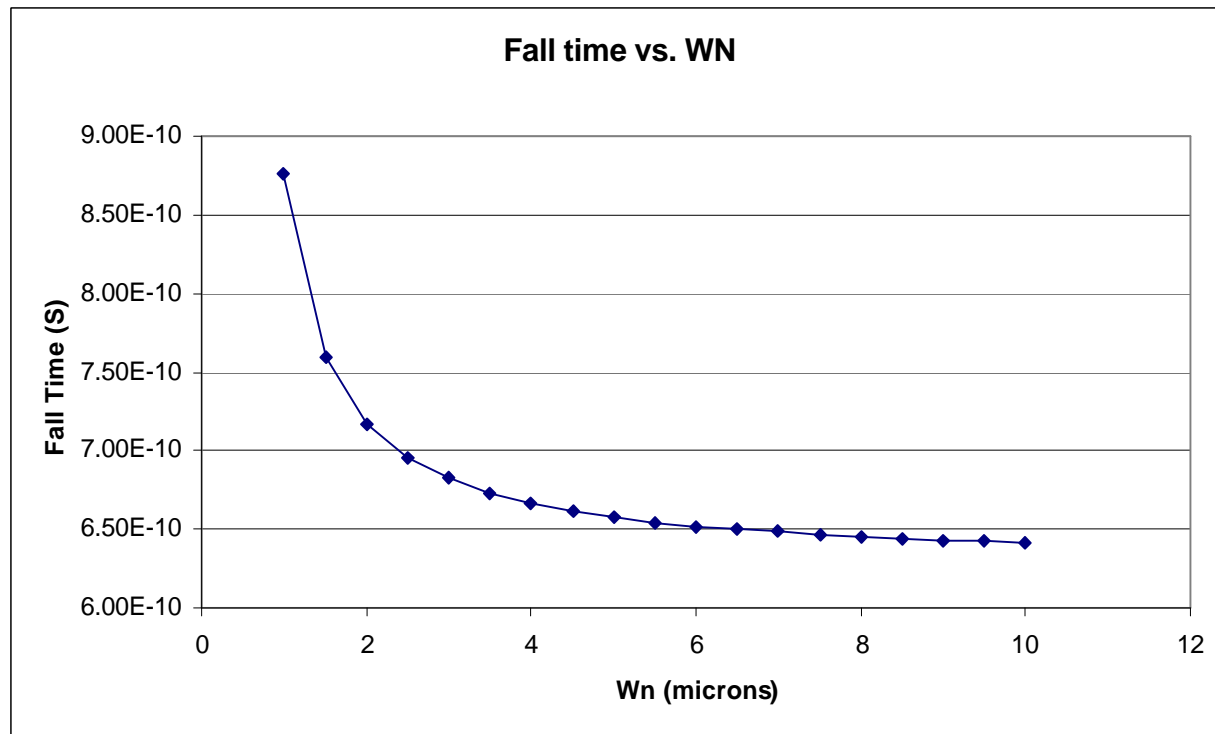
Transient Response

~: WN="1"; WN="9"; WN="8"; WN="8"; WN="7"; WN="7"; WN="6"; WN="6"; WN="5
x: WN="5"; WN="4"; WN="4"; WN="3"; WN="3"; WN="2"; WN="2"; WN="1"; WN="1
~: WN="1"; WN="9"; WN="8"; WN="8"; WN="7"; WN="7"; WN="6"; WN="6"; WN="5
x: WN="5"; WN="4"; WN="4"; WN="3"; WN="3"; WN="2"; WN="2"; WN="1"; WN="1

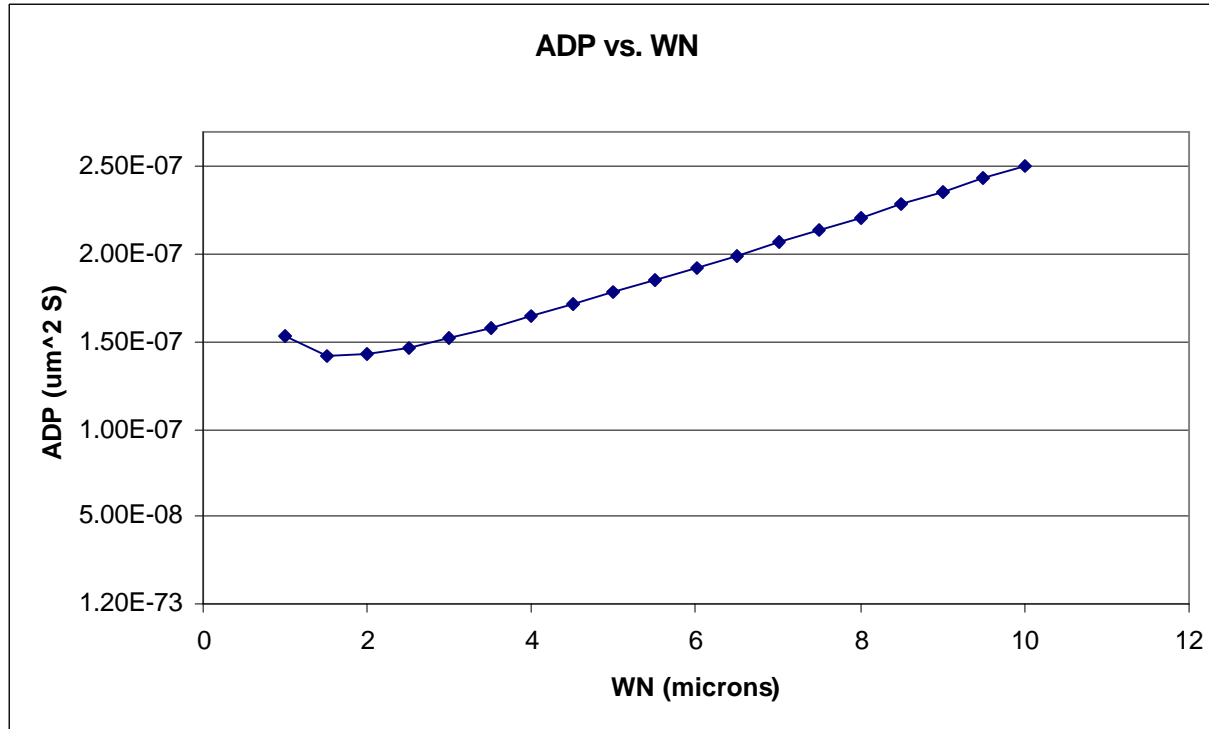


Results From Spice

The maximum error is $\sim 5\%$ at $WN=10\mu\text{m}$.



Results From Spice



Results are the same! WN should be 1.5 for best ADP

What next?

- Now we need to find WP for a symmetric response.
- Note: This will lower our speed and and increase our ADP
 - This will make our transitions symmetric and thus increase our noise margins.

Design a NAND3 for Symmetric Response

- Set the rise and fall times equal to each other and then find a ration between W_P and W_N .

$$\frac{3 \cdot L_N \cdot C}{W_N} := \frac{L_P}{W_P} \cdot D$$

$$R := \frac{D}{3 \cdot C}$$

$$L_N := L_P$$

$$R = 6.42 \times 10^{-1}$$

$$\frac{W_P}{W_N} := \frac{D}{3 \cdot C}$$

If $W_P = W_N \times .642$ and $W_N = 1.5 \mu\text{m}$, then the value for W_P would be less than the allowed $1.5 \mu\text{m}$!

We set $W_P = 1.5$ and then solve for W_N . $W_N = 2.34 \mu\text{m}$, but $2.4 \mu\text{m}$ is what is actually allowed. Use $W_N = 2.34 \mu\text{m}$.

Simulation

- When this is simulated we find that the NAND3 gate is not symmetric!
- Use an iterative process to find WN and Ratio and thus WP.
 1. Run transient for hand calculations.
 2. Measure rise and fall time.
 3. The new ratio is the old ratio times the rise time divided by the fall time.
 4. Repeat 1-3 until you are within a practical value of WP.

Simulation Results

		WP					
WN	ROLD	WP	Real	TF	TR	TR/TF	RNEW
2.4	0.642	1.5408	1.5	476	719	1.510504	0.969743697
2.4	0.969744	2.327385	2.25	614	562	0.915309	0.887615567
2.4	0.887616	2.130277	2.1	583	590	1.012007	0.898273044
2.4	0.898273	2.155855	2.1	588	587	0.998299	0.896745368
2.4	0.896745	2.152189	2.1	587	588	1.001704	0.898273044

Use $WN=2.4\mu\text{m}$ and $WP=2.1\mu\text{m}$ with a ratio of .897.

In reality I would have stopped at the third iteration, but I wanted an accurate ratio.

Note: The ratio is quite different. The error in in the KP and KN values which change with width!

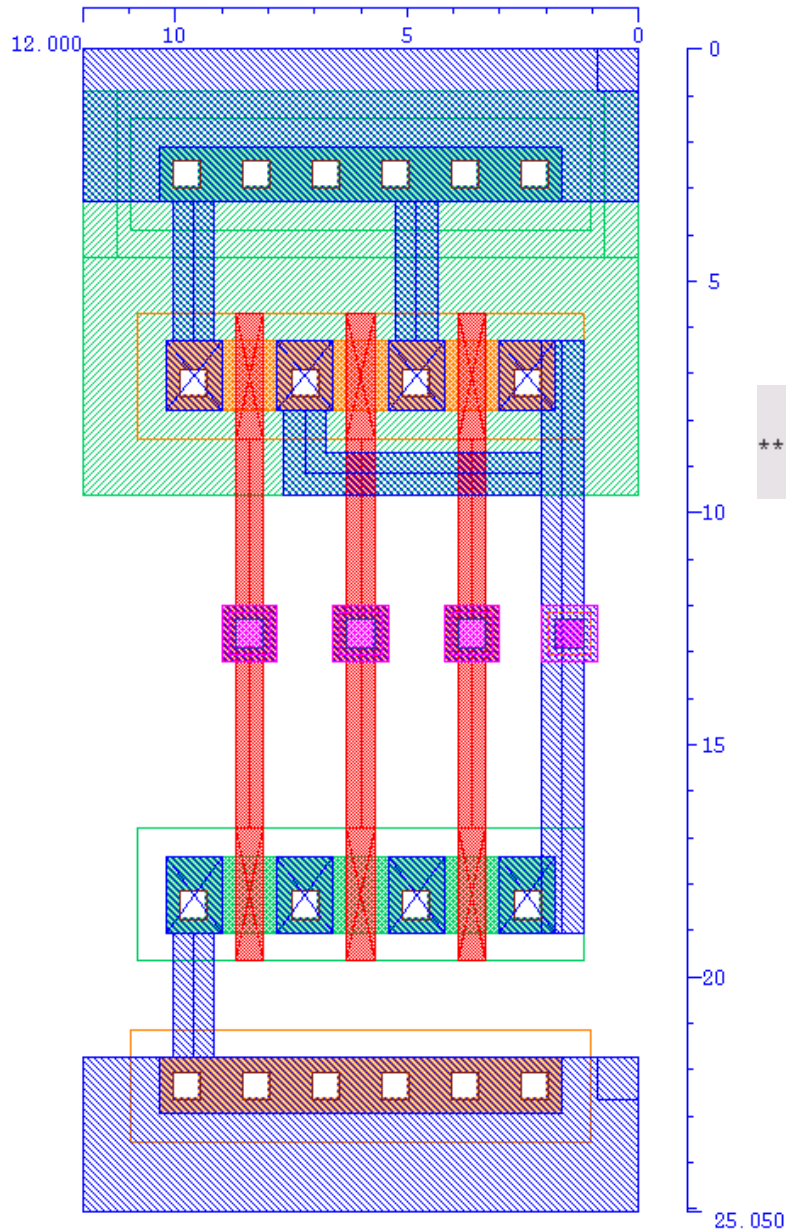
We can use $WN=1.65\mu\text{m}$ and $WP=1.5\mu\text{m}$ which is closer to our ideal ADP.

Finish the design

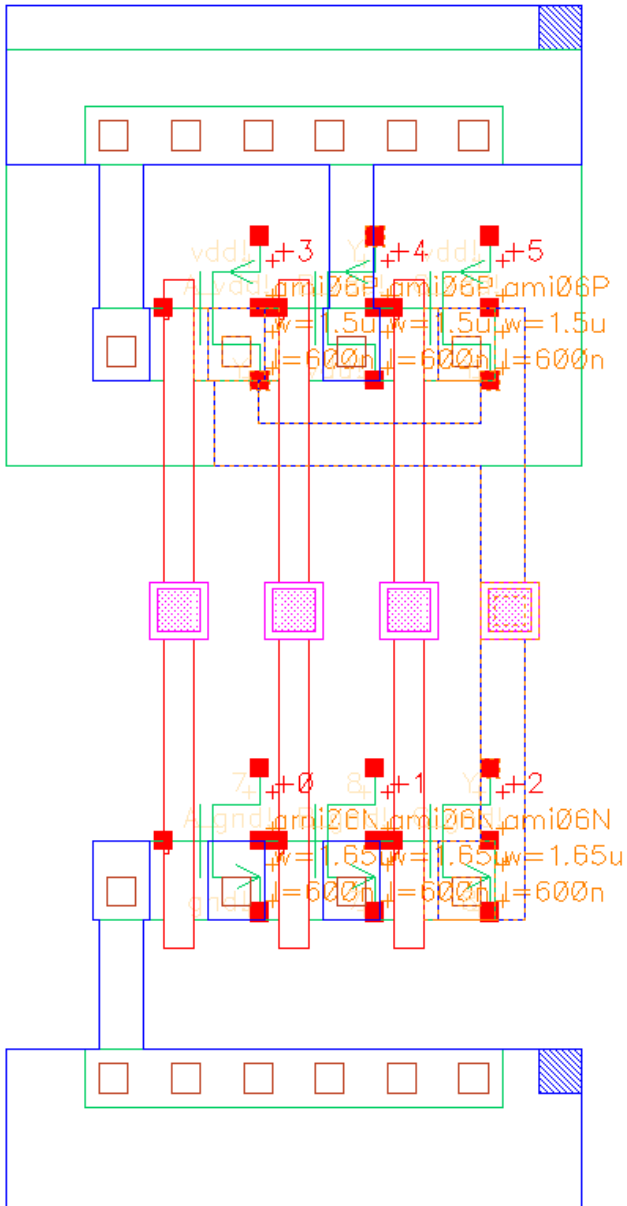
- We go back into the schematic and enter in WN and WP.
- We layout the NAND3
- DRC
- LVS
- Post Extraction simulation
- Noise Analysis

Final Layout

```
completed ....Wed Jun 11 20:18:32 2003  
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00  
***** Summary of rule violation for cell "nand3 layout" *****  
Total errors found: 0
```



Final Extracted



```
Extraction started.....Wed Jun 11 20:22:06 2003  
completed ...Wed Jun 11 20:22:07 2003  
CPU TIME = 00:00:01 TOTAL TIME = 00:00:01  
***** Summary of rule violation for cell "nand3 layout" *****  
Total errors found: 0
```

LVS Report

```
@(#)SCDS: LVS version 4.4.6 06/01/2001 20:24 (cds11612) $
```

```
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...
```

```
Net-list summary for /home/dparent/cell/LVS/layout/netlist
```

count	
8	nets
6	terminals
3	pmos
3	nmos

3 PMOS and 3 NMOS

```
Net-list summary for /home/dparent/cell/LVS/schematic/netlist
```

count	
8	nets
6	terminals
3	pmos
3	nmos

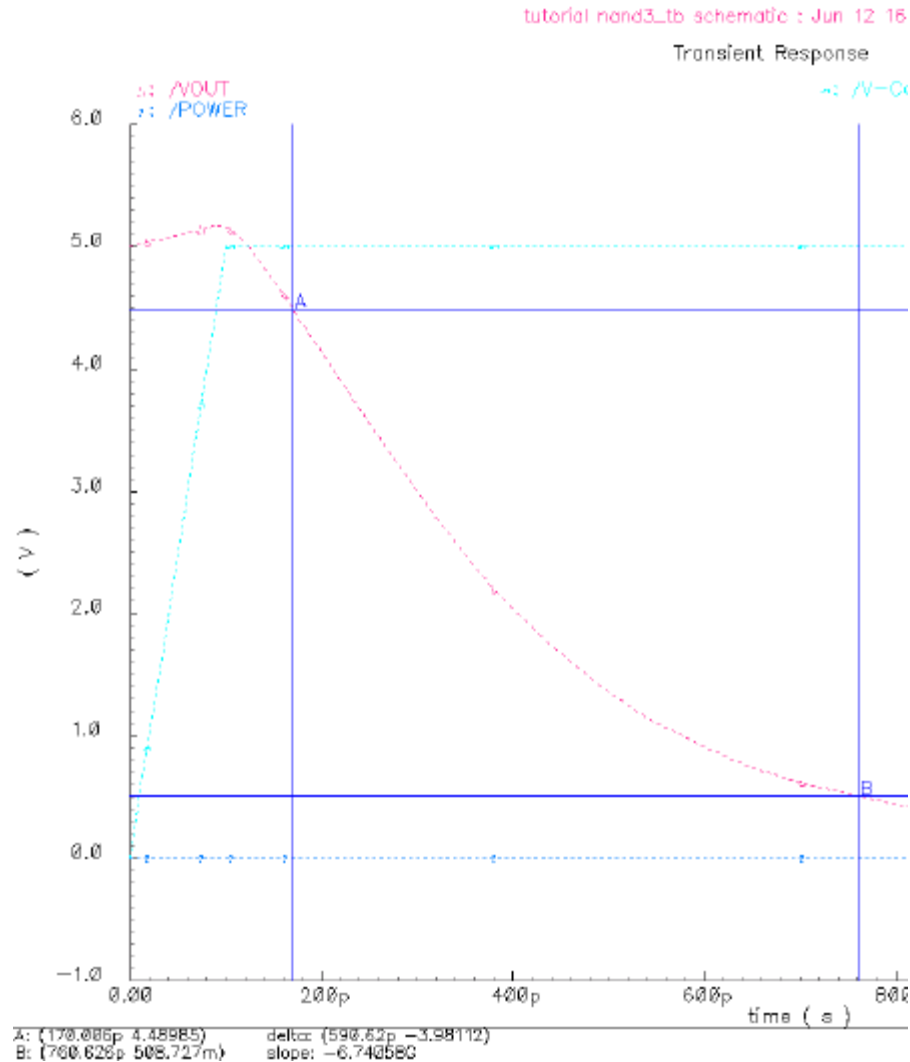
```
Terminal correspondence points
```

1	A
2	B
3	C
4	Y
5	gnd!
6	vdd!

NETLISTS MATCH

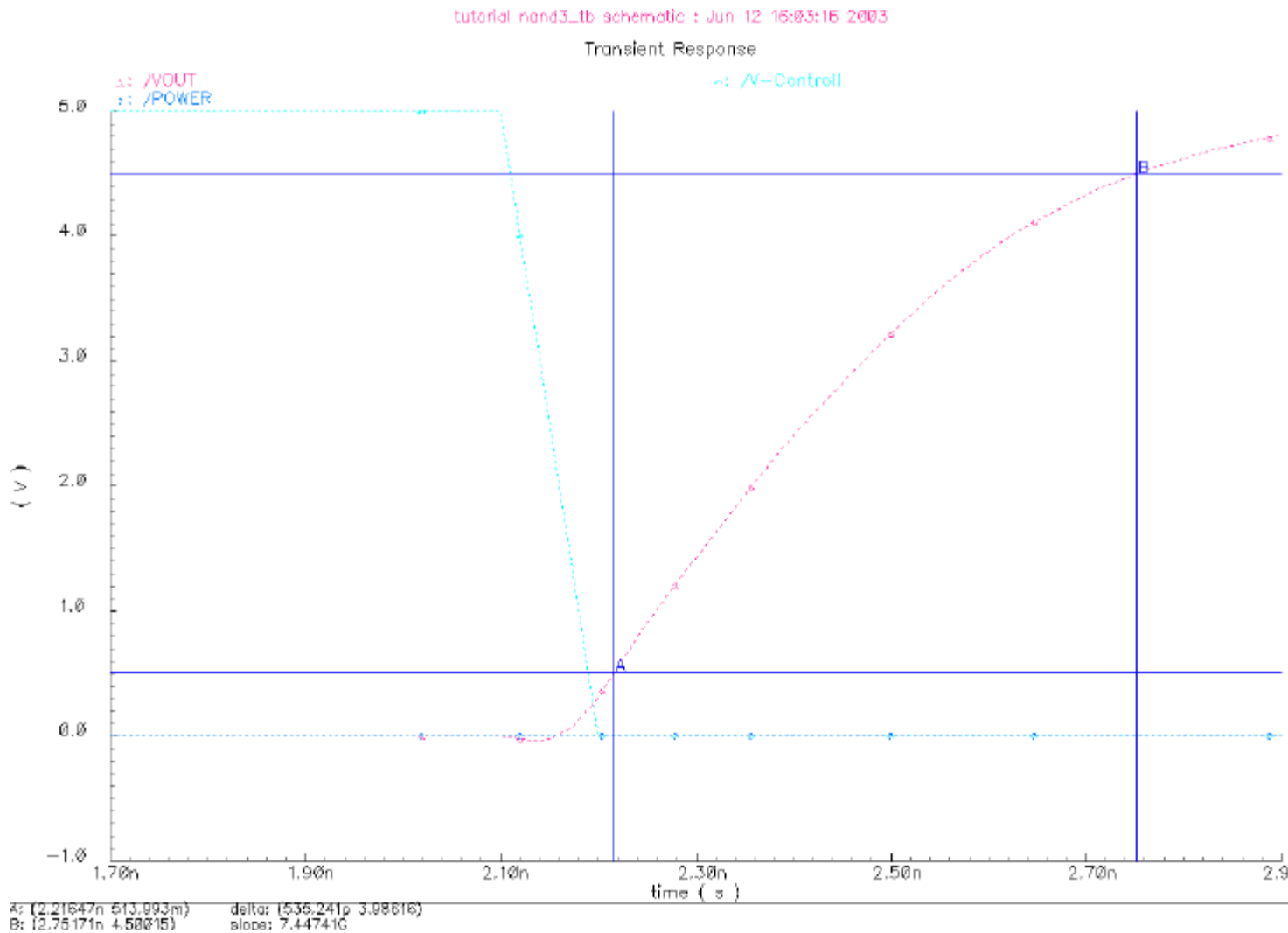
```
The net-lists match.
```

Post Extraction Simulation



Fall
Time

Post Extraction Simulation

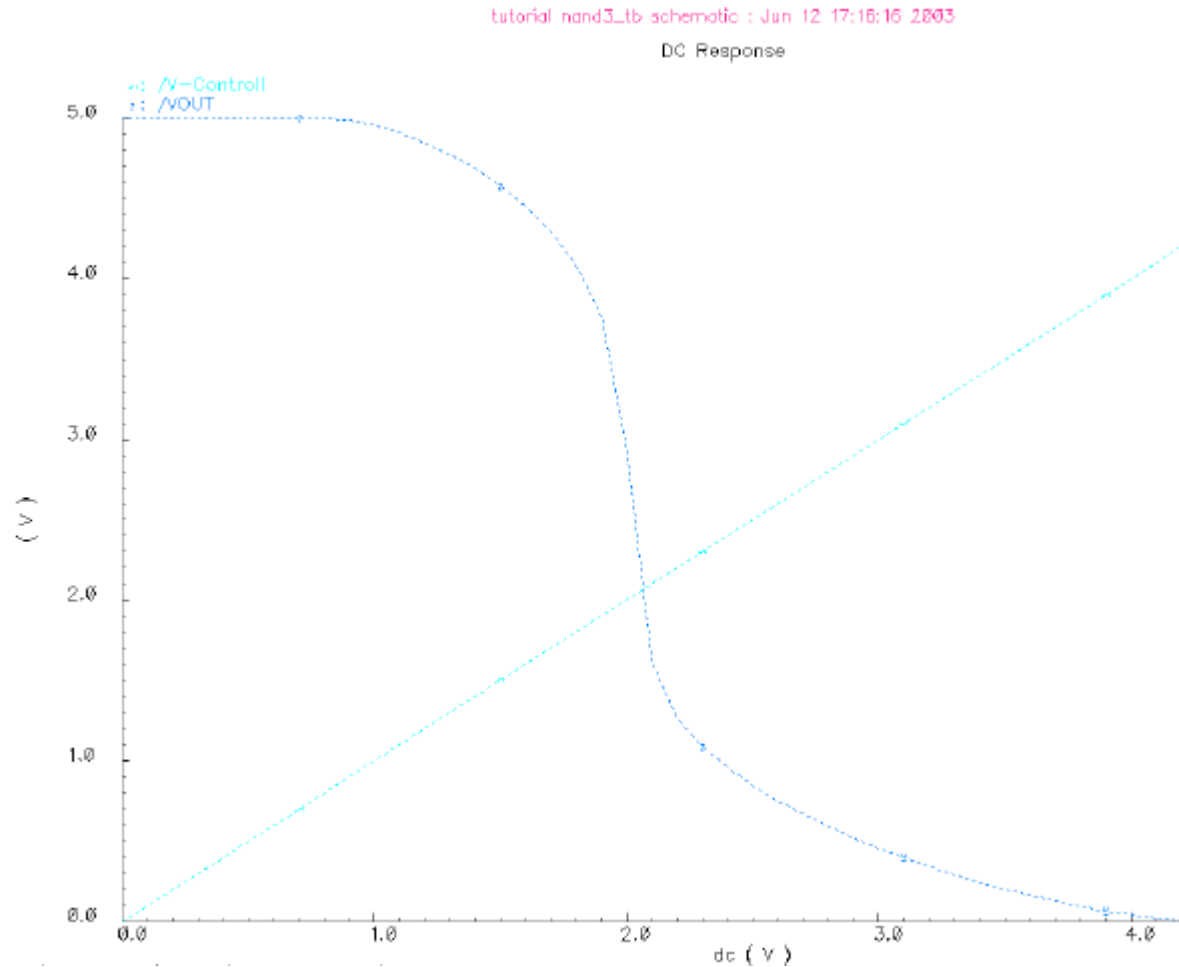


Rise
Time

Are we done?

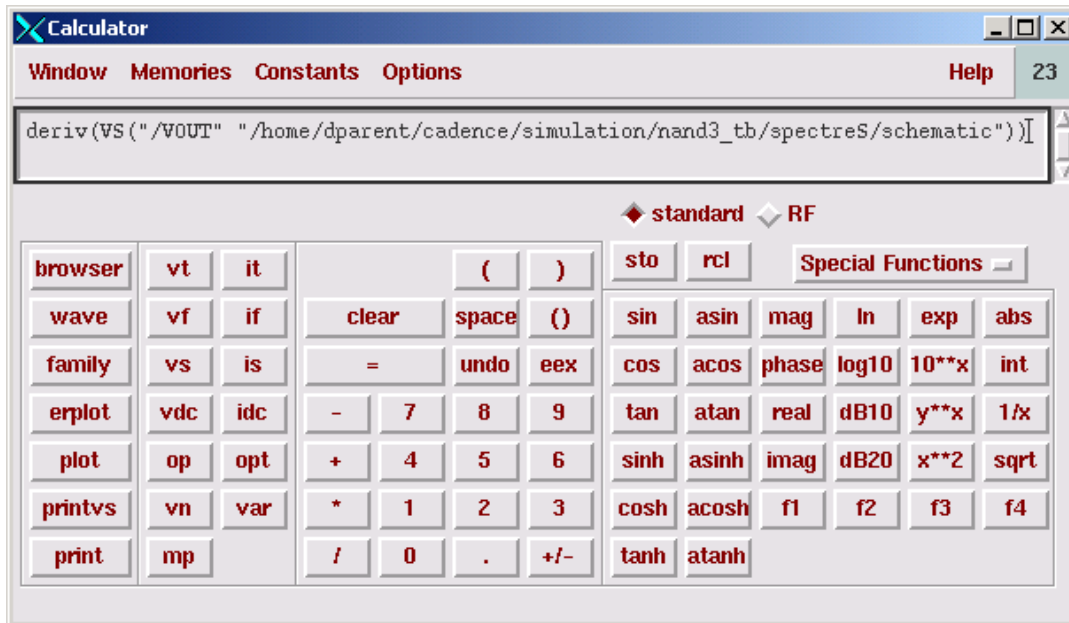
- Depends
 - If 10% error between the rise and fall times is ok then yes.
 - If the error is unacceptable then no.
- What do we do?
 - The rise time is too fast compared to the fall time. We can not decrease WP so we increase WN by the $1/(.896 * T_{rise}/T_{fall})$

Noise Analysis (DC Sweep)



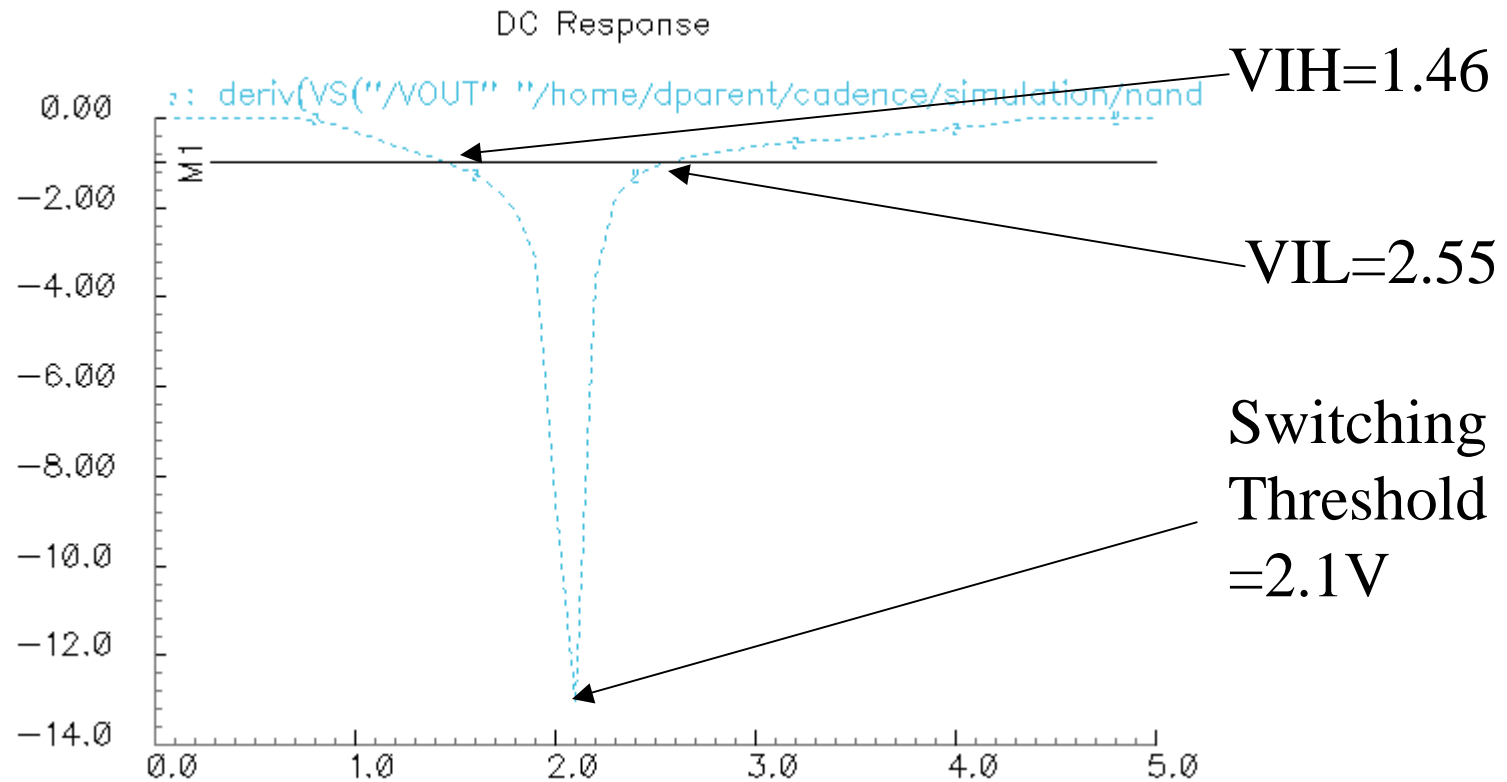
Switching threshold V_{OH} V_{OL}

We can find the switching threshold, V_{OH} and V_{OL} by taking the derivative of the DC sweep. The maximum of the derivative will be the switching threshold and where the derivative crosses the -1 line are V_{OL} and V_{OH}.



Derivative of DC Sweep

tutorial nand3_tb schematic : Jun 12 17:16:16 2003

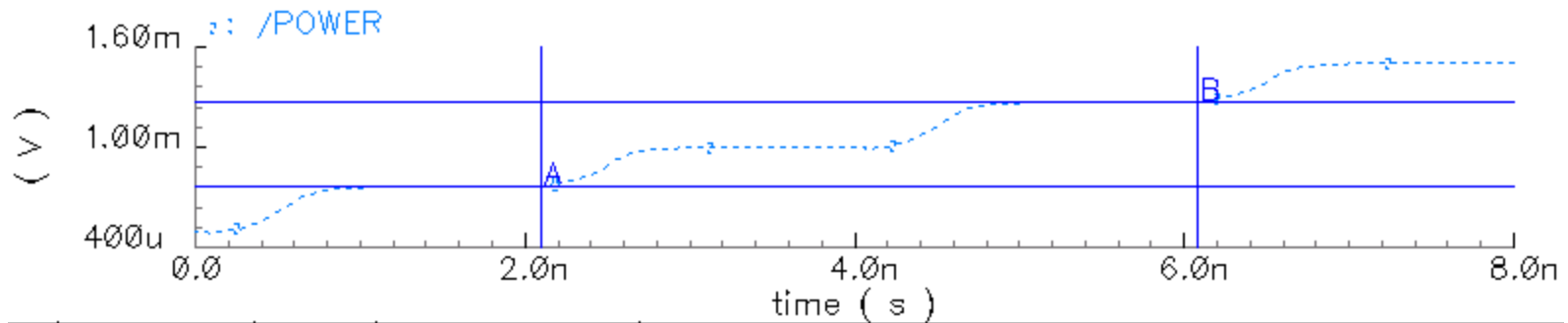


Power

There are
4 NANDs
switching in the
TB so
 $P=505\mu\text{W}/4$

tutorial nand3_tb schematic : Jun 12 17:07:48 2003

Transient Response



A: (2.1n 765.318u) delta: (3.98147n 505.156u)
B: (6.08147n 1.27047m) slope: 126.877K

Design summary

- $W_N=1.8\mu\text{m}$, $W_P=1.5\mu\text{m}$ $L_P=L_N=.6\mu\text{m}$
- Rise and fall times equal 533ps with in 2% error.
- Propagation delays equal 278ps within 1% error
- Switching threshold=2.1V
- $V_{IH}=1.46\text{V}$, $V_{IL}=2.55\text{V}$
- Area= $306\mu\text{m}^2$ (VDD and GND line wider to prevent electro migration failure and IR loss.)
- Power= $126\mu\text{W}$

Conclusions

- Setting up the test vectors for “worst case” requires special attention to which capacitances are being charged and discharged.
- Hand calculations were very accurate for finding the optimum widths.
- Hand calculations were not as accurate for designing symmetric rise and fall times.
 - We could back fit our C and D parameters for future hand calculations.

$$C := \frac{W_N \cdot t_f}{C_{LOAD} \cdot 3 \cdot L_N} \quad C = 1.16 \times 10^4 \Omega$$

$$D := \frac{W_P \cdot t_r}{C_{LOAD} \cdot L_P} \quad D = 2.98 \times 10^4 \Omega$$

Design Flow for a generic Static CMOS circuit for optimum width

- Start with W_N or $W_P=1.5\mu\text{m}$
- Use new C and D and the equivalent inverter technique to solve for the width that will be larger than $1.5\mu\text{m}$.
- Set up a test bench that is for the worst case.
 - Have the controlling voltage at the bottom of an NMOS stack or at the top of a PMOS stack.
- Iteratively solve for W_P or W_N while holding W_N or W_P constant until rise and fall times are within 10%. and then complete normal design flow tasks.

What would happen if....

- We made the finger spaces closer on the nmos, thus reducing capacitance?
 - DC no change (Capacitance does not matter with a DC analysis.)
 - Propagation delay changes to 289ps
 - Rise and fall time go to 589ps
 - Power goes to 137uW