Spice parameters of diodes

EE221

D. W. Parent

There are 4 DC spice parameters for a diode

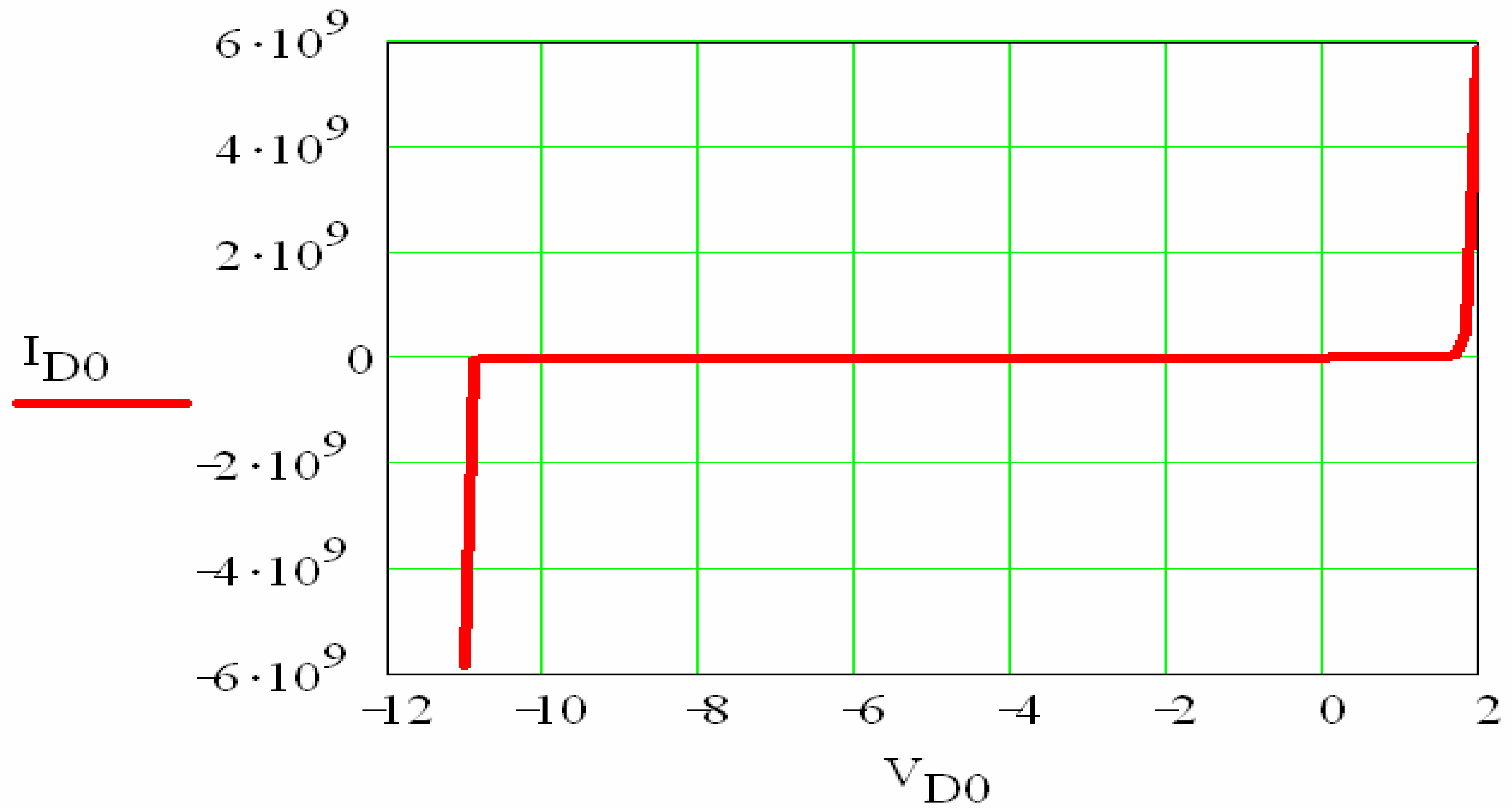
IS Saturation current (Given in Amps)
N Emission Coefficient (No Units)
RS Parasitic resistance (Given in Ω)
BV Breakdown Voltage (Given in Volts)
IBV Breakdown Current (Given in Amps)

GMIN is a small resistance
To prevent a value of zero current form Flowing. Usually set to 10^{-12}S

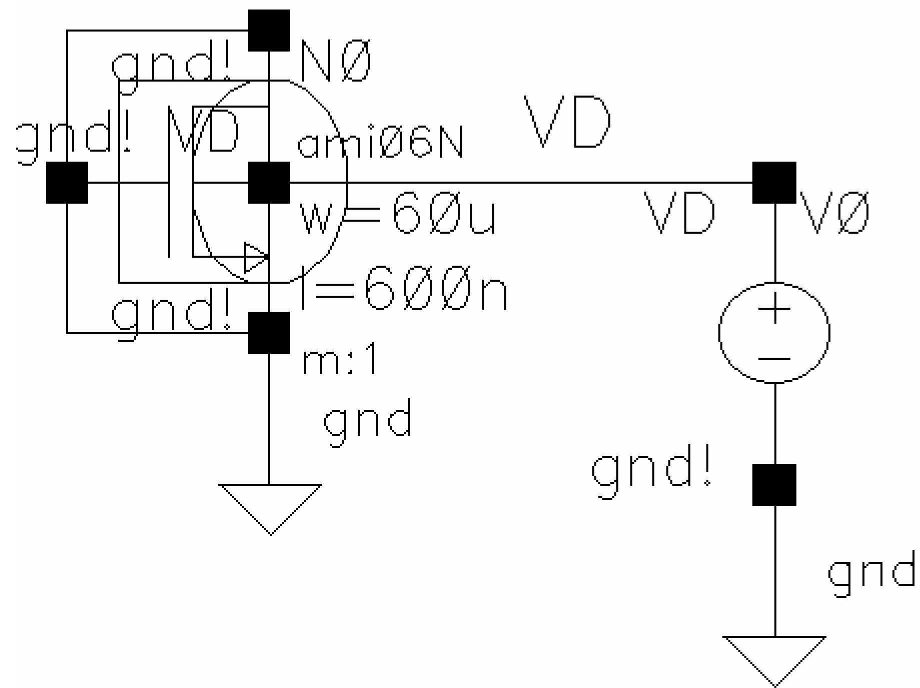
$$I_s := 1 \times 10^{-7}$$
$$n := 2$$
$$r_s := 100$$
$$V_t := .0259$$
$$BV := 10$$
$$G_{min} := 1 \times 10^{-9}$$
$$IBV := I_s \cdot \frac{BV}{V_t}$$

$$I_{D0_i} := \begin{cases} \left[I_s \cdot \left(e^{\frac{V_{D0_i}}{n \cdot V_t}} - 1 \right) + V_{D0_i} \cdot G_{min} \right] & \text{if } V_{D0_i} > -BV \\ (-IBV) & \text{if } V_{D0_i} = -BV \\ \left[-I_s \cdot \left[e^{\frac{-\left(BV + V_{D0_i}\right)}{V_t}} - 1 + \frac{BV}{V_t} \right] \right] & \text{if } V_{D0_i} < -BV \end{cases}$$

Full Diode Response

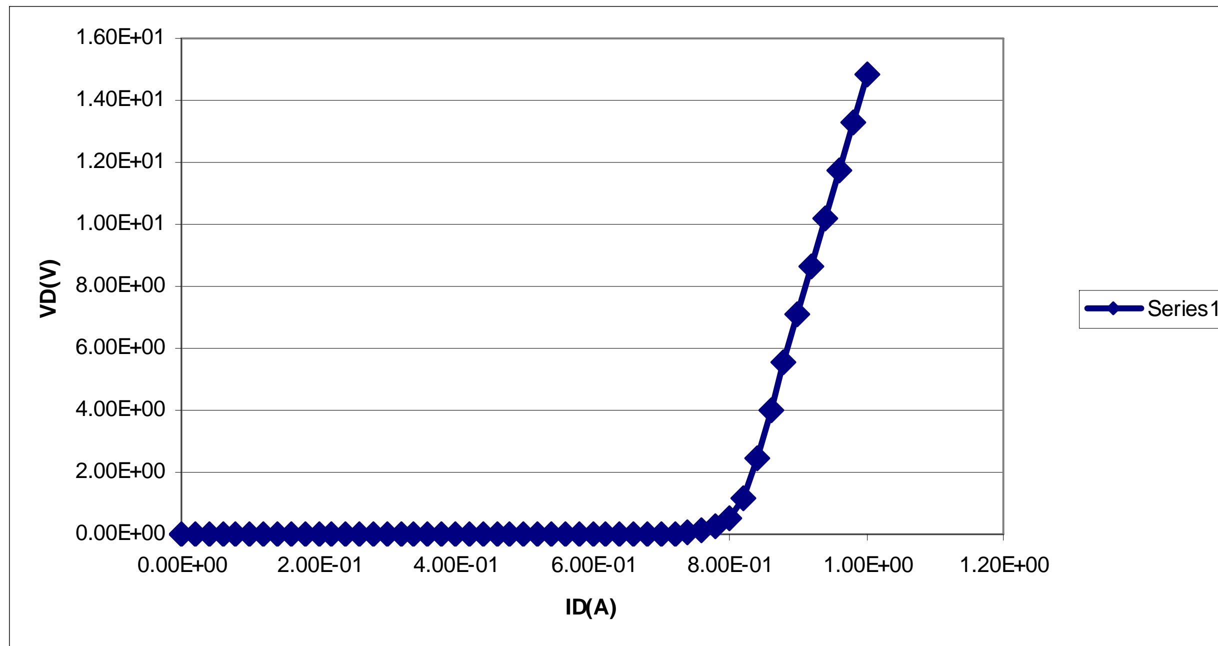


Test the diode of a NMOS

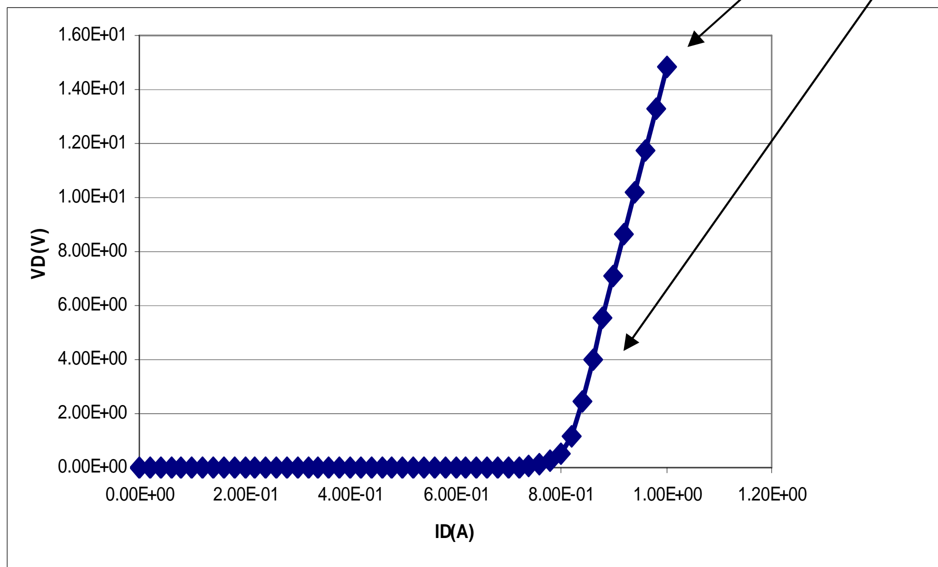


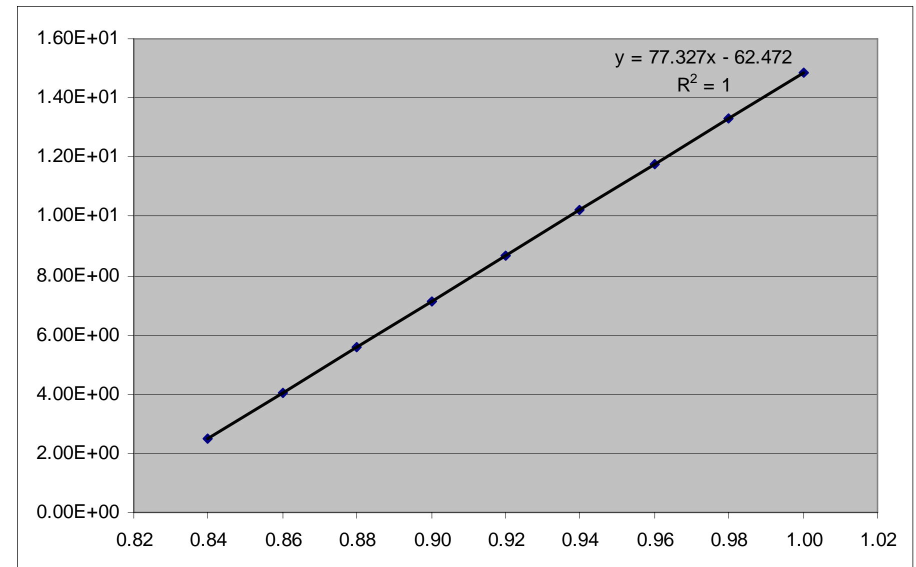
Note there are two diodes being tested.

Forward Bias Diode
Linear

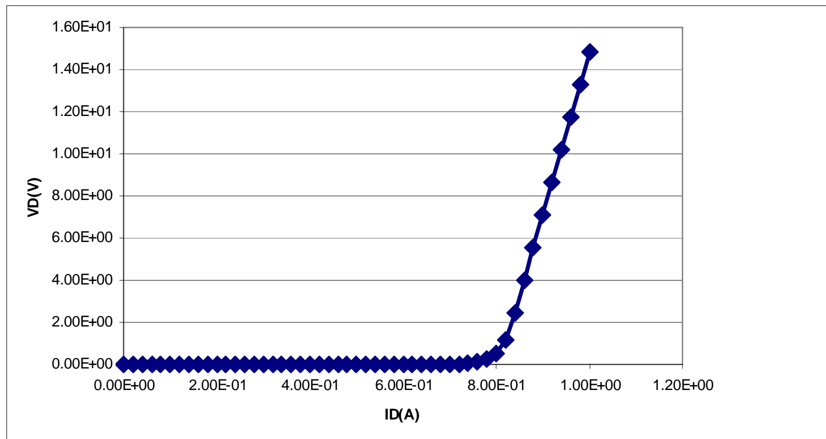


Take the RS value from the Linear part of the diode curve



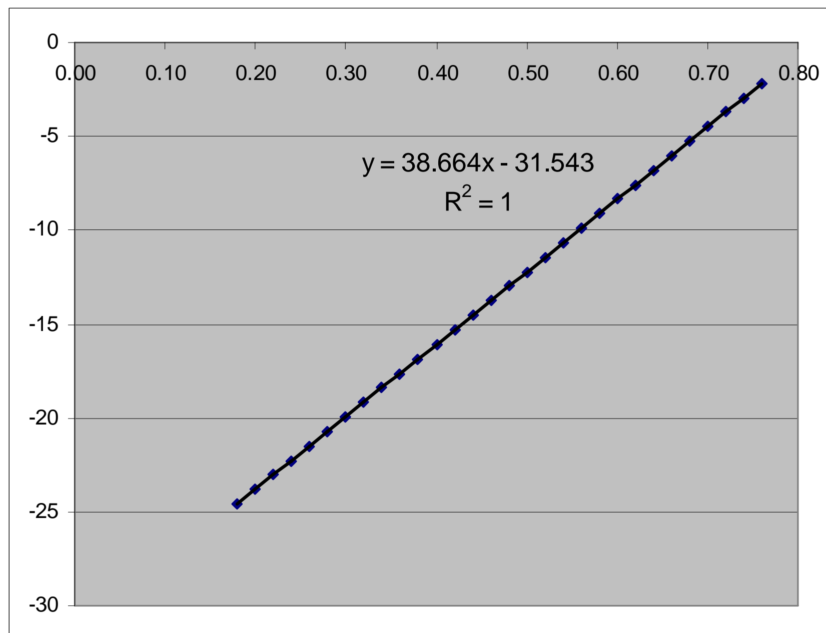


Forward Bias Log Scale (RS position omitted)



$$I_S := e^{-31.543} \quad I_S = 2 \times 10^{-14}$$

$$n := \frac{1}{38.664 \cdot .0259} \quad n = 0.999$$



Do not use linear
Region of Diode
Or too close to 0V.
The RS value and GMIN
Will skew the results.

Reverse bias breakdown

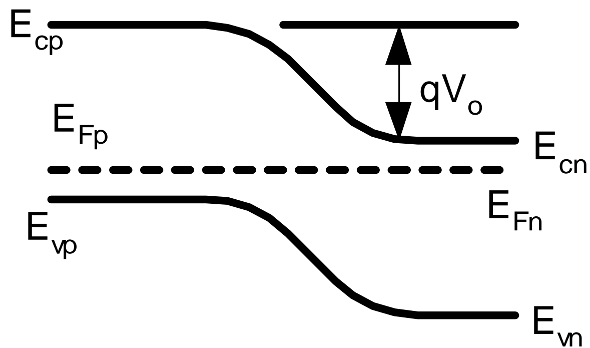
- Under reverse bias a pn junction exhibits a small voltage independent current until a critical voltage is reached V_{br}. If the bias voltage exceeds V_{br} the current increases dramatically.
- If biased properly with a current limiting diode, you can operate in reverse breakdown mode with out damaging the diode.

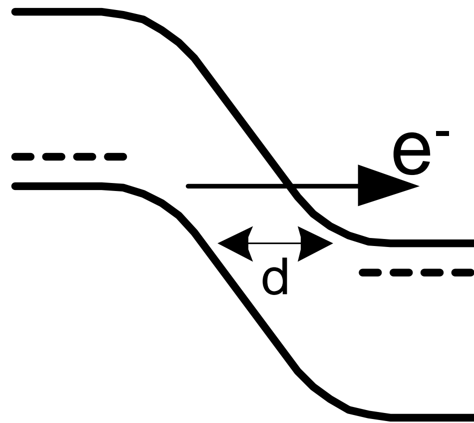
Reverse Breakdown

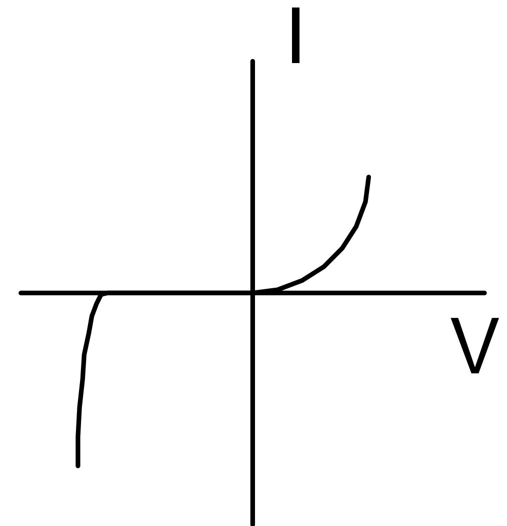
- Zener Breakdown
  - This effect applies to heavily doped junctions (p+, n+). This is a low voltage effect.
  - Barrier is thin due to high abrupt doping
  - When the reverse bias voltage is large enough, electrons can tunnel to the p-side, and holes can tunnel to the n-side (section 2.4.4)
  - Reverse bias of a p+/n+ junction
    - leads to large electric field (10^6V/cm)
    - leads to covalent electrons being "ripped away"

Reverse Breakdown

- Zener Breakdown





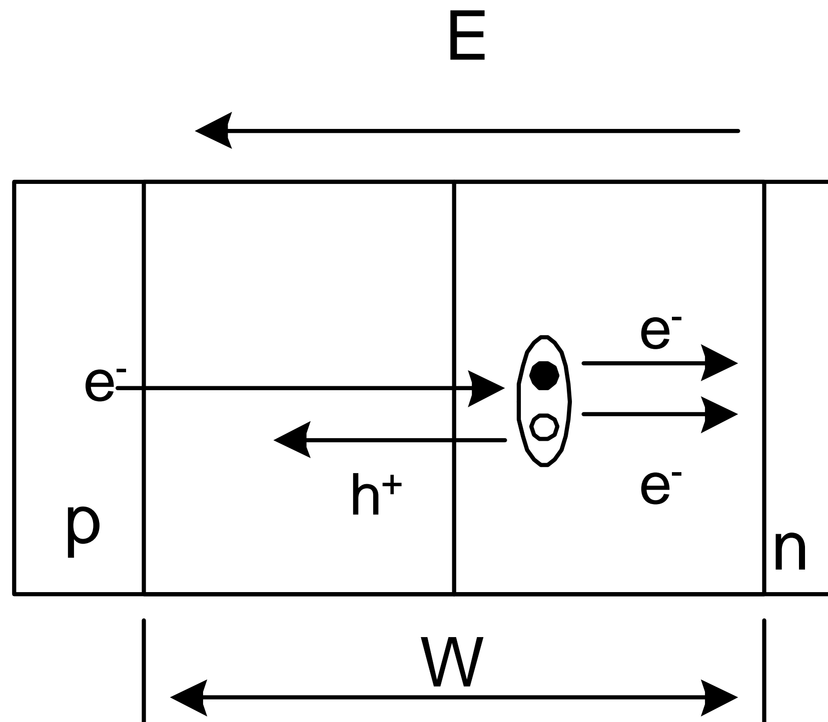


Reverse Breakdown

- Avalanche Breakdown
  - Lightly doped junctions, tunneling can not occur
    - W increases with reverse bias.
  - Impact ionization
    - A carrier can be accelerated by a high electric field with enough kinetic energy to knock an electron out of the lattices covalent bond and make an EHP. One carrier can cause many carriers to be created.
    - To design V_{br}, use figure 5-22 on page 190.

Reverse Breakdown

- Avalanche Breakdown



PE

An abrupt p-n junction has the following properties at 300K:

p side	n side
$Na=2x10^{20}cm^{-4}$	$Nd=1x10^{15}cm^{-3}$
$\tau_n=.1x10^{-6}s$	$\tau_p=10x10^{-6}s$
$\mu_p=200\ cm^{2/}Vs$	$\mu_n=1300cm^2/Vs$
$\mu_n=700$	$\mu_p=450$
$A=10^{-4}cm^2$	$A=10^{-4}cm^2$

Find the breakdown voltage if the diode is made of Ge.

Find the breakdown voltage if the diode is made of Si, and

Nd is changed to $1x10^{19}cm^{-3}$.

Transient and AC conditions

- Time variation of stored charge.
  - Time dependant continuity equation
  - p+/n diode (figure 5-20 page 168)

$$\mathrm{x_n}(0) \rightarrow \text{all hole current}$$

$$\mathrm{x_n}(\infty) \rightarrow \text{no hole current}$$

$$\mathrm{i(t)} = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt}$$

$$Q_p(t) = I\tau_p e^{-t/\tau_p}$$

Transient and AC conditions

- Time variation of stored charge.
  - Quasi-steady state approximation

$$v(t) = \frac{kT}{q} \ln\left(\frac{I\tau_p}{qAL_p p_n} e^{-t/\tau_p} + 1 \right)$$

- To decrease switching time
  - decrease n-type region to less than L_p or decrease τ_p (Au or Pt doping)

Transient and AC conditions

- Reverse recovery transient
  - This is a switching characteristic or large signal analysis (large deviations from a reference point).
  - Assume a p+/n diode biased with resistor R, driven by a square wave (+E to -E with period T)
    - Forward bias: For large E most of the voltage drops across the resistor and the current is given by I_f=E/R.

Transient and AC conditions

- Reverse recovery transient
  - Sudden application of reverse bias:
    - Current initially becomes $i=I_r=-E/R$ because the stored charge in the junction can not be removed instantly, therefor the voltage can not be changed instantly.
    - Once all the minority charge is gone the junction will become reversed biased and thus act like a large resistance because only the I_{gen} current is flowing.

Transient and AC conditions

- Reverse recovery transient
  - Sudden application of reverse bias:
    - The time it takes for the junction voltage to become zero is t_{sd}. (figure 5-21 page 171)

$$t_{sd} = \tau_p \left[erf^{-1}\left(\frac{I_f}{I_f + I_r} \right) \right]^2$$

with the quasi-steady state approximation:

$$\mathrm{t_{sd}} = \tau_p \ln\left(1 + \frac{I_f}{I_r} \right)$$

Transient and AC conditions

- Capacitance of p-n junctions
  - This is for small signal analysis. Assume a bias point and that the applied time varying voltage or current does not perturb the diode’s G and C very far from their bias values.

Transient and AC conditions

- Junction capacitance:
  - Dominant under reverse bias, due to separation of positive and negative charges.

$$W = \left[\frac{2\varepsilon(V_o - V)}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{\frac{1}{2}}$$

$$|Q| = qA \frac{N_a N_d}{N_a + N_d} W$$

$$C_j = \left| \frac{dQ}{d(V_o - V)} \right| = \frac{A}{2} \left[\frac{2q\varepsilon}{(V_o - V)} \frac{N_a N_d}{N_a + N_d} \right]^{\frac{1}{2}}$$

Transient and AC conditions

- Storage capacitance:
  - Dominant under forward bias, due to the voltage lagging behind the current.

$$G_s = \frac{dI}{dV} = \frac{q}{kT} I$$

$$C_s = \frac{dQ_p}{dV} = \frac{q}{kT} I \tau_p$$

$$i(ac) = G_s v(ac) + C_s \frac{dv(ac)}{dt}$$

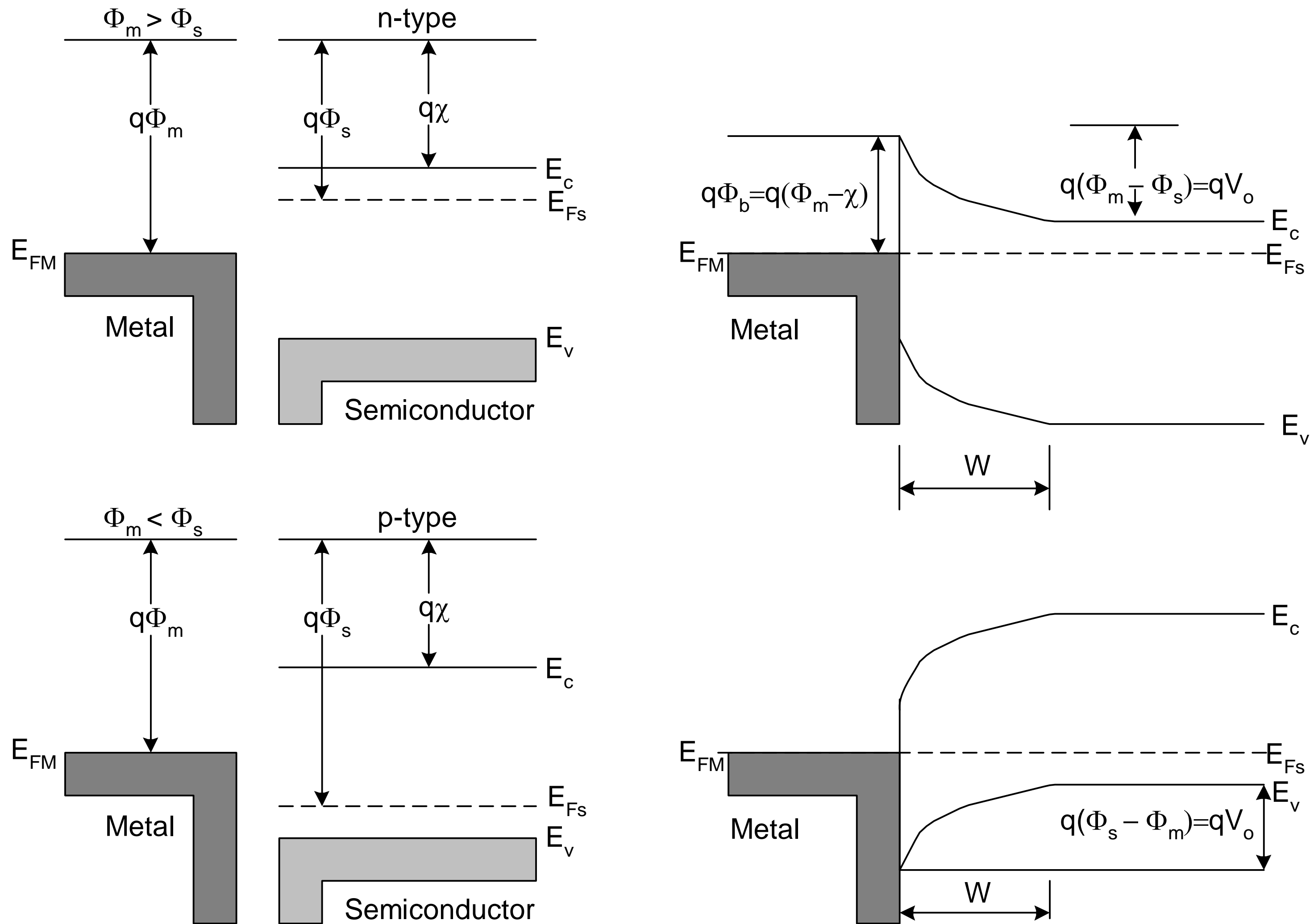
Example Cj, Cs

- For the ZnSe example calculate Cj at –2, 0, and 2 volts.
- For the ZnSe example calculate Cs at –2, 0, and 2 volts.
- Minority lifetimes are 1ns.

Schottky barriers

- Diode like behavior can be mimicked by applying clean metal to a clean semiconductor.
  - Easy to do and faster switching times can be realized.
- n-type
  - Semiconductor bands bend up causing a more positive region near the interface, which attracts electrons from the metal to the interface interface.
- p-type
  - Semiconductor bands bend down causing a more negative region near the interface, which attracts holes from the metal to the interface.

Schottky barriers



Rectifying contacts

- Apply a forward bias to the Metal of the M/S(n) diode and the contact potential is reduced by V_o-V
  - Allows electrons to diffuse into metal.
- Apply a forward bias to the Semiconductor of the M/S(p) diode and the contact potential is reduced by V_o-V
  - Allows holes to diffuse into metal.

Rectifying contacts

- Apply a reverse bias to the Metal of the M/S(n) diode and the contact potential is increased by V_o+V_r.
  - Electrons have to overcome a voltage independent barrier to diffuse into metal.
- Apply a reverse bias to the Semiconductor of the M/S(p) diode and the contact potential is reduced by V_o+V_r.
  - Holes have to overcome a voltage independent barrier to diffuse into metal.

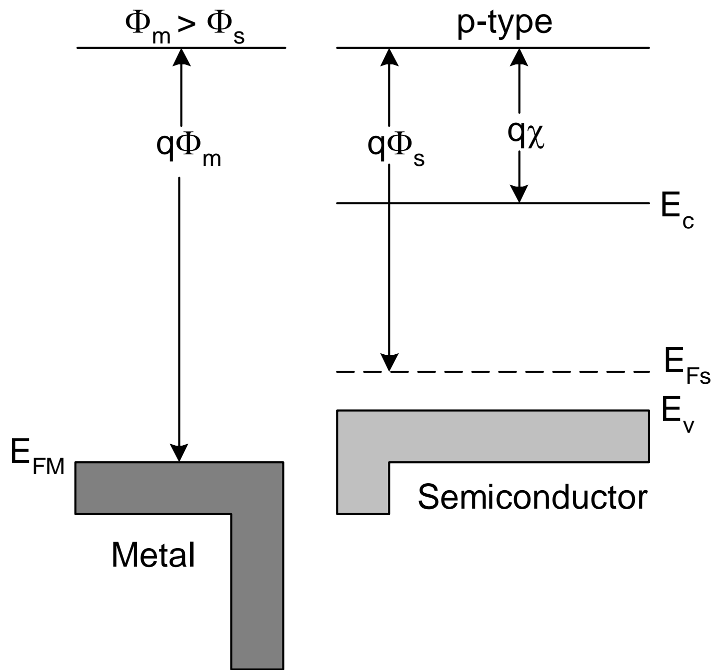
Rectifying contacts

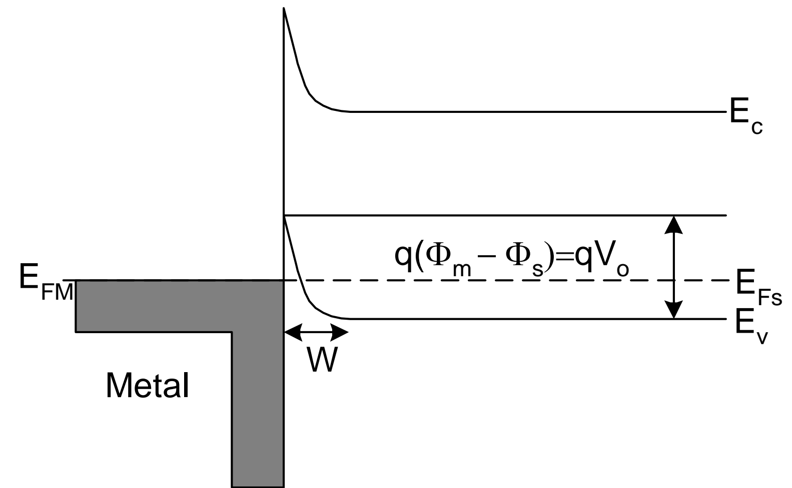
- Current flows primarily by **majority** carriers is both cases.
- Very little charge storage occurs, which leads to **fast switching speeds**.

Ohmic contacts

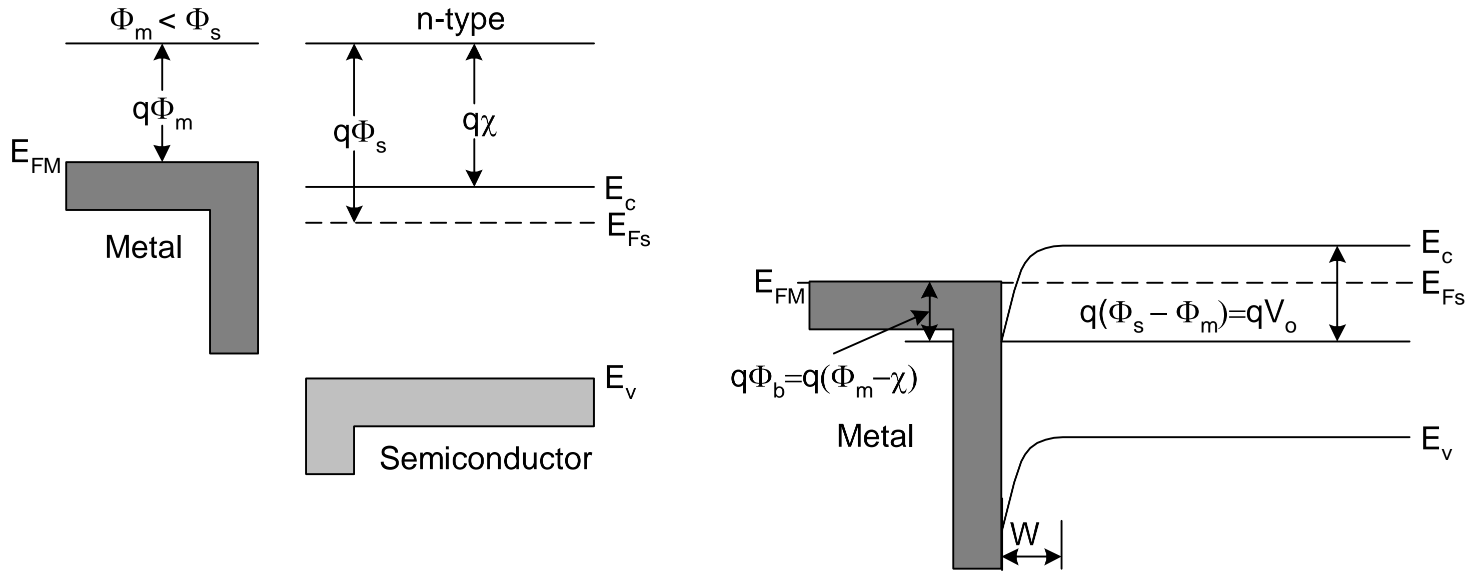
- Metal/semiconductor ohmic contacts
  – linear near the origin, non-rectifying
- Two methods of fabrication
  – Choose a metal with a workfunction that aligns the fermi levels with majority carriers. (Al for p-type Si, Au for n-type Si
  – Dope the semiconductor heavily so that W is very thin so that tunneling occurs (Al on p^+ or n^+ Si)
  – Heavy doping all ways improves ohmic behavior.

Ohmic contacts





Ohmic contacts



Real Schottky barriers

- In Si, there is a thin oxide in between the metal and semiconductor.
- Surface states arise from the crystal ending
  - This can pin the fermi level to midgap in GaAs
- If a metal semiconductor junction is alloyed the interface is blurred between metal/metal-semiconductor/semiconductor.
- Contact design is very dependant on your process.