

EE221

MOS CAP

# MOSFET

- Metal Insulator Semiconductor (MIS) transistor
- Insulated Gate Field Effect Transistor (IGFET)
- Majority Carrier Device.

# Applications of a MOS Capacitor

- DRAM storage
- Loop Filter for PLL
- CCD
- Process Monitor
  - Substrate doping, Oxide thickness, Leakage,  $V_T$

# Fabrications

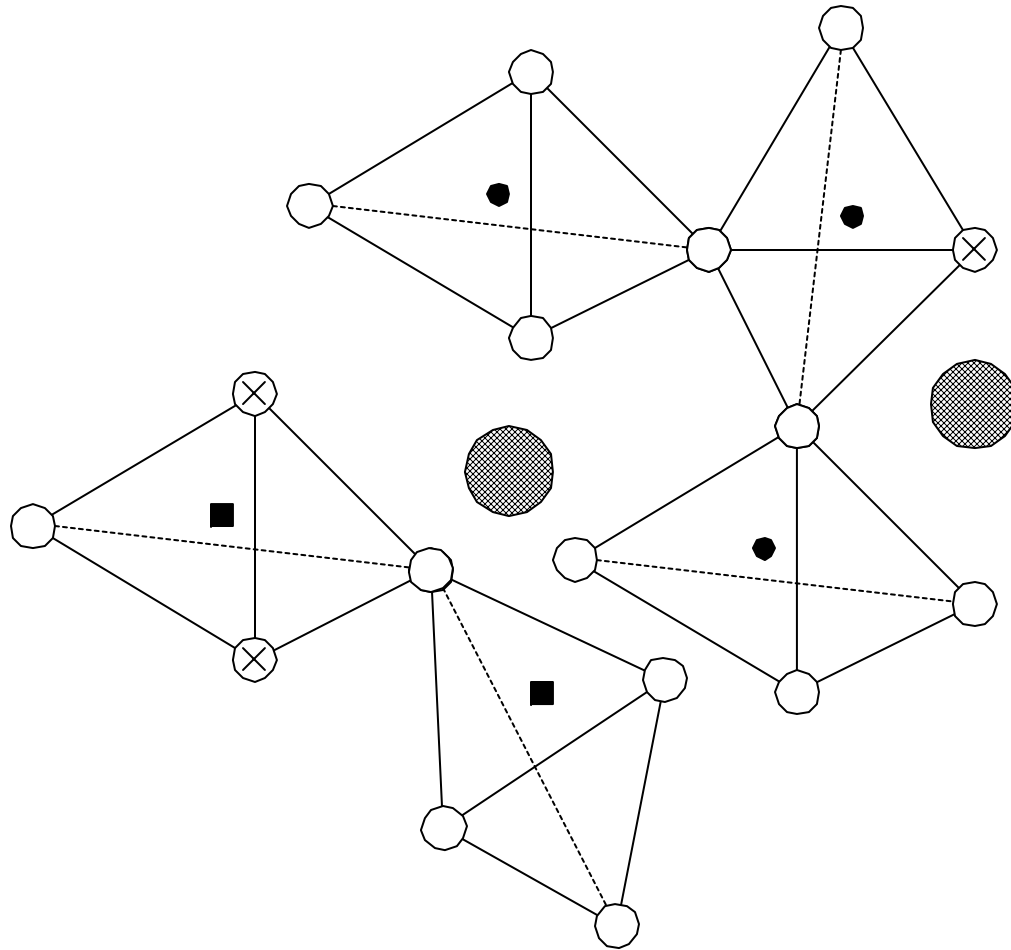
# Silicon dioxide






- What is  $\text{SiO}_2$ ?
- What is  $\text{SiO}_2$  used for?
- Advantages and Disadvantages of  $\text{SiO}_2$
- How is it grown?
  - Dry
  - Wet
- Numerical Examples

# What is SiO<sub>2</sub>?

- Two forms
  - Single crystal (quartz)
  - Amorphous
- We are interested in Amorphous SiO<sub>2</sub>
  - Random three dimensional network of SiO<sub>2</sub> constructed from polyhedra of oxygen ions.
  - This material is more porous than Quartz (density of 2.15-2.25g/cm<sup>3</sup> compared to 2.65 25g/cm<sup>3</sup> )

# What is SiO<sub>2</sub>?



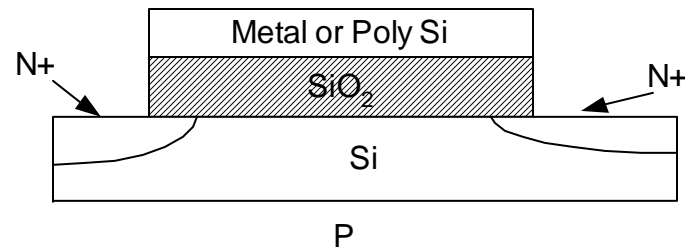
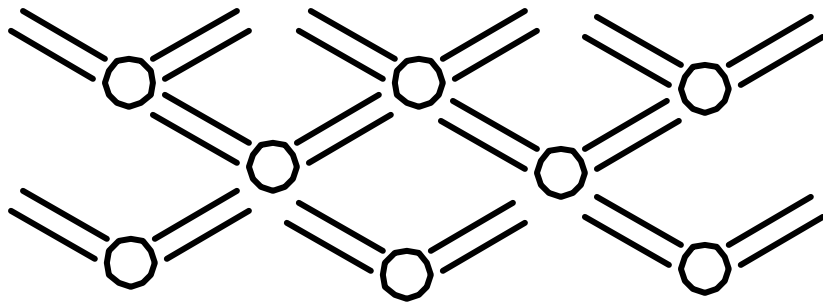
-  Network modifier
-  Nonbridging oxygen
-  Silicon
-  Network former
-  Bridging oxygen

The O-Si-O Bond angle is 109°

Tetrahedral distance between Si and O ions is 1.6Å

# What is SiO<sub>2</sub> used for?

- MOS Metal Oxide Semiconductor
- Device passivation
  - Combines with dangling bonds to reduce surface states

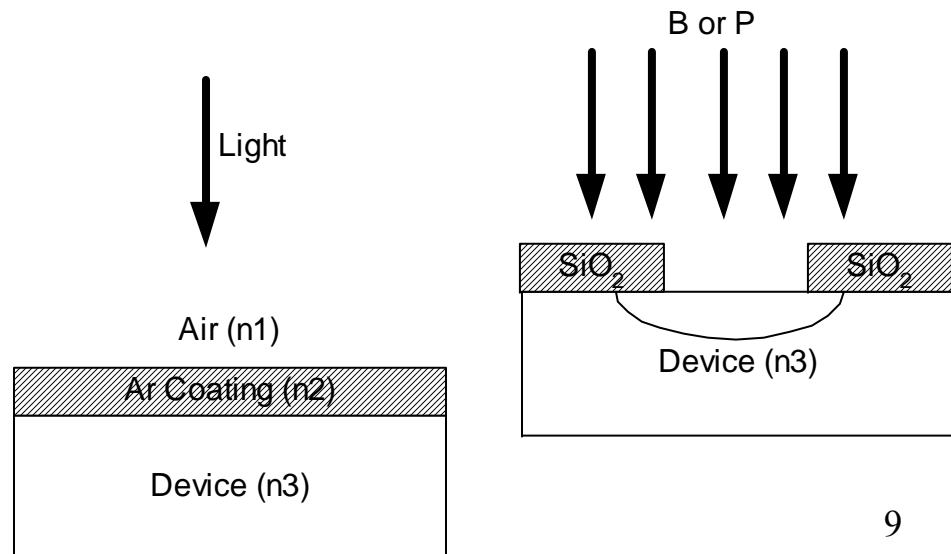


# What is SiO<sub>2</sub> used for?

- Diffusion Masks
  - Block the diffusion of B and P for example
- Antireflective coating for Photodevices

$$n_2 = \sqrt{n_1 n_3},$$

$$\text{thickness} = \frac{\lambda}{4n_2}$$



# Advantages and Disadvantages of $\text{SiO}_2$

- CMOS digital logic gates use little power when not switching logic state, thus high levels of integration are possible because the standby power consumption is low.
- $\text{SiO}_2$  is a native film that is quite easy to grow. All that is required is heat and oxygen or steam.

# Advantages and Disadvantages of $\text{SiO}_2$

- $\text{SiO}_2$  consumes Si while growing. 44% of the  $\text{SiO}_2$  layer comes from the original Si.
  - This leads to a non-planer structure after each oxidation step.
- Due to the large increase in volume there is  $2-4 \times 10^9$  dyn  $\text{cm}^{-1}$  of compressive strain.
  - This causes dislocations.
- Oxidation-Induced Stacking Faults (these can be removed by a high temp treatment).

# Advantages and Disadvantages of $\text{SiO}_2$

- The large dielectric constant leads to larger capacitance values for a given thickness (compared to silicon nitride).

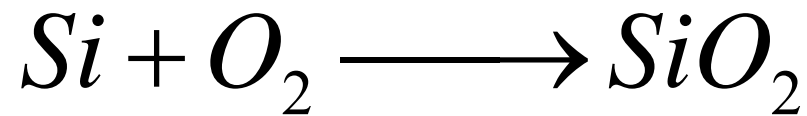
# How is it grown?

- The oxidizing species must diffuse through the SiO<sub>2</sub> layer that has already grown. This leads to a linear regime of growth and a parabolic regime of growth. Given by the equation:

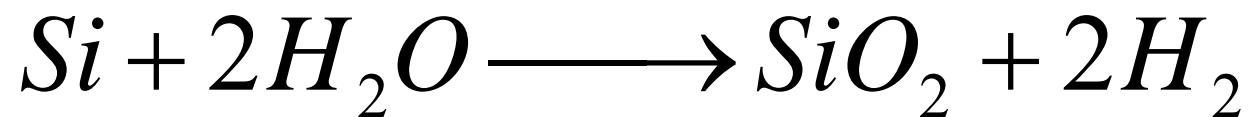
$$X^2 + A(\mu m)X = B(\mu m^2 / hr)t(hr)$$

# How is it grown?

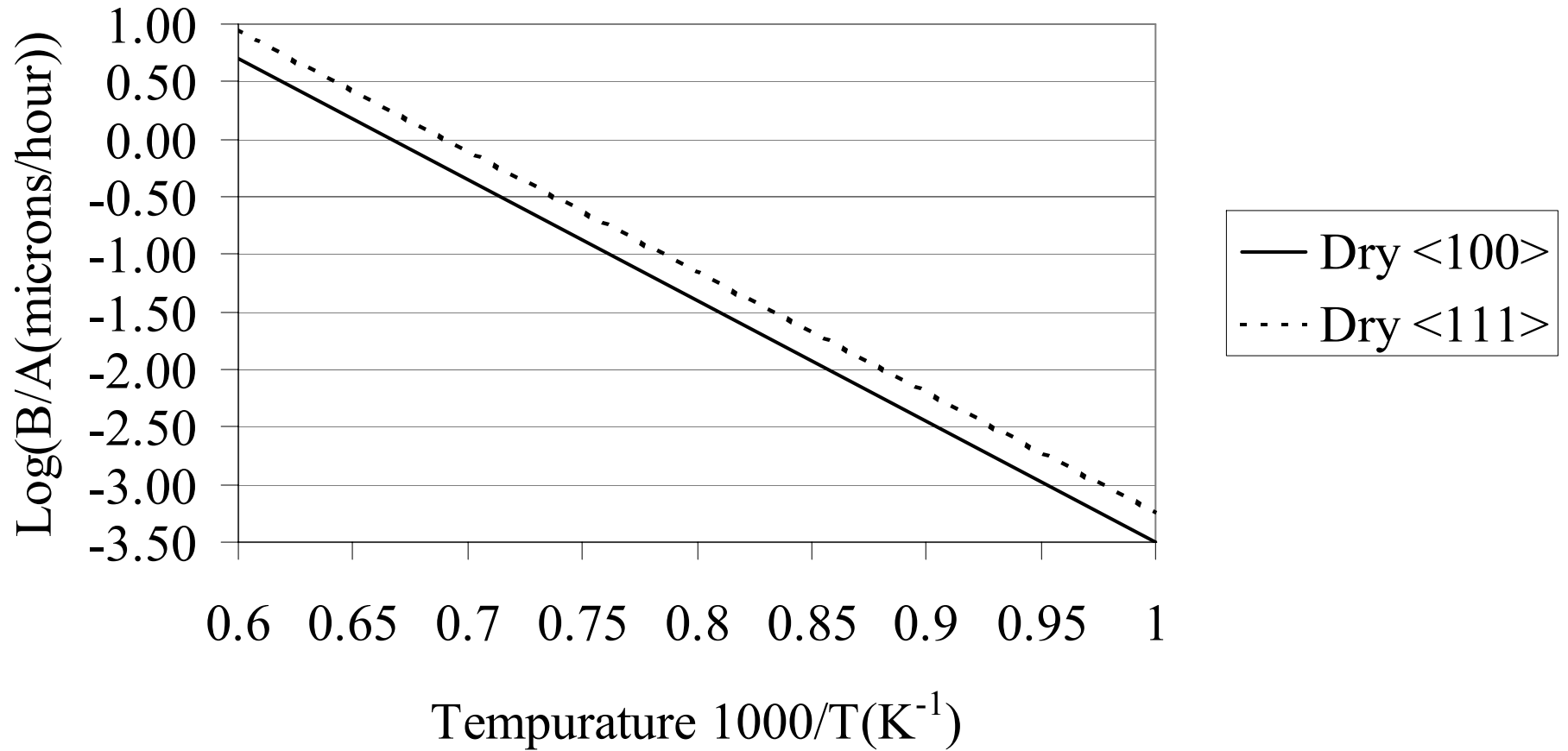
- Dry oxidation: Flow dry O<sub>2</sub> over sample at elevated temperatures.



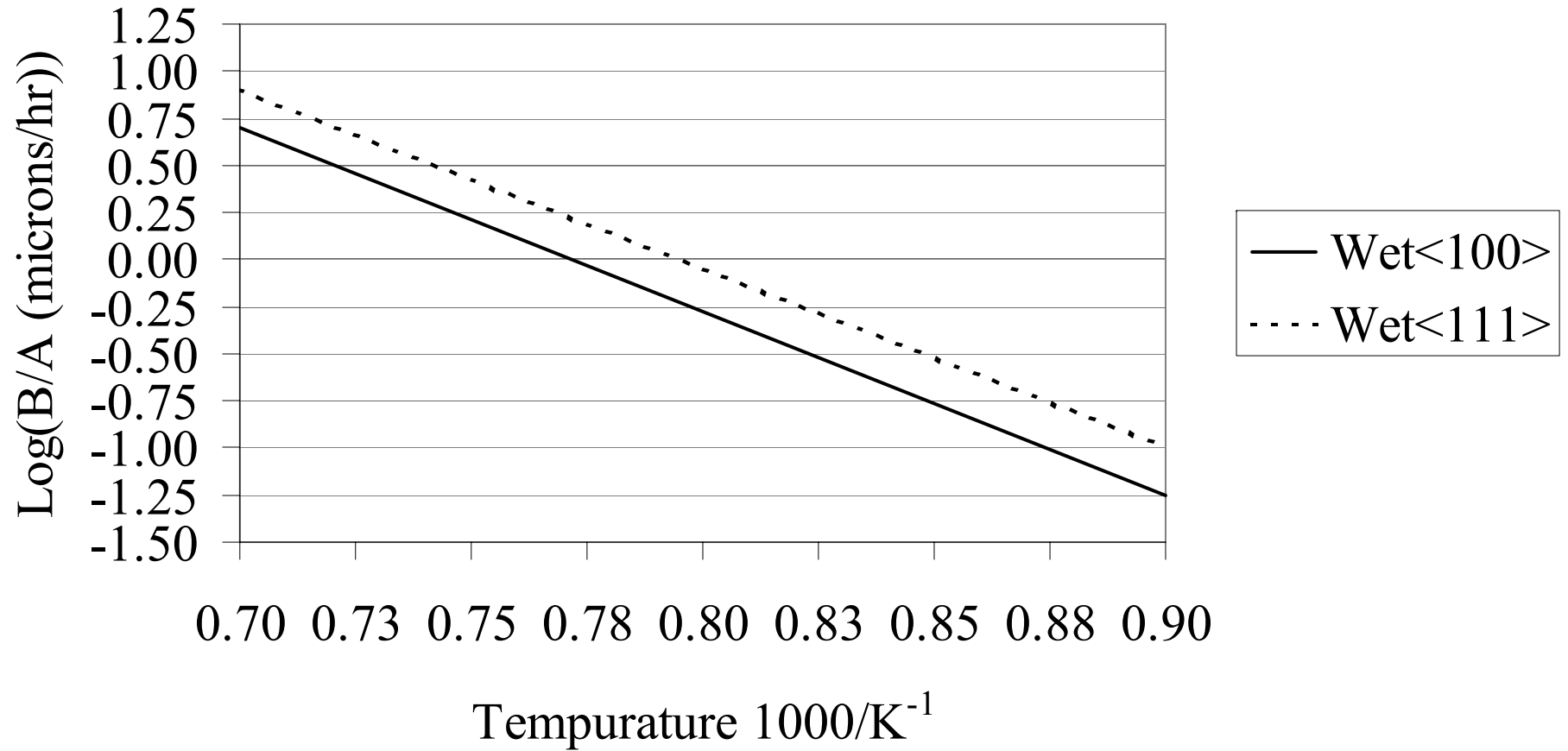
- Wet oxidation: Bubble N<sub>2</sub> through a water bubbler @95C° over sample at elevated temperatures.



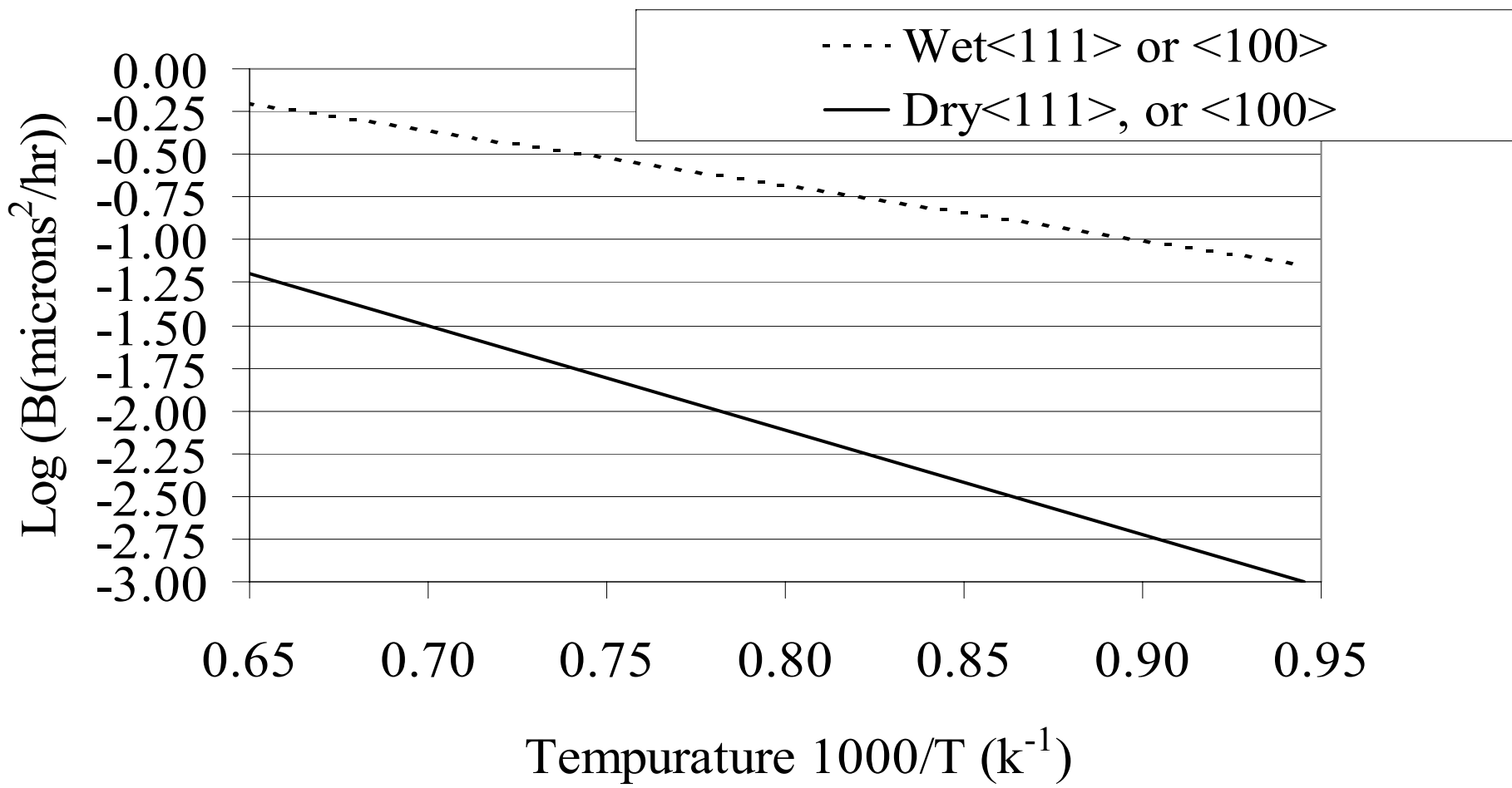
# Linear Rate Constant versus Temperature

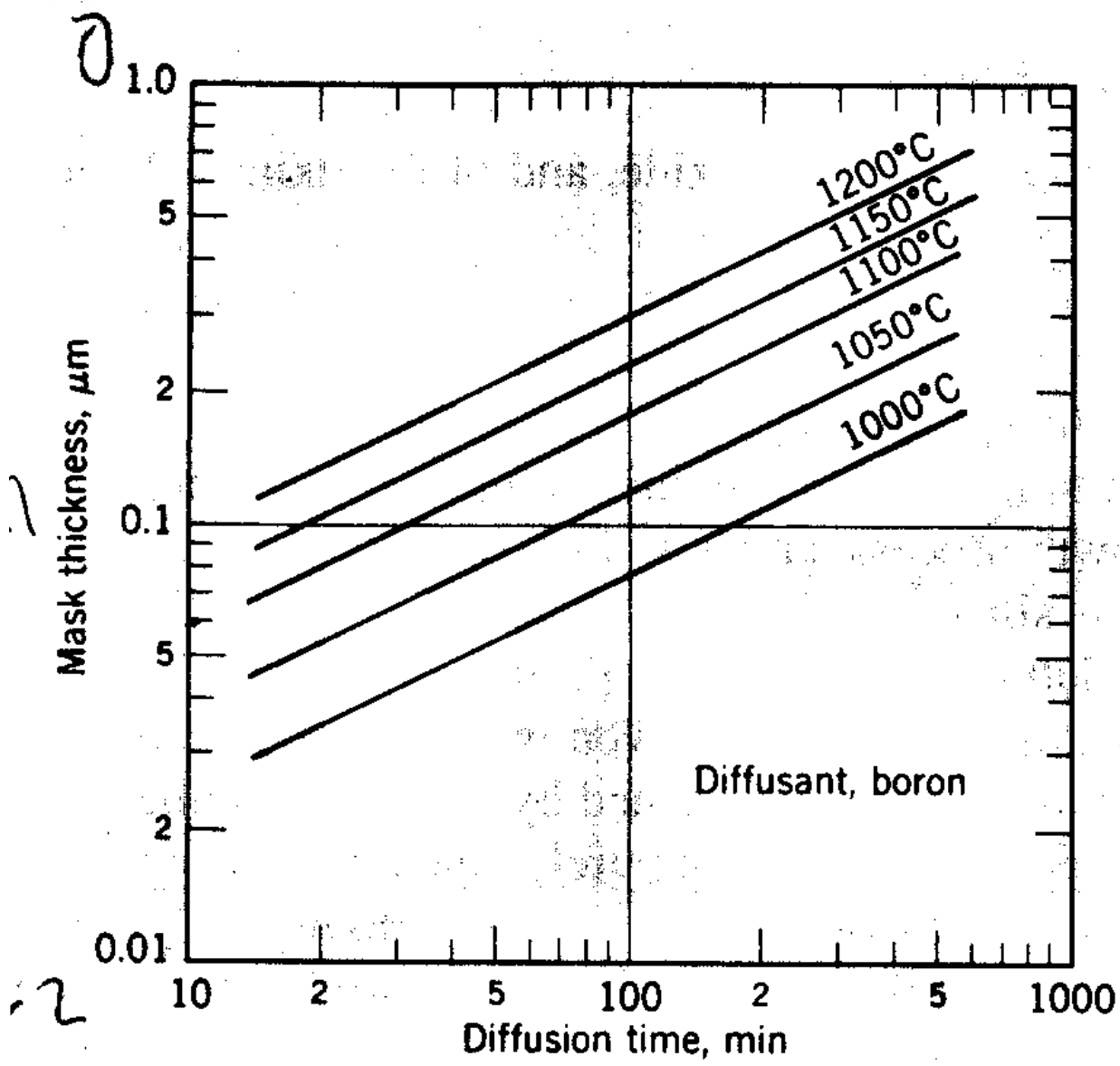


# Wet Oxidation

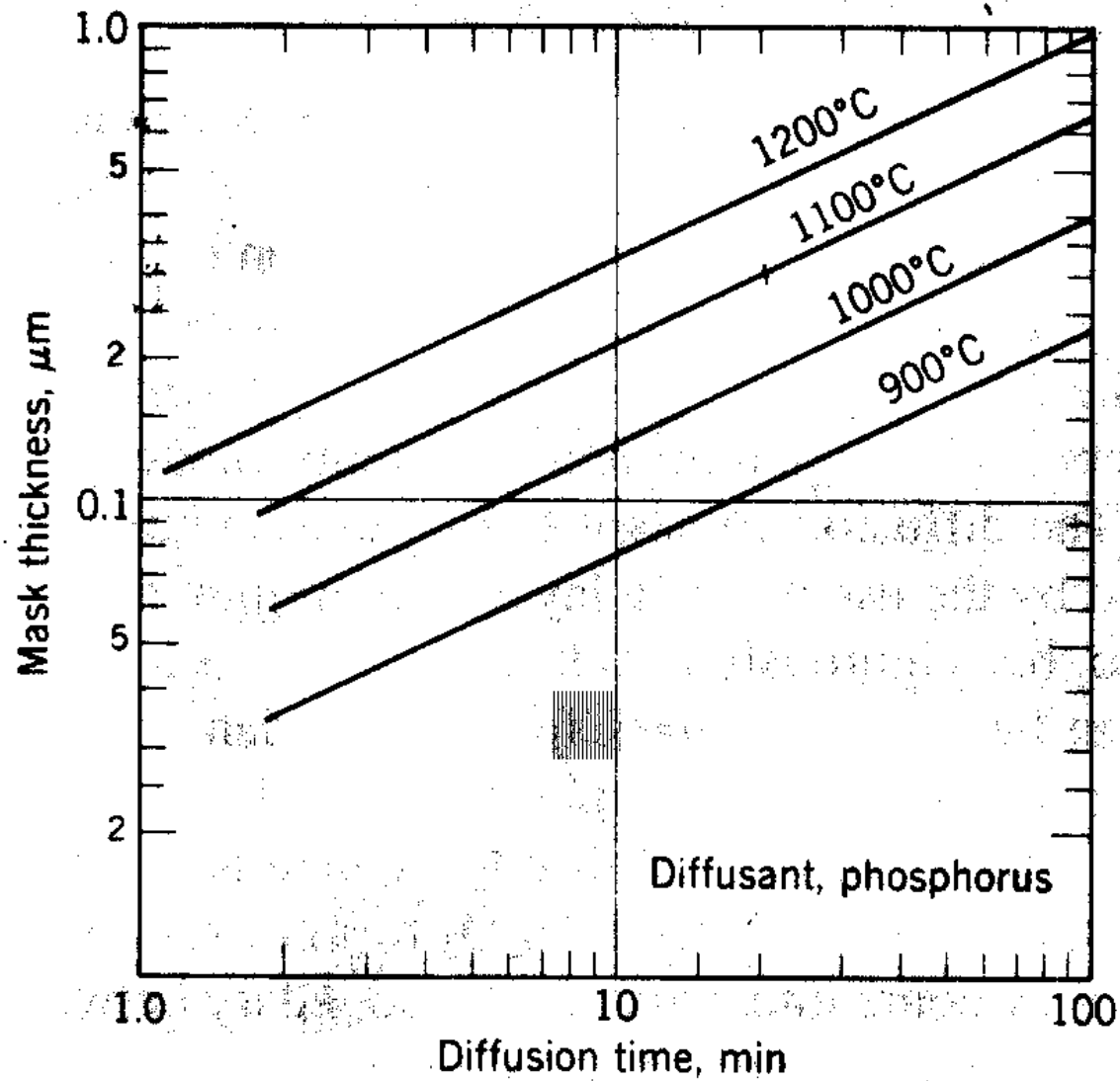


Parabolic Rate Constant versus Temperature





**Fig. 7.13** Mask thickness for boron.



**Fig. 7.14** Mask thickness for phosphorus.

# Numerical Examples

- How long do we need to grow  $\text{SiO}_2$  at  $1155^\circ\text{C}$  using a wet process  $\langle 111 \rangle$  to protect against a 30 minute  $1100^\circ\text{C}$  P diffusion?
- How long do we need to grow  $\text{SiO}_2$  at  $1265^\circ\text{C}$  using a dry process  $\langle 100 \rangle$  to create a MOS insulator capacitance ( $C_i = \epsilon_i/d$ ) of  $69\text{nF}$ ?
  - Note: For  $\text{SiO}_2$   $\epsilon_i = 3.9 * 8.85\text{e-}14\text{F/cm}$

# Ideal MOS Capacitor

- In this section we will discuss an ideal case and then add in “real surfaces” later.
- Modified work functions are necessary
  - Metal-Oxide interface  $q\phi_m$
  - Semiconductor-Oxide interface  $q\phi_s$

# Examples

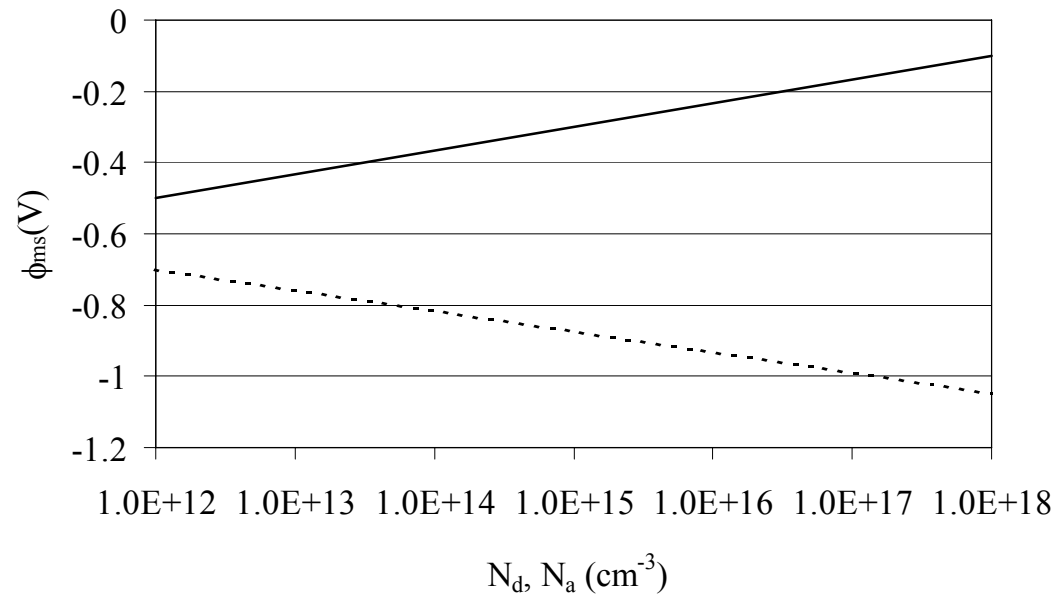
- Solve Example 8-1 except  $N_a=1 \times 10^{17} \text{cm}^{-3}$
- Solve Example 8-2 except use a  $50 \text{\AA}$   $\text{SiO}_2$  layer.

# Effects of Real Surfaces

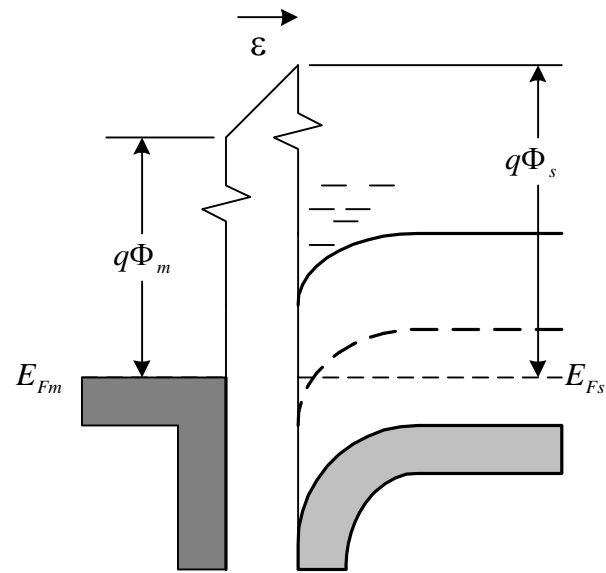
- Work Function Difference:
  - Doping level changes ( $\phi_{ms} = \phi_m - \phi_s$ )
  - Always negative
  - To take into account band bends down (can even cause a channel to exist).
- Interface Charge:
  - $Q_m$  (Mobile ionic),  $Q_{ot}$  (Oxide trapped),  $Q_f$  (Oxide fixed),  $Q_{it}$  (Interface trap)

# Work Function Difference

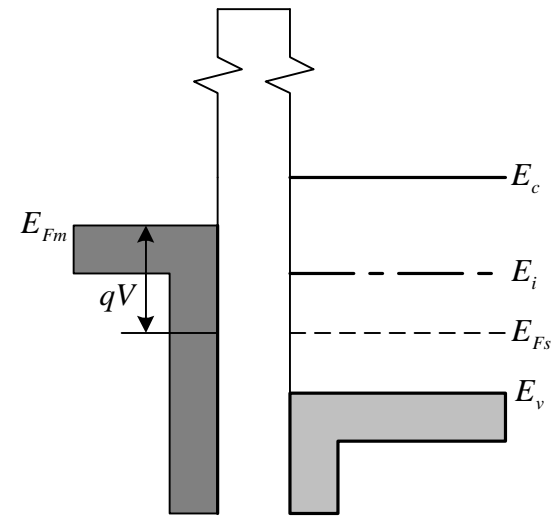
Variation of the metal-semiconductor work function



# Effects of Real Surfaces

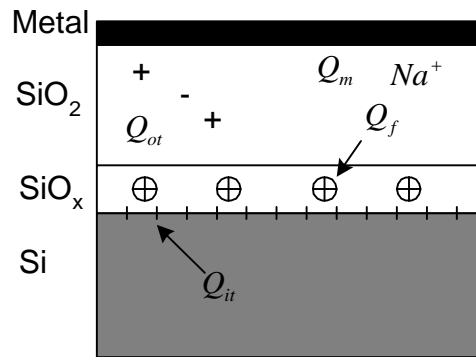


(a) Equilibrium  
 $V=0$

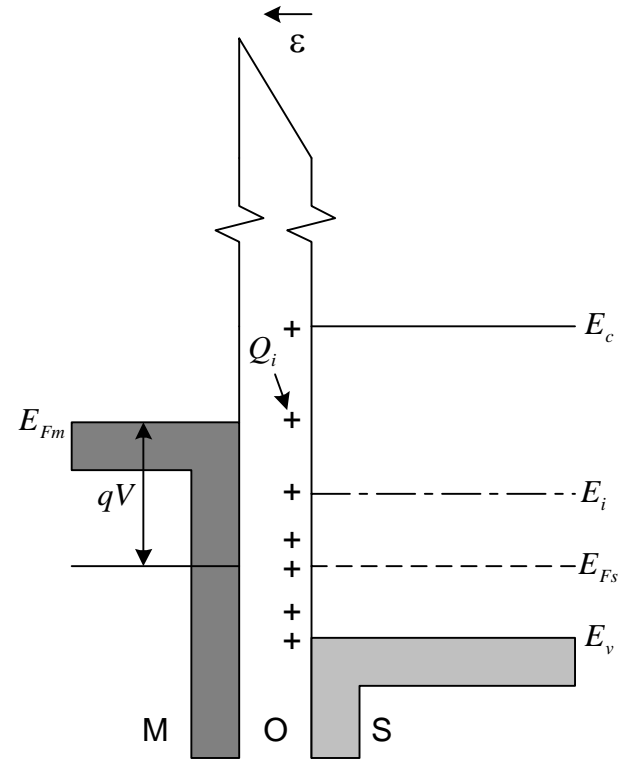


(b) Flat band  
 $V = V_{FB} = \Phi_{ms}$

# Effects of Real Surfaces



- $Q_m$  Mobile ionic charge
- $Q_{ot}$  Oxide trapped charge
- $Q_f$  Oxide fixed charge
- $Q_{it}$  Interface trap charge



$$V_{FB} = \varphi_{ms} - \frac{Q_i}{C_i} \quad V = V_{FB} = -\frac{Q_i}{C_i}$$

# Real Surfaces

- Interface Charge:
  - $Q_m$  (Mobile ionic) Sodium atoms move around under electric field
  - $Q_{ot}$  (Oxide trapped) Imperfections in  $\text{SiO}_2$  cause charge to be trapped
  - $Q_f$  (Oxide fixed) Ionic silicon left over from oxidation process.
  - $Q_{it}$  (Interface trap) Charge due to abrupt interface of  $\text{SiO}_2$  and Si.

# Threshold Voltage (Al Gate)

$$V_T = \varphi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\varphi_F (NMOS) \quad \varphi_F = .0259 \ln\left(\frac{N_a}{n_i}\right) (NMOS)$$

$$V_T = \varphi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} - 2\varphi_F (PMOS) \quad \varphi_F = .0259 \ln\left(\frac{N_d}{n_i}\right) (PMOS)$$

$\varphi_{ms}$  Get from chart (both n and p channel)

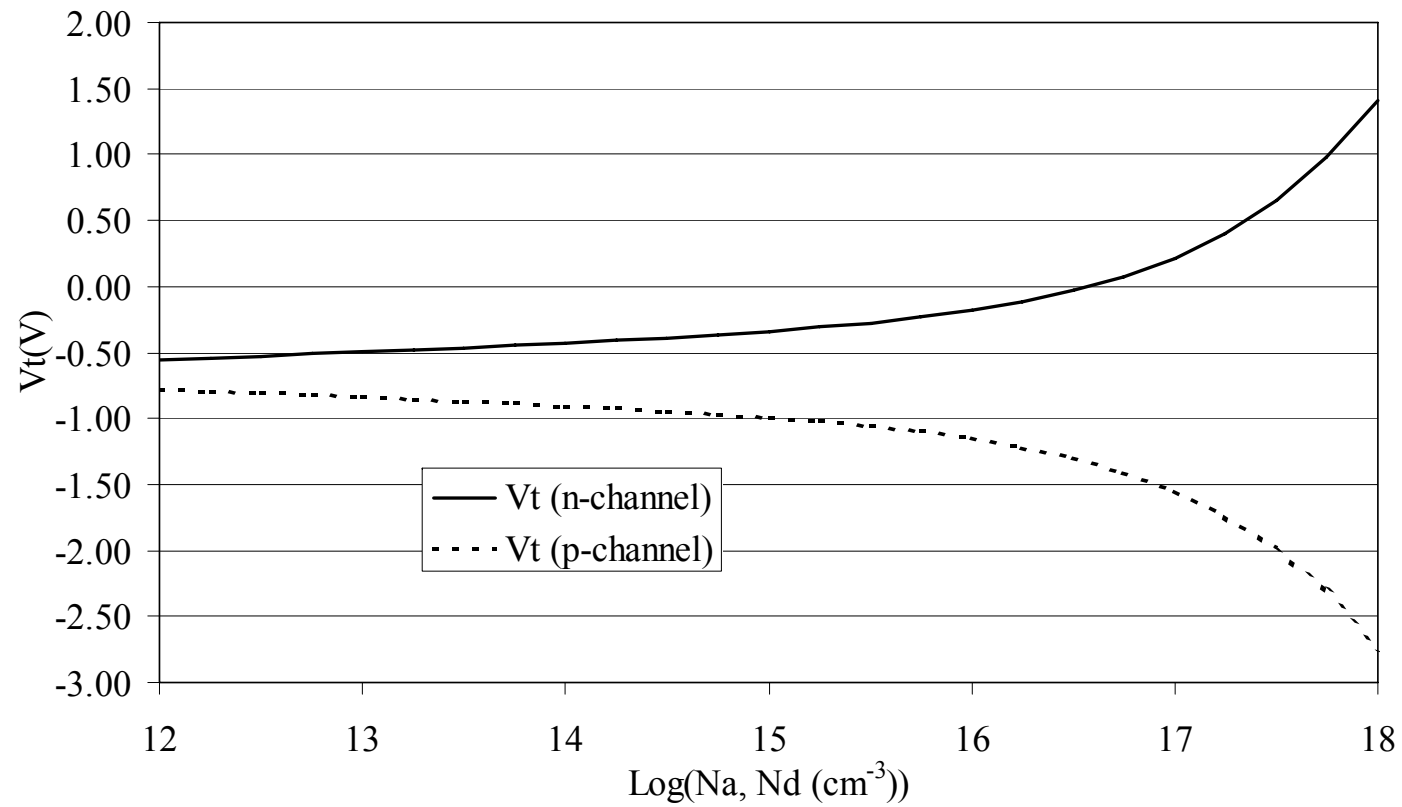
$$C_i = \frac{(3.9)(8.885 \times 10^{-14} \text{ F/cm})}{d(\text{cm})} \quad (\text{both n and p channel})$$

$Q_i$  = Given to you by process engineer.

$$Q_d(nmos) = -2(\epsilon_s q N_a \varphi_F)^{\frac{1}{2}}, \quad Q_d(pmos) = 2(\epsilon_s q N_d \varphi_F)^{\frac{1}{2}},$$

# Threshold Voltage

$V_t$  for  $d=100\text{\AA}$ ,  $Q_d=5 \times 10^{10}(\text{cm}^{-2})q$



# Control of Threshold Voltage

- Silicon gate technology
  - $\Phi_{ms}$  is reduce by using poly-silicon as the gate
    - Poly-silicon must be heavily doped
    - $\Phi_{ms}$  is now just the difference in Fermi levels of the two silicon regions.
    - Poly-silicon is also more process friendly (It can withstand higher temperatures than Al)

# Control of Threshold Voltage

- Control of  $C_i$ 
  - We would like a small  $V_T$  under the gate but elsewhere we would like a large  $V_T$  to prevent channels from forming between transistors.
  - Smaller  $C_i$ , leads to a smaller threshold.

# Control of Threshold Voltage

- Ion Implantation
  - B ions can be implanted in a two dimensional sheet just below the oxide layer. These ions are negatively charged and can be used to offset  $Q_d$ . Dose typically 10 seconds.

$$V_{T(New)} = V_{T(Old)} + \frac{qF_B}{C_i}$$

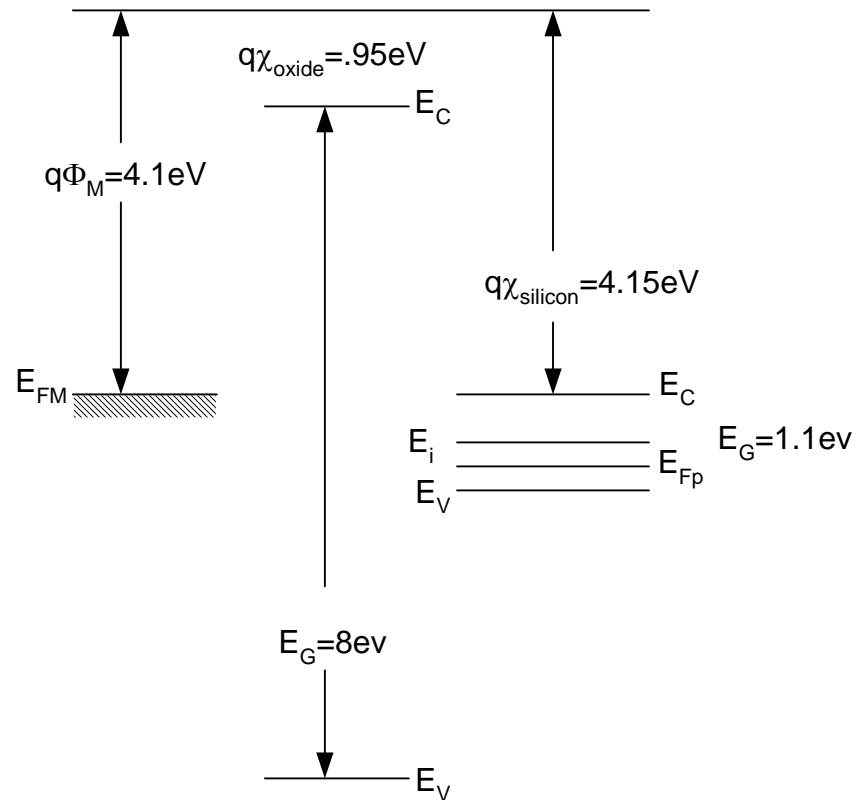
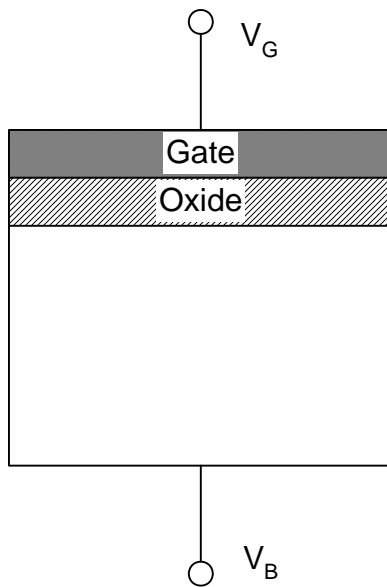
# Control of Threshold Voltage

- Control  $Q_i$ 
  - Grow the  $\text{SiO}_2$  layer on  $\{100\}$  oriented wafers
    - Less dangling bonds
    - Slower growth rate leads to higher quality layer
    - HCl in oxygen reduces sodium in  $\text{SiO}_2$

# The MOS Structure

- M-Metal or Polysilicon called the Gate
- Oxide for Silicon dioxide (or maybe some new exotic material)
- Semiconductor. Silicon Yes there are some reports of a GaAs based MOSFET.
  - I even have a grad student working on it.
  - If you want to feed your family stick with silicon based MOSFETS.

# The Big Picture



# Basic Equations

$$np = n_i^2$$

$$\phi_F = \frac{E_F - E_i}{q}$$

$$n_{po} = \frac{n_i^2}{Na}$$

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{Na}{n_i}$$

$$p_{po} = Na$$

$$\phi_{Fn} = \frac{kT}{q} \ln \frac{Nd}{Ni}$$

# Example

- Derive the metal-semiconductor work function.
- Derive the metal-semiconductor work function if the gate is polysilicon.

# Example

- Units:
  - The units used in energy band diagrams should all be in joules which is a measurement of energy.
  - To actually calculate anything useful we use electron volts because the numbers would be unwieldy if we used Joules.
  - On the diagram  $\phi$  and  $\chi$  always have a q before them to make sure the units work out, but do not use them in an equation. Energy levels are given in eV on the diagram but represent energy in Joules.

# Units Continued

- Take for example  $\phi_F$ . To make the units work out we divide  $E_F - E_i$  by the electronic charge, but in practice  $E_F$  and  $E_i$  are already in eV!

$$\phi_F = \frac{E_F - E_i}{q}$$

- In practice use:  $\phi_F = E_F - E_i$

# Metal Semiconductor Work Function (A1)

$$\Phi_{\text{FP}} := \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_A}{n_i}\right) \quad \Phi_{\text{FN}} := \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_D}{n_i}\right)$$

$$\Phi_{\text{ms}} := \Phi_{\text{Aluminum}} - \left( \chi_{\text{Si}} + \frac{E_g}{2} + \Phi_{\text{FP}} \right)$$

$$\Phi_{\text{ms}} := \Phi_{\text{Aluminum}} - \left( \chi_{\text{Si}} + \frac{E_g}{2} - \Phi_{\text{FN}} \right)$$

# Metal Semiconductor Work Function (n+ Poly Si)

$$\Phi_{\text{ms}} := \left( \chi_{\text{Si}} + \frac{E_{\text{g}}}{2} - \Phi_{\text{FN}} \right) - \left( \chi_{\text{Si}} + \frac{E_{\text{g}}}{2} + \Phi_{\text{FP}} \right)$$

$$\Phi_{\text{ms}} := \Phi_{\text{FN}} - \Phi_{\text{FP}}$$

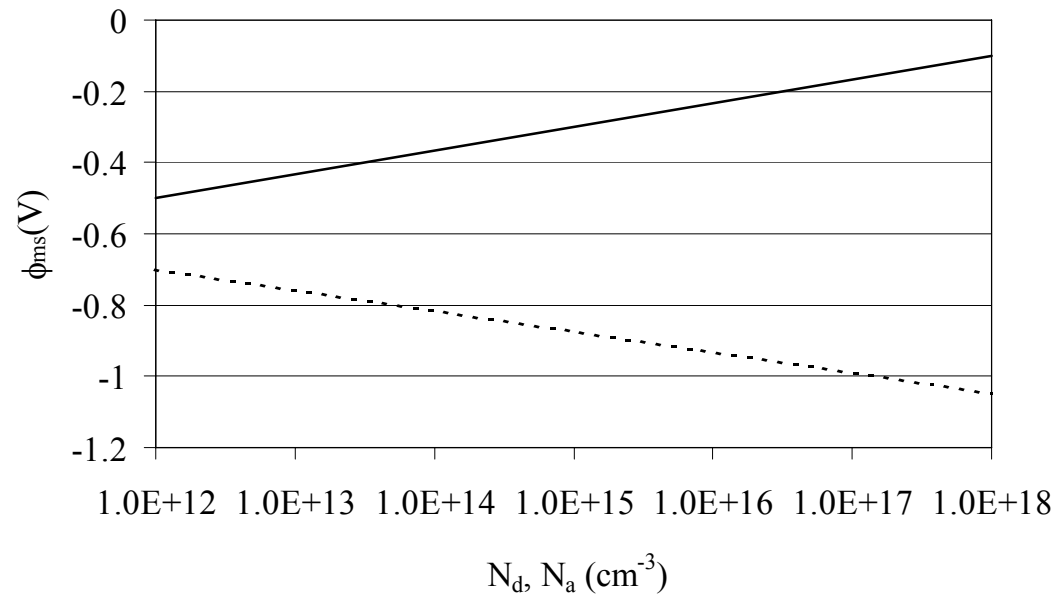
$$\varphi_{\text{ms}} = \frac{kT}{q} \ln\left(\frac{N_{\text{A}} N_{\text{D}}}{n_{\text{i}}^2}\right)$$

# Effects of Real Surfaces

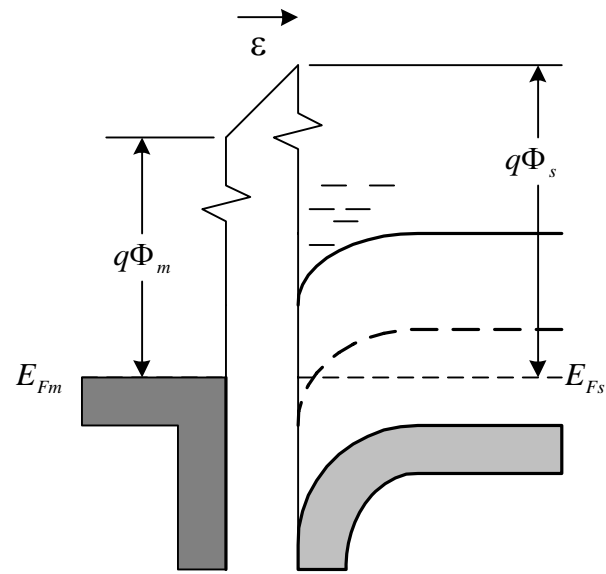
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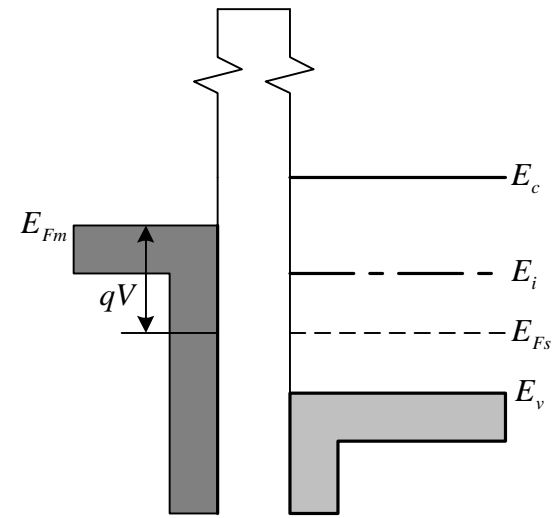
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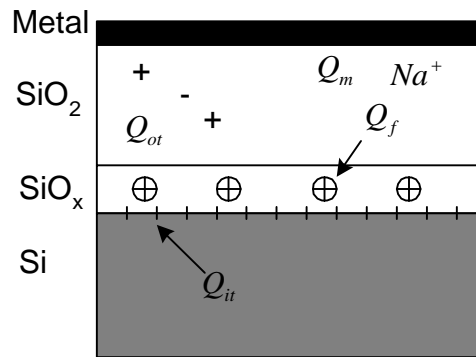


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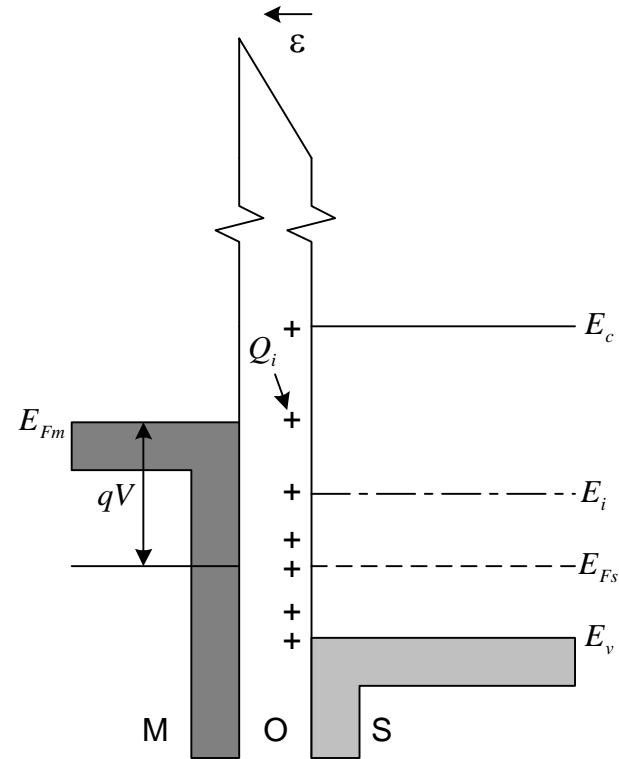


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