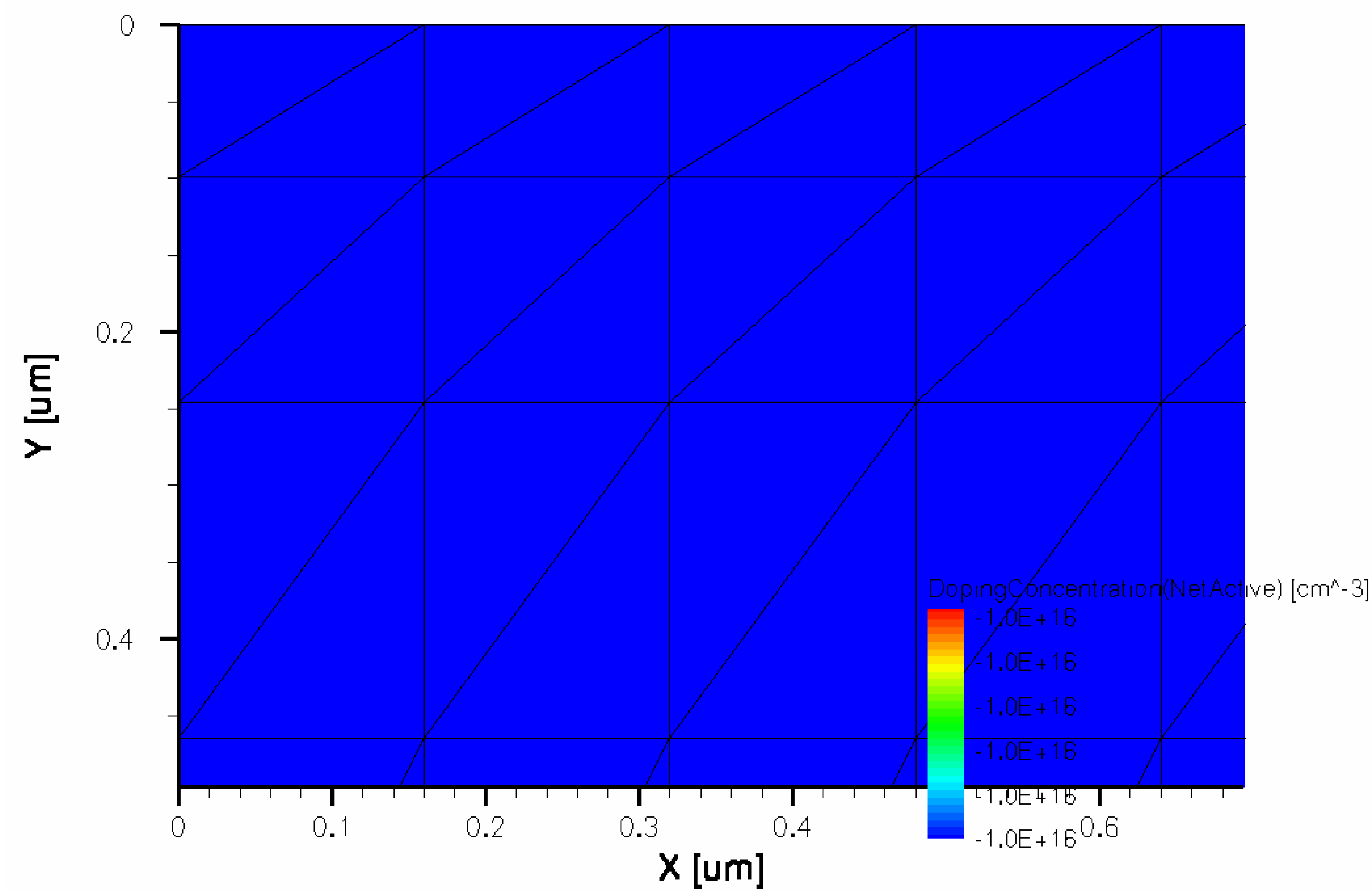
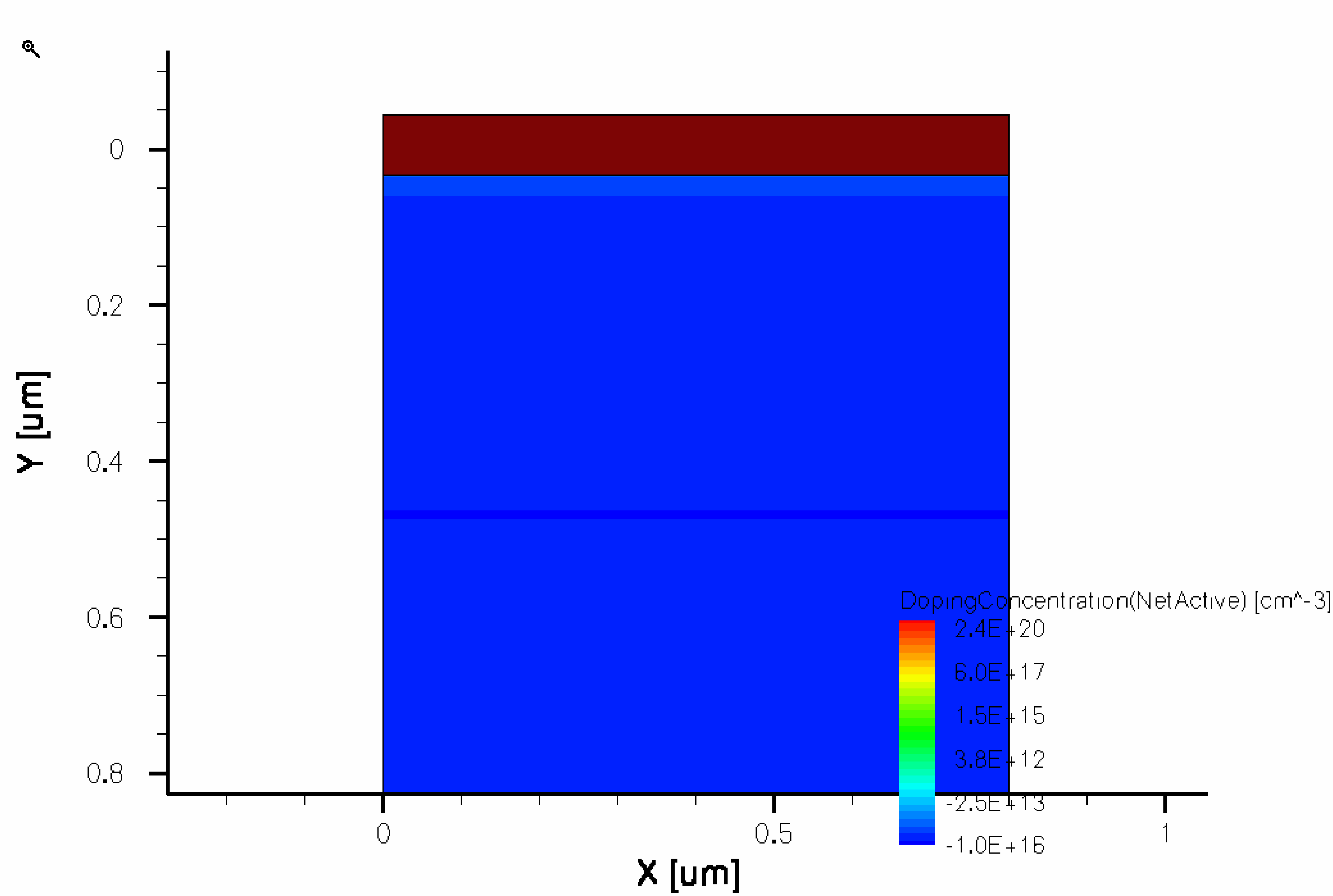
The Diode

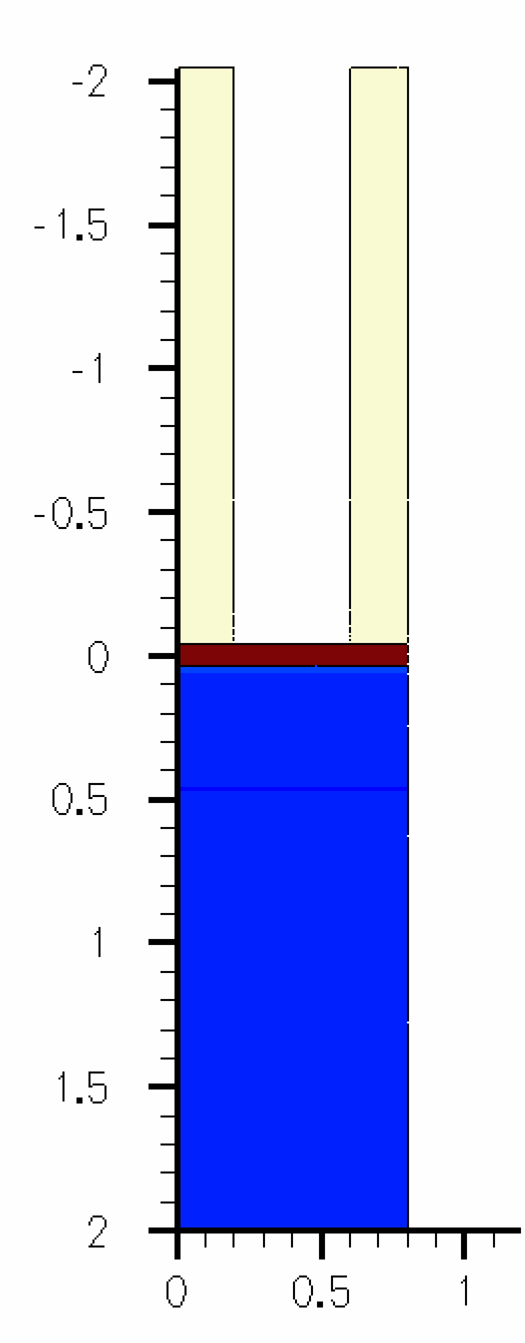
D. W. Parent

Bare Si Wafer, <100> NA=10^{16}cm^{-3}

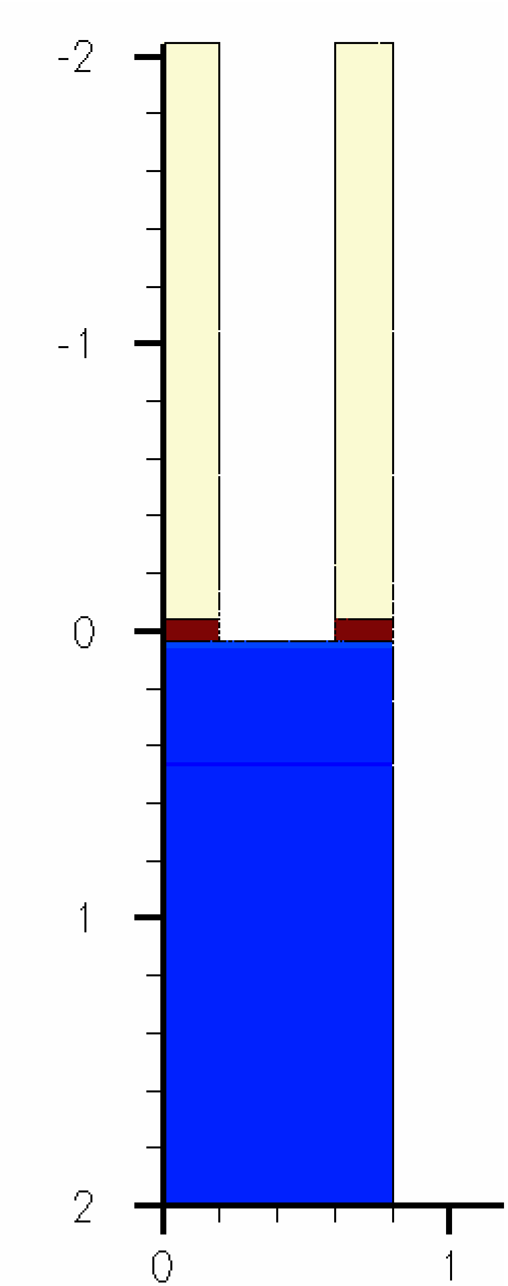


Masking Oxide



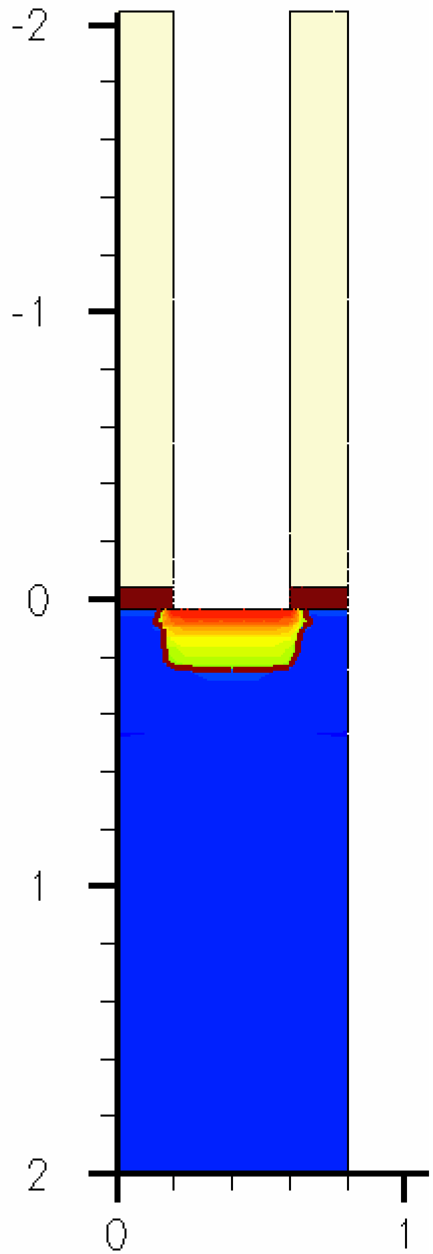


Pattern Photoresist

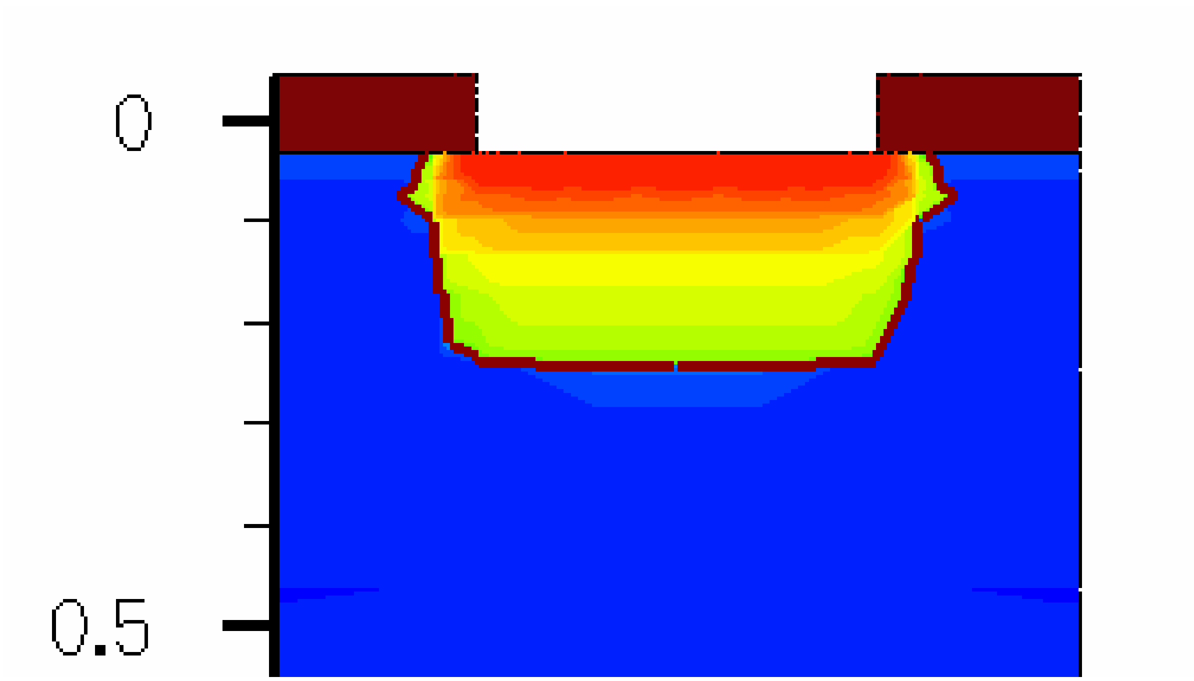


Etch Oxide

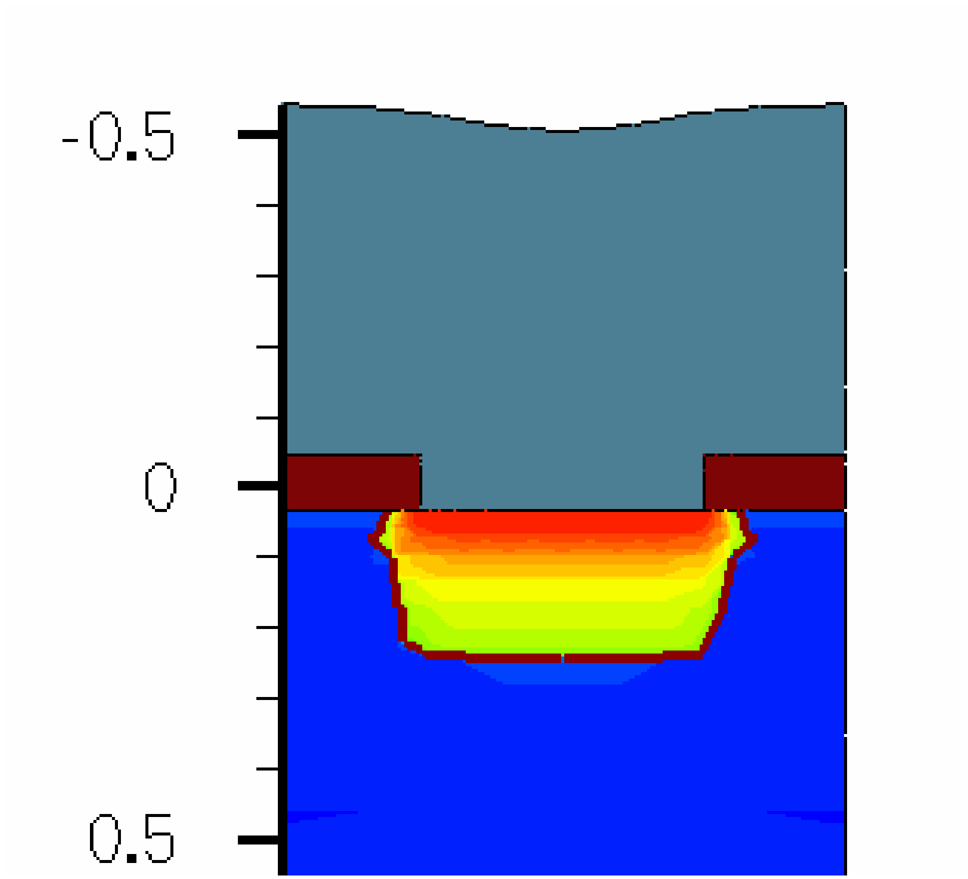
Implant



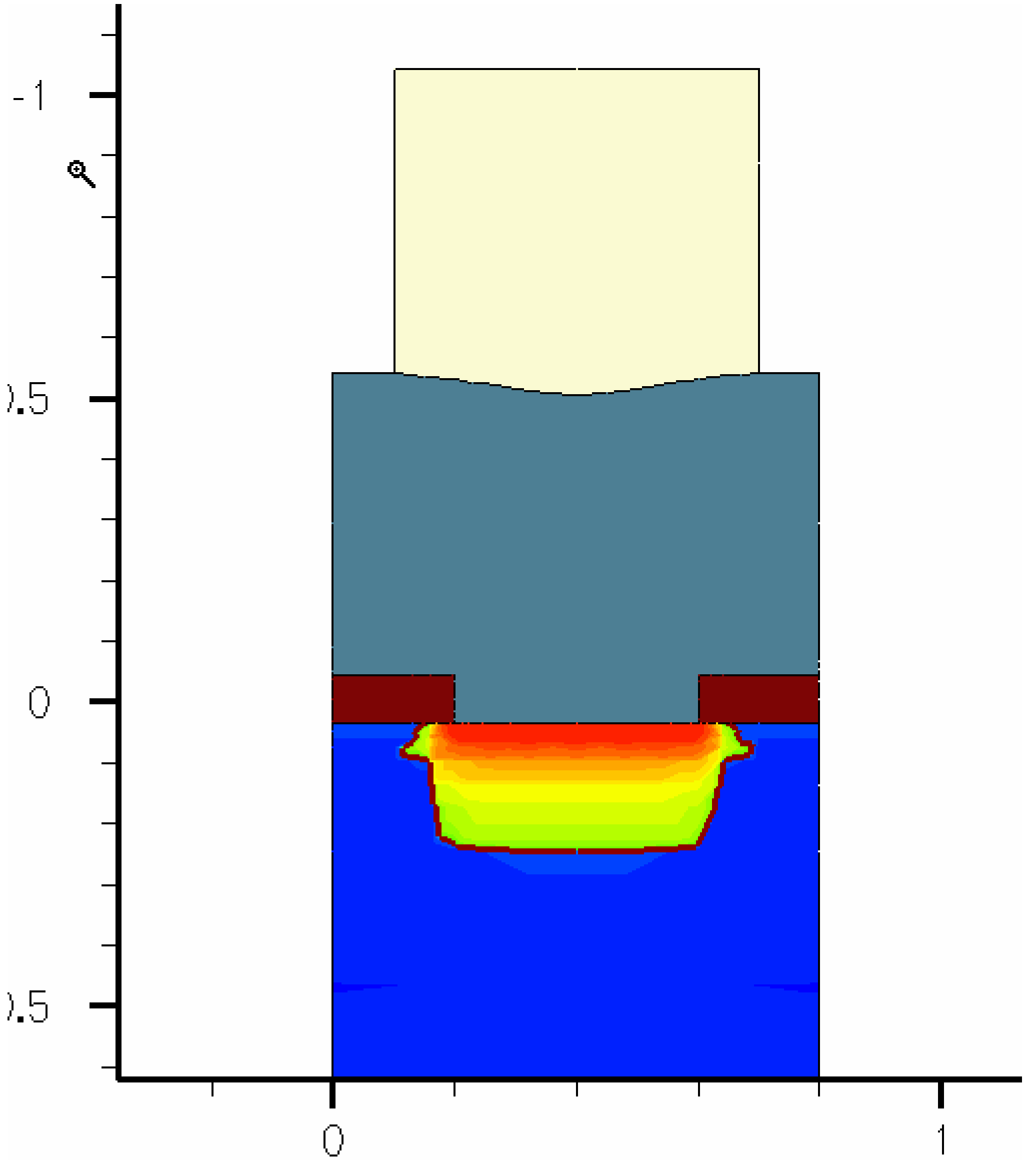
Strip PR



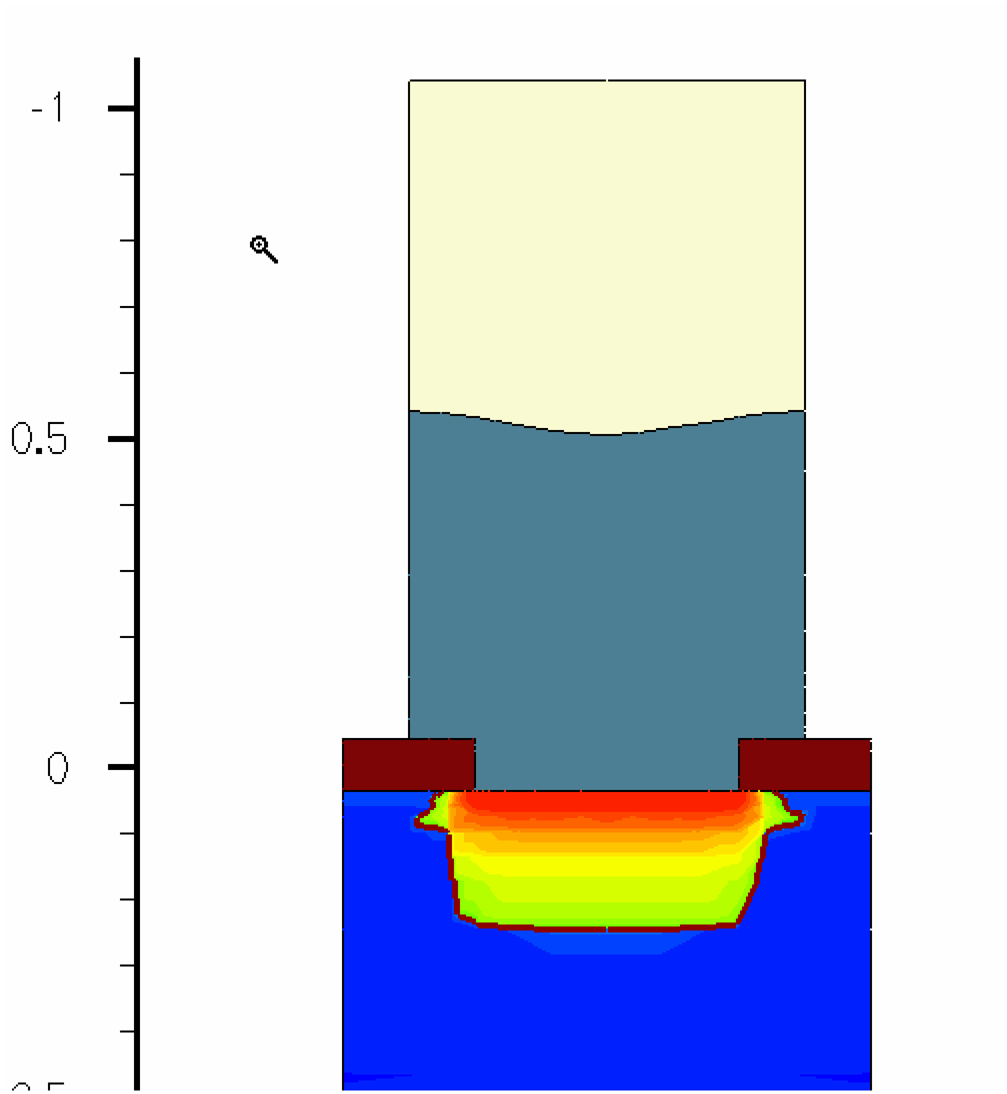
Metalization



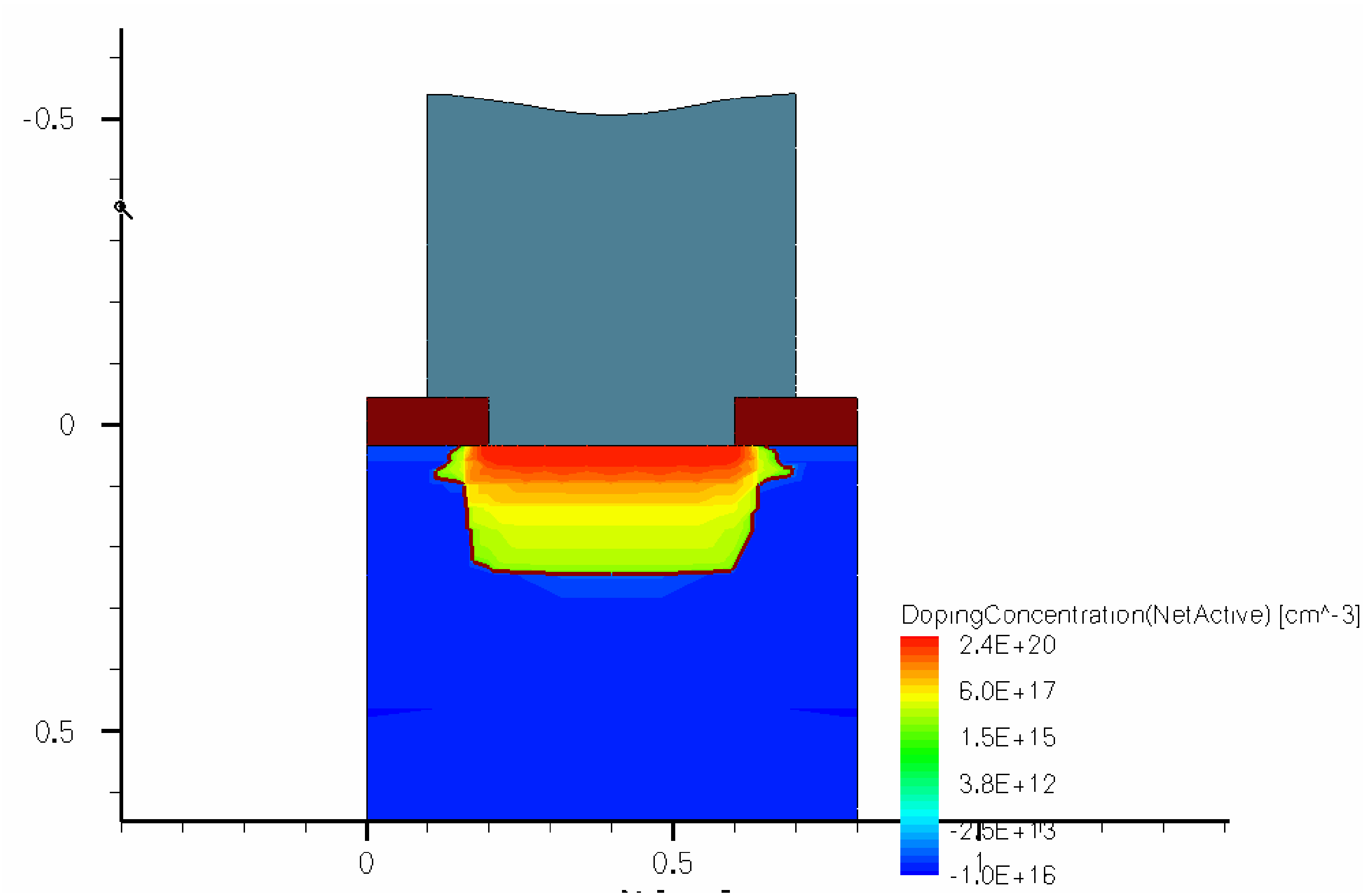
Pattern M1



Etch Al



Final Diode



-0.5
0
0.5
0
0.5
1
DopingConcentration(NetActive) [cm^-3]
2.4E+20
6.0E+17
1.5E+15
3.8E+12
-2.5E+13
-1.0E+16

Impurity Diffusion

- Diffusion: An old concept whose mathematics have been worked out for a long time.
- Diffusion: A concentration gradient will cause a force to redistribute particles until there is no concentration gradient.
- Uses: Drain and Source regions for MOS, active regions for BJTs

Impurity Diffusion

- It is ideal for batch processes.
- It does not induce crystal damage
- Diffusion is very useful for p and n type doping in Si.
- Diffusion in III-V(GaAs, InP) is limited to Zn diffusions for p+ layers for ohmic contacts.

Impurity Diffusion

- Diffusion does not give you as exact control over doping concentration and junction depth as does ion-implantation, but it is an inexpensive process.
- Ion-implantation can place oxygen ions under the surface of Si which can be turned into SiO2.
- Ion-implantation can place a buried layer of dopant atoms in silicon.

Impurity Diffusion (How does it work?)

- At elevated temperatures impurity atoms move around the lattice in a random series of jumps.
  - Three dimensional in nature
  - Only net movement if there is a concentration gradient.

Impurity Diffusion (How does it work?)

- Random series of jumps?
  - Interstitial Diffusion: Impurity atoms jump between the empty spaces in the semiconductor lattice. This is a fast process that Na^+ and Li^+ use to move around the lattice (Bad).
  - Substitutional Diffusion: Impurity atoms jump from one vacant lattice site to an adjacent lattice site. There are not many of these vacant sites so this type of diffusion is slow.

Dopants used for Si diffusion

- Arsenic
  - Low misfit factor which leads to high n-type concentrations. Also has an abrupt doping profile.
- Phosphorus
  - Most common diffusion dopant source. It does not make as abrupt junctions as arsenic.

Dopants used for Si diffusion

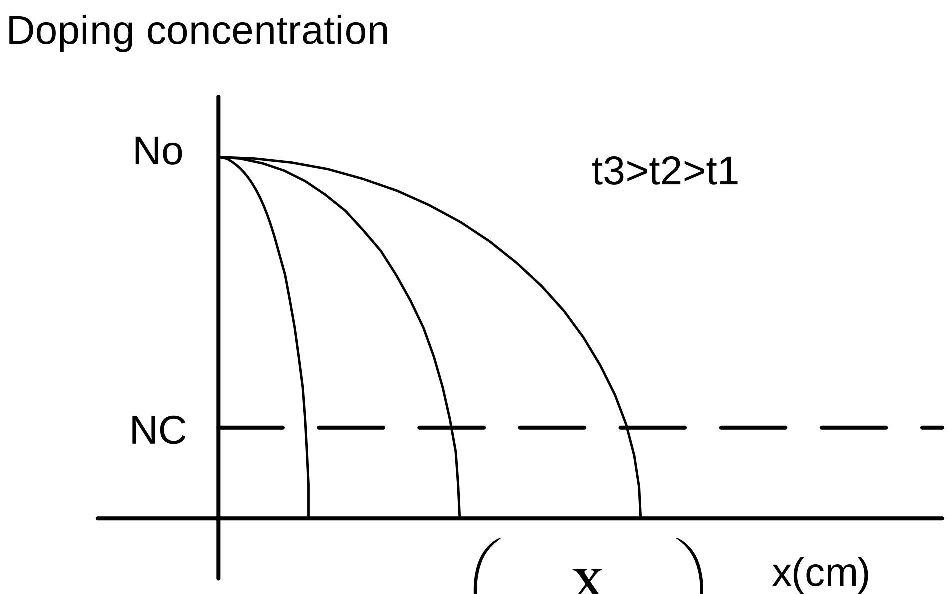
- Boron
  - Used for p and p+ diffusions
- Aluminum
  - Annealed into Si to make p+/p(boron) ohmic contacts.

Lateral diffusion

- At the beginning of the diffusion process, there is no concentration gradient in the Si.
- As soon as there are impurity atoms in the Si, there is an impurity gradient in all directions thus diffusion occurs in all directions.
- This causes impurities to diffusion underneath the mask. (not so the ion-implantation)

Types of Diffusion

- "Infinite Source" or Pre-deposition

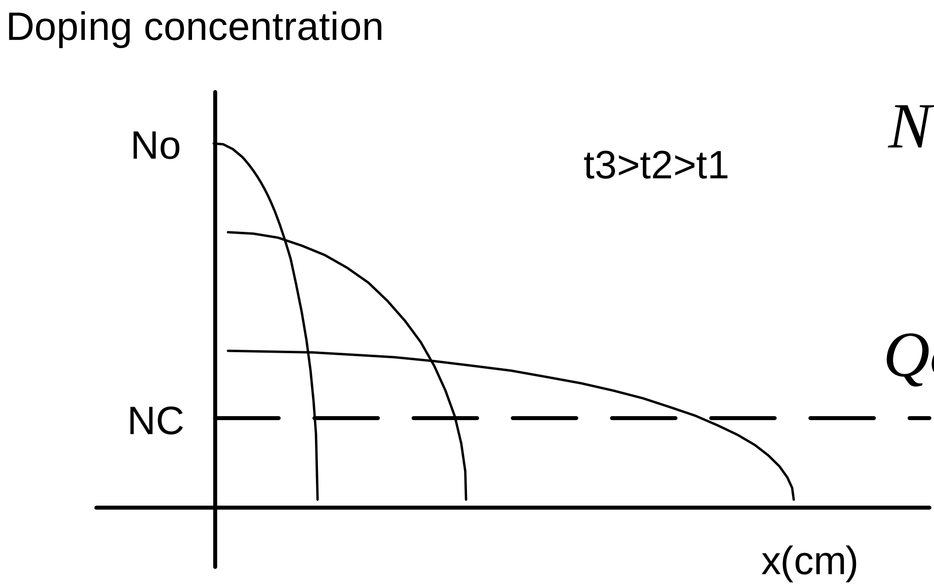


$$N(x,t) = No\,erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

$$No(cm^{-3}), D(cm^2/s), x(cm), t(s)$$

Types of Diffusion

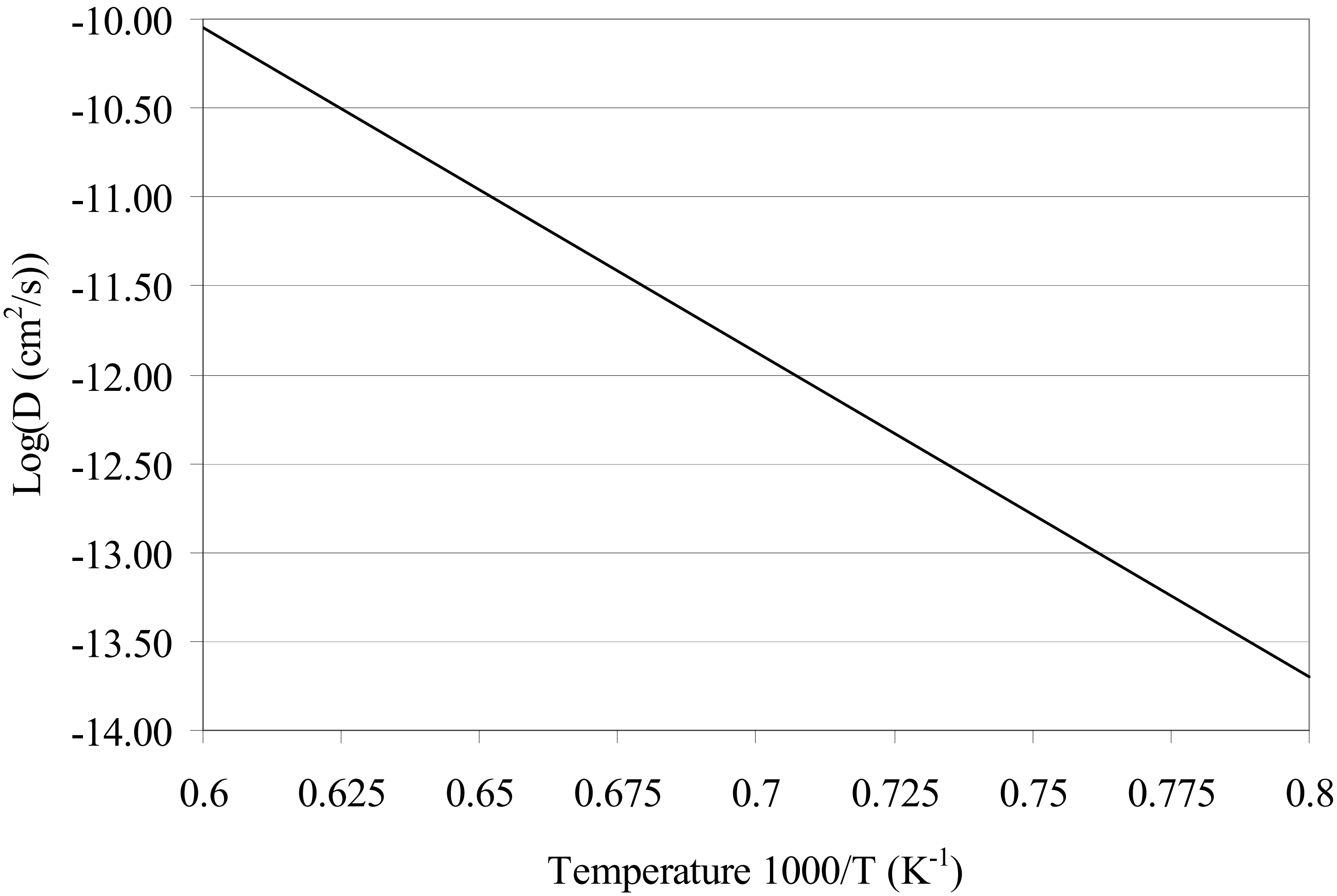
- "Limited Source" or Drive-in

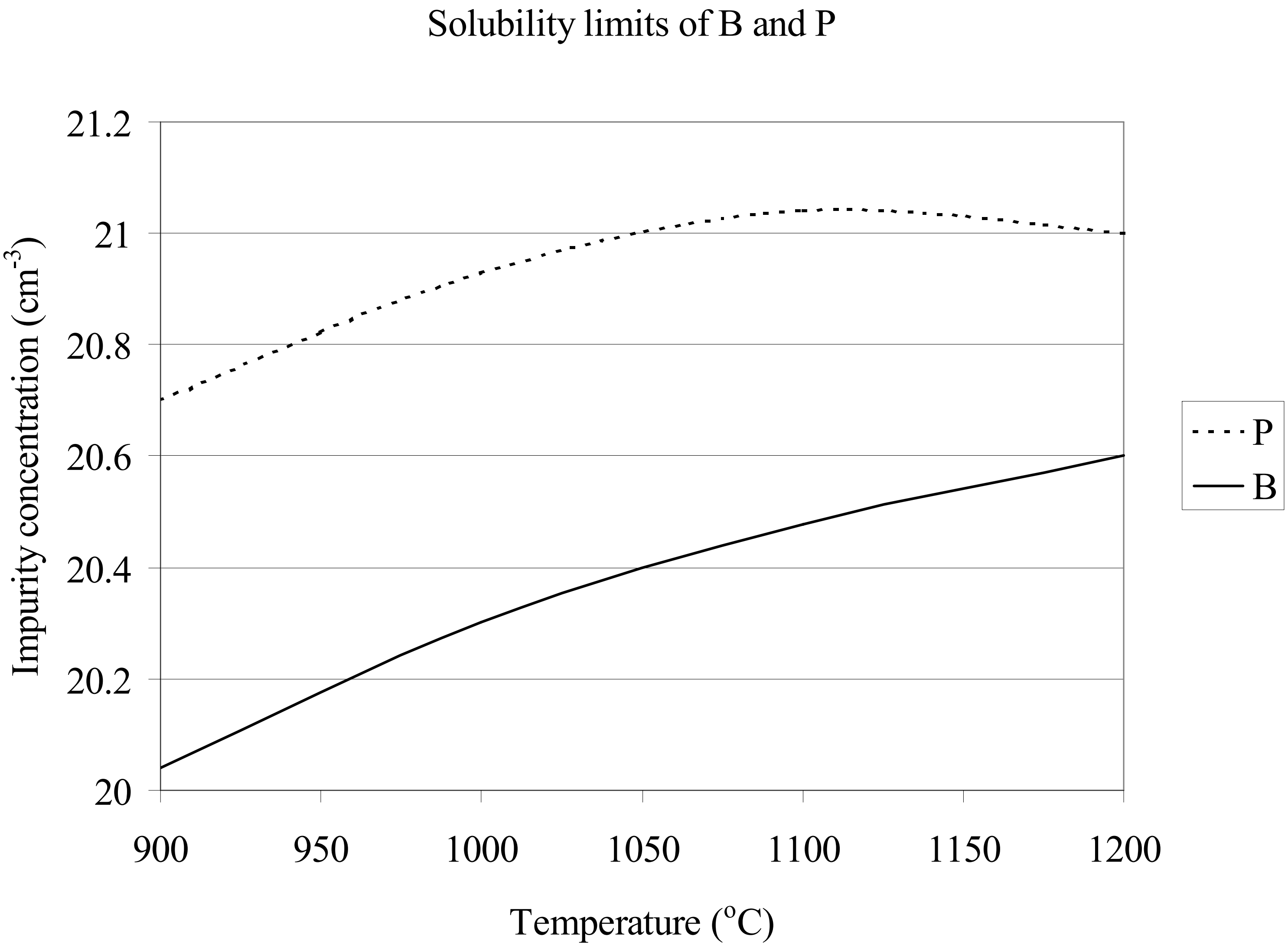


$$N(x,t) = \frac{Qo}{\sqrt{\pi D t}} e^{-\left(\frac{x}{2\sqrt{Dt}}\right)^2}$$

$$Qo = 2N_{o1}\left(\frac{D_1 t_1}{\sqrt{\pi}}\right)^{\frac{1}{2}}$$

Average Diffusivities for P and B





Solubility limits of B and P
21.2
21
20.8
20.6
20.4
20.2
20
900
950
1000
1050
1100
1150
1200
Temperature (°C)
Impurity concentration (cm-3)
P
B

Z	erf(Z)	Z	erf(Z)	Z	erf(Z)	Z	erf(Z)
0.00	0.000000000	0.50	0.520499878	1.00	0.842700793	1.50	0.966105146
0.01	0.011283416	0.51	0.529243620	1.01	0.846810496	1.51	0.967276748
0.02	0.022564575	0.52	0.537898630	1.02	0.850838018	1.52	0.968413497
0.03	0.033841222	0.53	0.546464097	1.03	0.854784211	1.53	0.969516209
0.04	0.045111106	0.54	0.554939250	1.04	0.858649947	1.54	0.970585690
0.05	0.056371978	0.55	0.563323366	1.05	0.862436106	1.55	0.971622733
0.06	0.067621594	0.56	0.571615764	1.06	0.866143587	1.56	0.972628122
0.07	0.078857720	0.57	0.579815806	1.07	0.869773297	1.57	0.973602627
0.08	0.090078126	0.58	0.587922900	1.08	0.873326158	1.58	0.974547009
0.09	0.101280594	0.59	0.595936497	1.09	0.876803102	1.59	0.975462016
0.10	0.112462916	0.60	0.603856091	1.10	0.880205070	1.60	0.976348383
0.11	0.123622896	0.61	0.611681219	1.11	0.883533012	1.61	0.977206837
0.12	0.134758352	0.62	0.619411462	1.12	0.886787890	1.62	0.978038088
0.13	0.145867115	0.63	0.627046443	1.13	0.889970670	1.63	0.978842840
0.14	0.156947033	0.64	0.634585829	1.14	0.893082328	1.64	0.979621780
0.15	0.167995971	0.65	0.642029327	1.15	0.896123843	1.65	0.980375585
0.16	0.179011813	0.66	0.649376688	1.16	0.899096203	1.66	0.981104921
0.17	0.189992461	0.67	0.656627702	1.17	0.902000399	1.67	0.981810442
0.18	0.200935839	0.68	0.663782203	1.18	0.904837427	1.68	0.982492787
0.19	0.211839892	0.69	0.670840062	1.19	0.907608286	1.69	0.983152587
0.20	0.222702589	0.70	0.677801194	1.20	0.910313978	1.70	0.983790459
0.21	0.233521923	0.71	0.684665550	1.21	0.912955508	1.71	0.984407008
0.22	0.244295912	0.72	0.691433123	1.22	0.915533881	1.72	0.985002827
0.23	0.255022600	0.73	0.698103943	1.23	0.918050104	1.73	0.985578500
0.24	0.265700059	0.74	0.704678078	1.24	0.920505184	1.74	0.986134595
0.25	0.276326390	0.75	0.711155634	1.25	0.922900128	1.75	0.986671671
0.26	0.286899723	0.76	0.717536753	1.26	0.925235942	1.76	0.987190275
0.27	0.297418219	0.77	0.723821614	1.27	0.927513629	1.77	0.987690942
0.28	0.307880068	0.78	0.730010431	1.28	0.929734193	1.78	0.988174196
0.29	0.318283496	0.79	0.736103454	1.29	0.931898633	1.79	0.988640549
0.30	0.328626759	0.80	0.742100965	1.30	0.934007945	1.80	0.989090502
0.31	0.338908150	0.81	0.748003281	1.31	0.936063123	1.81	0.989524545
0.32	0.349125995	0.82	0.753810751	1.32	0.938065155	1.82	0.989943156
0.33	0.359278655	0.83	0.759523757	1.33	0.940015026	1.83	0.990346805
0.34	0.369364529	0.84	0.765142711	1.34	0.941913715	1.84	0.990735948
0.35	0.379382054	0.85	0.770668058	1.35	0.943762196	1.85	0.991111030
0.36	0.389329701	0.86	0.776100268	1.36	0.945561437	1.86	0.991472488
0.37	0.399205984	0.87	0.781439845	1.37	0.947312398	1.87	0.991820748
0.38	0.409009453	0.88	0.786687319	1.38	0.949016035	1.88	0.992156223
0.39	0.418738700	0.89	0.791843247	1.39	0.950673296	1.89	0.992479318
0.40	0.428392355	0.90	0.796908212	1.40	0.952285120	1.90	0.992790429
0.41	0.437969090	0.91	0.801882826	1.41	0.953852439	1.91	0.993089940
0.42	0.447467618	0.92	0.806767722	1.42	0.955376179	1.92	0.993378225
0.43	0.456886695	0.93	0.811563559	1.43	0.956857253	1.93	0.993655650
0.44	0.466225115	0.94	0.816271019	1.44	0.958296570	1.94	0.993922571
0.45	0.475481720	0.95	0.820890807	1.45	0.959695026	1.95	0.994179334
0.46	0.484655390	0.96	0.825423650	1.46	0.961053510	1.96	0.994426275
0.47	0.493745051	0.97	0.829870293	1.47	0.962372900	1.97	0.994663725
0.48	0.502749671	0.98	0.834231504	1.48	0.963654065	1.98	0.994892000
0.49	0.511668261	0.99	0.838508070	1.49	0.964897865	1.99	0.995111413

Z	erf(Z)	Z	erf(Z)	Z	erf(Z)	Z	erf(Z)
2.00	0.995322265	2.50	0.999593048	3.00	0.999977910	3.50	0.999999257
2.01	0.995524849	2.51	0.999614295	3.01	0.999979261	3.51	0.999999309
2.02	0.995719451	2.52	0.999634501	3.02	0.999980534	3.52	0.999999358
2.03	0.995906348	2.53	0.999653714	3.03	0.999981732	3.53	0.999999403
2.04	0.996085810	2.54	0.999671979	3.04	0.999982859	3.54	0.999999445
2.05	0.996258096	2.55	0.999689340	3.05	0.999983920	3.55	0.999999485
2.06	0.996423462	2.56	0.999705837	3.06	0.999984918	3.56	0.999999521
2.07	0.996582153	2.57	0.999721511	3.07	0.999985857	3.57	0.999999555
2.08	0.996734409	2.58	0.999736400	3.08	0.999986740	3.58	0.999999587
2.09	0.996880461	2.59	0.999750539	3.09	0.999987571	3.59	0.999999617
2.10	0.997020533	2.60	0.999763966	3.10	0.999988351	3.60	0.999999644
2.11	0.997154845	2.61	0.999776711	3.11	0.999989085	3.61	0.999999670
2.12	0.997283607	2.62	0.999788809	3.12	0.999989774	3.62	0.999999694
2.13	0.997407023	2.63	0.999800289	3.13	0.999990422	3.63	0.999999716
2.14	0.997525293	2.64	0.999811181	3.14	0.999991030	3.64	0.999999736
2.15	0.997638607	2.65	0.999821512	3.15	0.999991602	3.65	0.999999756
2.16	0.997747152	2.66	0.999831311	3.16	0.999992138	3.66	0.999999773
2.17	0.997851108	2.67	0.999840601	3.17	0.999992642	3.67	0.999999790
2.18	0.997950649	2.68	0.999849409	3.18	0.999993115	3.68	0.999999805
2.19	0.998045943	2.69	0.999857757	3.19	0.999993558	3.69	0.999999820
2.20	0.998137154	2.70	0.999865667	3.20	0.999993974	3.70	0.999999833
2.21	0.998224438	2.71	0.999873162	3.21	0.999994365	3.71	0.999999845
2.22	0.998307948	2.72	0.999880261	3.22	0.999994731	3.72	0.999999857
2.23	0.998387832	2.73	0.999886985	3.23	0.999995074	3.73	0.999999867
2.24	0.998464231	2.74	0.999893351	3.24	0.999995396	3.74	0.999999877
2.25	0.998537283	2.75	0.999899378	3.25	0.999995697	3.75	0.999999886
2.26	0.998607121	2.76	0.999905082	3.26	0.999995980	3.76	0.999999895
2.27	0.998673872	2.77	0.999910480	3.27	0.999996245	3.77	0.999999903
2.28	0.998737661	2.78	0.999915587	3.28	0.999996493	3.78	0.999999910
2.29	0.998798606	2.79	0.999920418	3.29	0.999996725	3.79	0.999999917
2.30	0.998856823	2.80	0.999924987	3.30	0.999996942	3.80	0.999999923
2.31	0.998912423	2.81	0.999929307	3.31	0.999997146	3.81	0.999999929
2.32	0.998965513	2.82	0.999933390	3.32	0.999997336	3.82	0.999999934
2.33	0.999016195	2.83	0.999937250	3.33	0.999997515	3.83	0.999999939
2.34	0.999064570	2.84	0.999940898	3.34	0.999997681	3.84	0.999999944
2.35	0.999110733	2.85	0.999944344	3.35	0.999997838	3.85	0.999999948
2.36	0.999154777	2.86	0.999947599	3.36	0.999997983	3.86	0.999999952
2.37	0.999196790	2.87	0.999950673	3.37	0.999998120	3.87	0.999999956
2.38	0.999236858	2.88	0.999953576	3.38	0.999998247	3.88	0.999999959
2.39	0.999275064	2.89	0.999956316	3.39	0.999998367	3.89	0.999999962
2.40	0.999311486	2.90	0.999958902	3.40	0.999998478	3.90	0.999999965
2.41	0.999346202	2.91	0.999961343	3.41	0.999998582	3.91	0.999999968
2.42	0.999379283	2.92	0.999963645	3.42	0.999998679	3.92	0.999999970
2.43	0.999410802	2.93	0.999965817	3.43	0.999998770	3.93	0.999999973
2.44	0.999440826	2.94	0.999967866	3.44	0.999998855	3.94	0.999999975
2.45	0.999469420	2.95	0.999969797	3.45	0.999998934	3.95	0.999999977
2.46	0.999496646	2.96	0.999971618	3.46	0.999999008	3.96	0.999999979
2.47	0.999522566	2.97	0.999973334	3.47	0.999999077	3.97	0.999999980
2.48	0.999547236	2.98	0.999974951	3.48	0.999999141	3.98	0.999999982
2.49	0.999570712	2.99	0.999976474	3.49	0.999999201	3.99	0.999999983

Example #1

- Starting with n-type Si<100>, $N_D=10^{14}cm^{-3}$, how long do we need to to a “infinite source” B diffusion at 1000°C to make a junction depth (x_j) equal to .5 $\times 10^{-4}$ cm?

Example #2

- Starting with p-type Si<111>, $N_A=10^{15}cm^{-3}$, how deep will the junction depth (x_j in cm) if we do an "infinite source" P *pre-dep* diffusion at 1000^{o}C for 10 minutes?
- What will be the junction depth (x_j in cm) if we do an "finite source" P *drive in* diffusion at 1000^{o}C for 30 minutes?

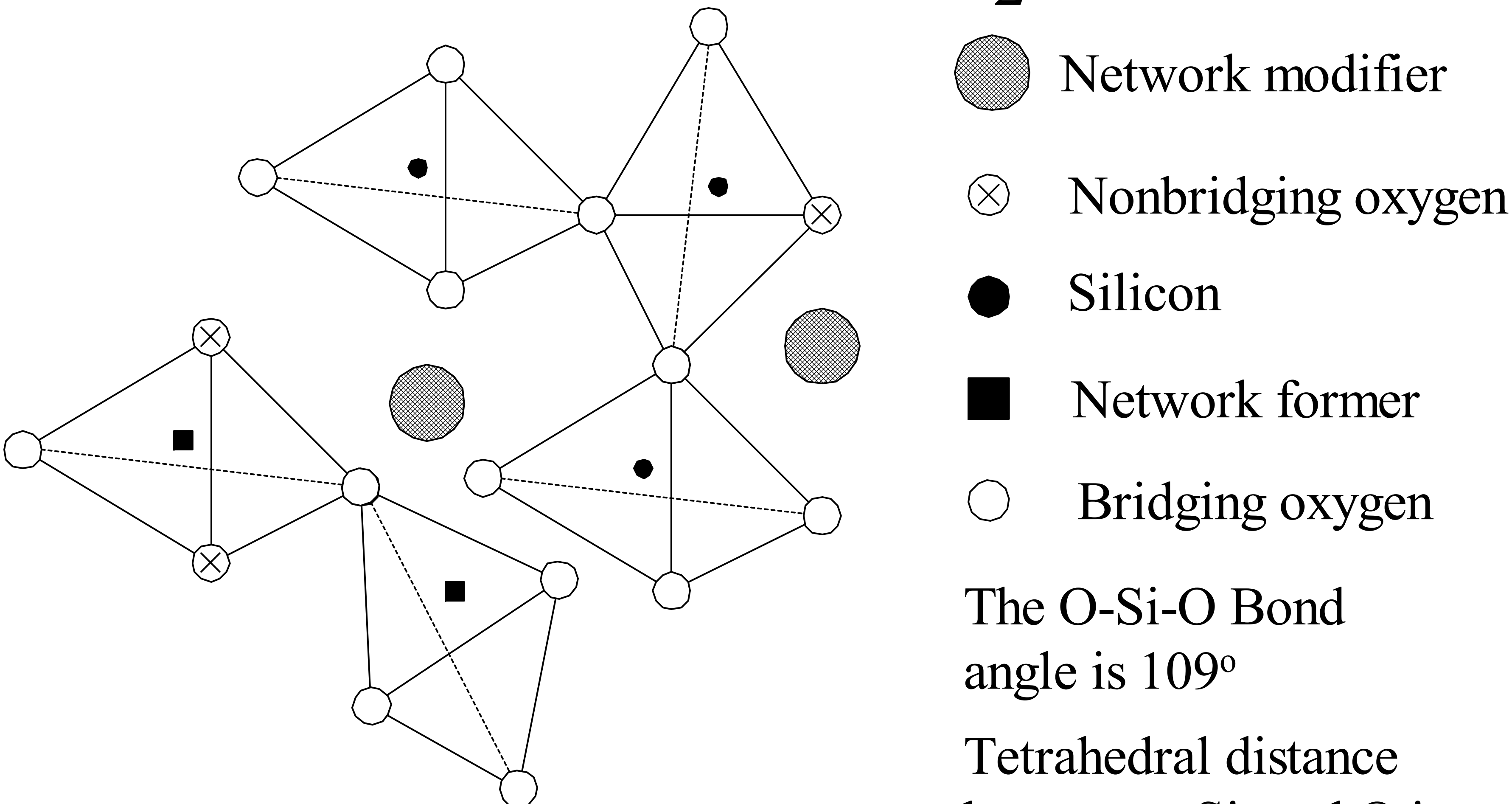
Silicon dioxide

- What is SiO_2?
- What is SiO_2 used for?
- Advantages and Disadvantages of SiO_2
- How is it grown?
  - Dry
  - Wet
- Numerical Examples

What is SiO_2?

- Two forms
  - Single crystal (quartz)
  - Amorphous
- We are interested in Amorphous SiO_2
  - Random three dimensional network of SiO_2 constructed from polyhedra of oxygen ions.
  - This material is more porous than Quartz (density of 2.15-2.25g/cm^3 compared to 2.65 25g/cm^3)

What is SiO_2?

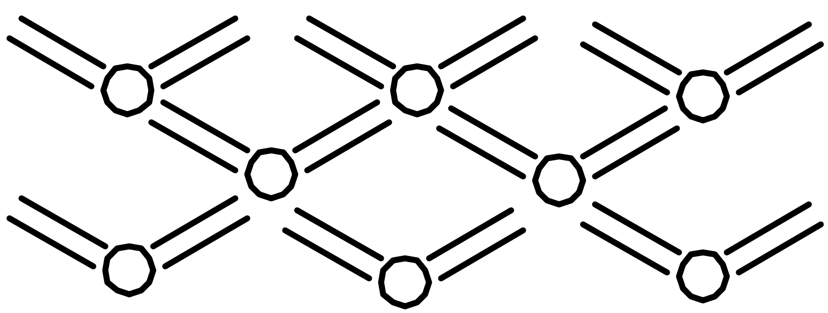


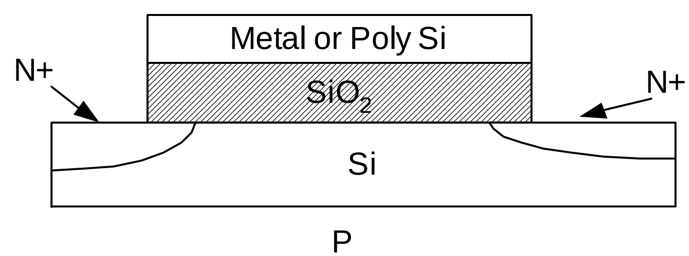
The O-Si-O Bond angle is 109^{o}

Tetrahedral distance bewtween Si and O ions is 1.6Å

What is SiO_2 used for?

- MOS Metal Oxide Semiconductor
- Device passivation
  - Combines with dangling bonds to reduce surface states



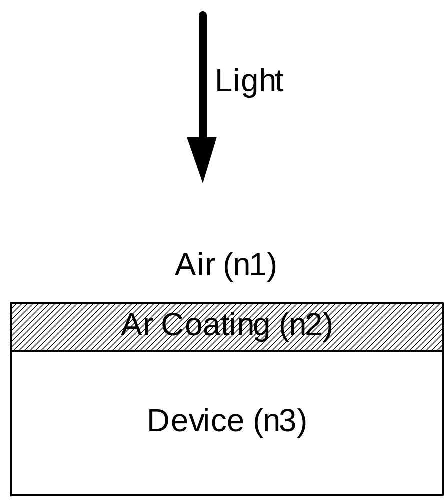


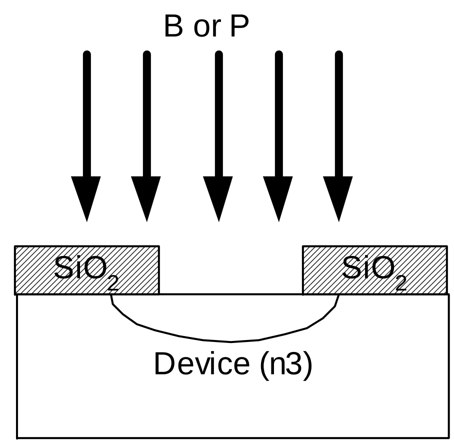
What is SiO_2 used for?

- Diffusion Masks
  - Block the diffusion of B and P for example
- Antireflective coating for Photodevices

$$n_2 = \sqrt{n_1 n_3},$$

$$\text{thickness} = \frac{\lambda}{4n_2}$$





Advantages and Disadvantages of SiO_2

- CMOS digital logic gates use little power when not switching logic state, thus high levels of integration are possible because the standby power consumption is low.
- SiO_2 is a native film that is quite easy to grow. All that is required is heat and oxygen or steam.

Advantages and Disadvantages of SiO_2

- SiO_2 consumes Si while growing. 44% of the SiO_2 layer comes from the original Si.
  - This leads to a non-planer structure after each oxidation step.
- Due to the large increase in volume there is 2-4×109 dyn cm-1 of compressive strain.
  - This causes dislocations.
- Oxidation-Induced Stacking Faults (these can be removed by a high temp treatment.

Advantages and Disadvantages of SiO_2

- The large dielectric constant leads to larger capacitance values for a given thickness (compared to silicon nitride).

How is it grown?

- The oxidizing species must diffuse through the $SiO2$ layer that has already grown. This leads to a linear regime of growth and a parabolic regime of growth. Given by the equation:

$$X^2 + A(\mu m)X = B(\mu m^2/hr)t(hr)$$

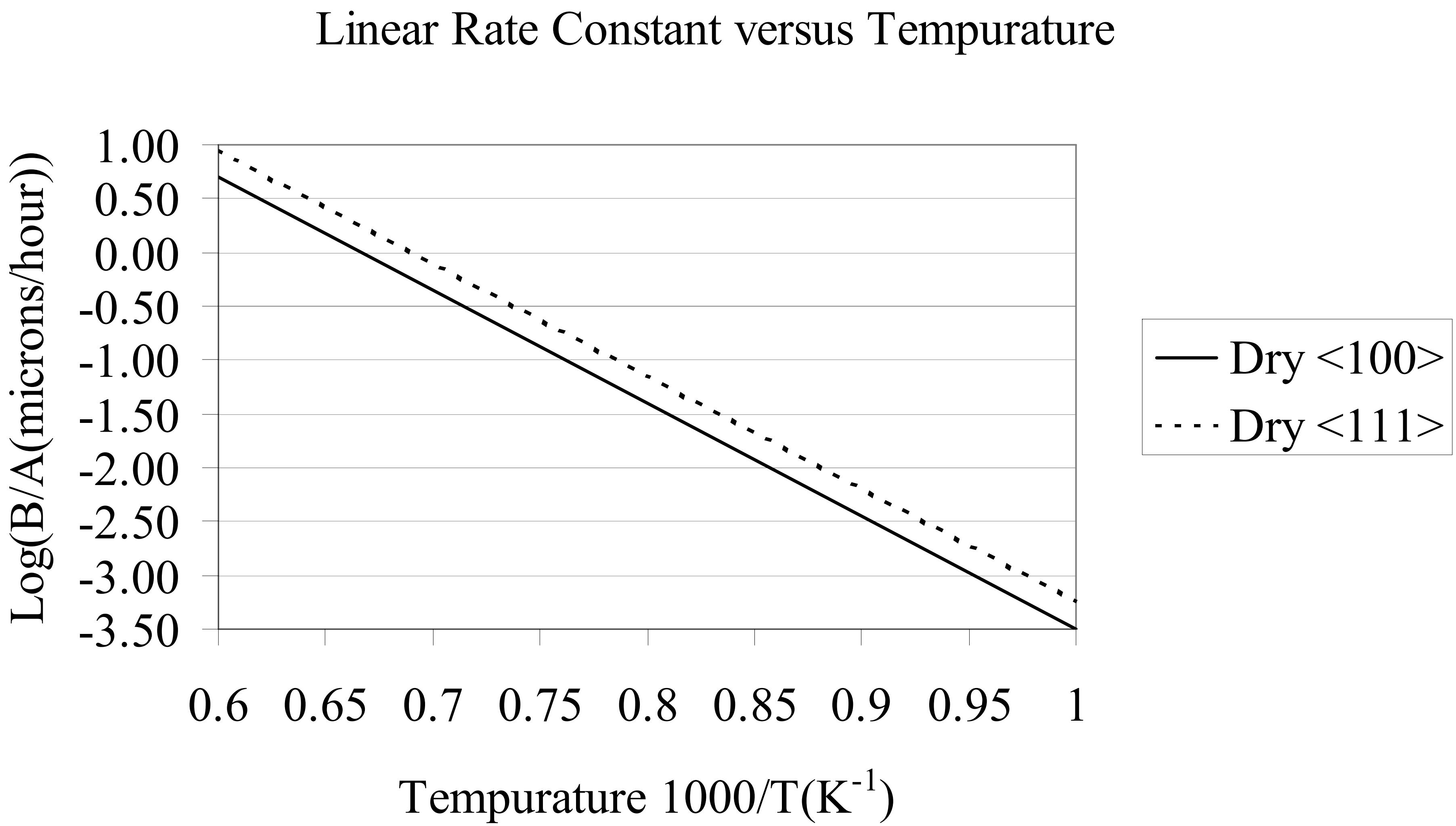
How is it grown?

- Dry oxidation: Flow dry O2 over sample at elevated temperatures.

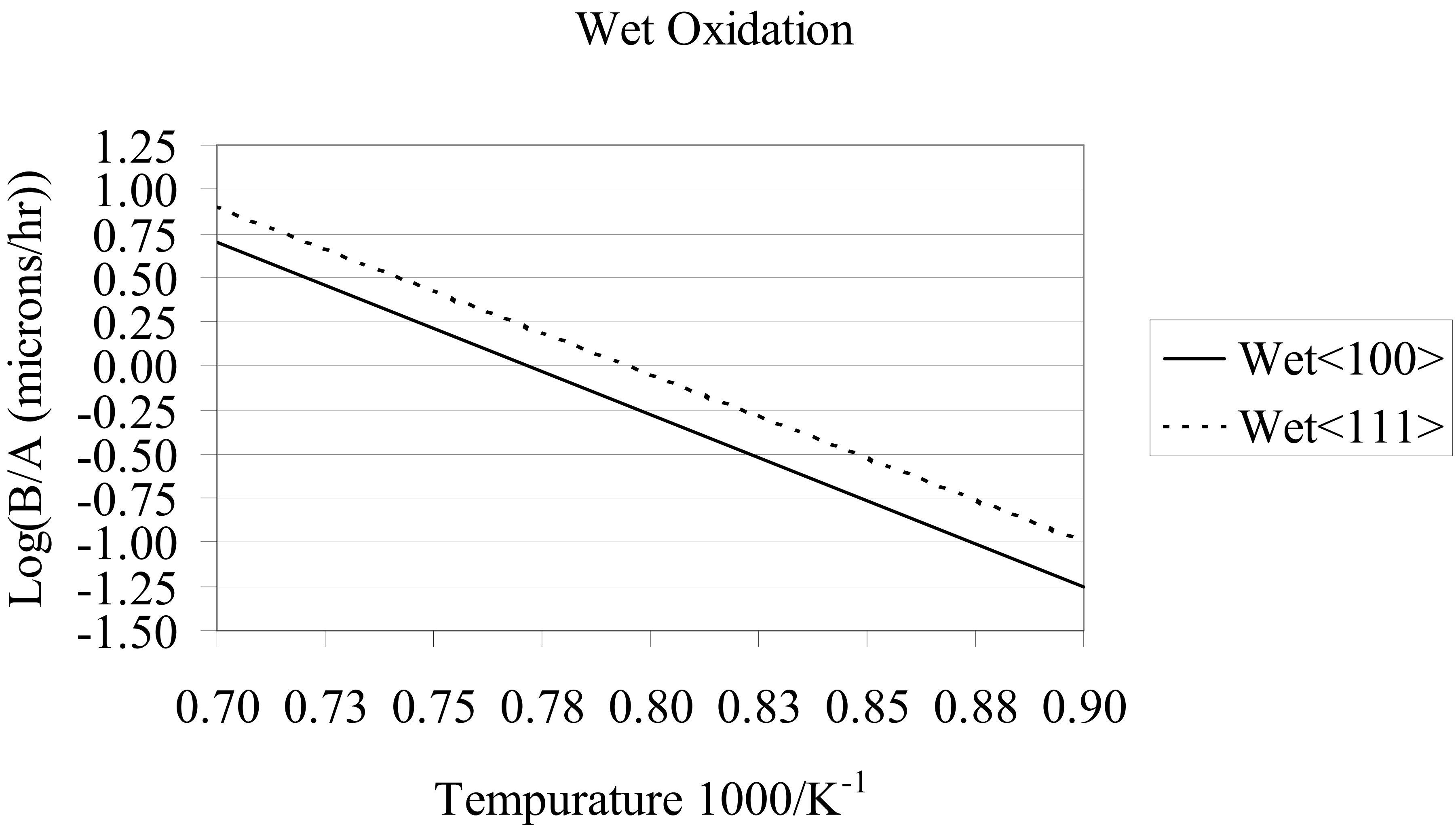
$$Si + O_2 \longrightarrow SiO_2$$

- Wet oxidation: Bubble N_2 through a water bubbler @95C^o over sample at elevated temperatures.

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

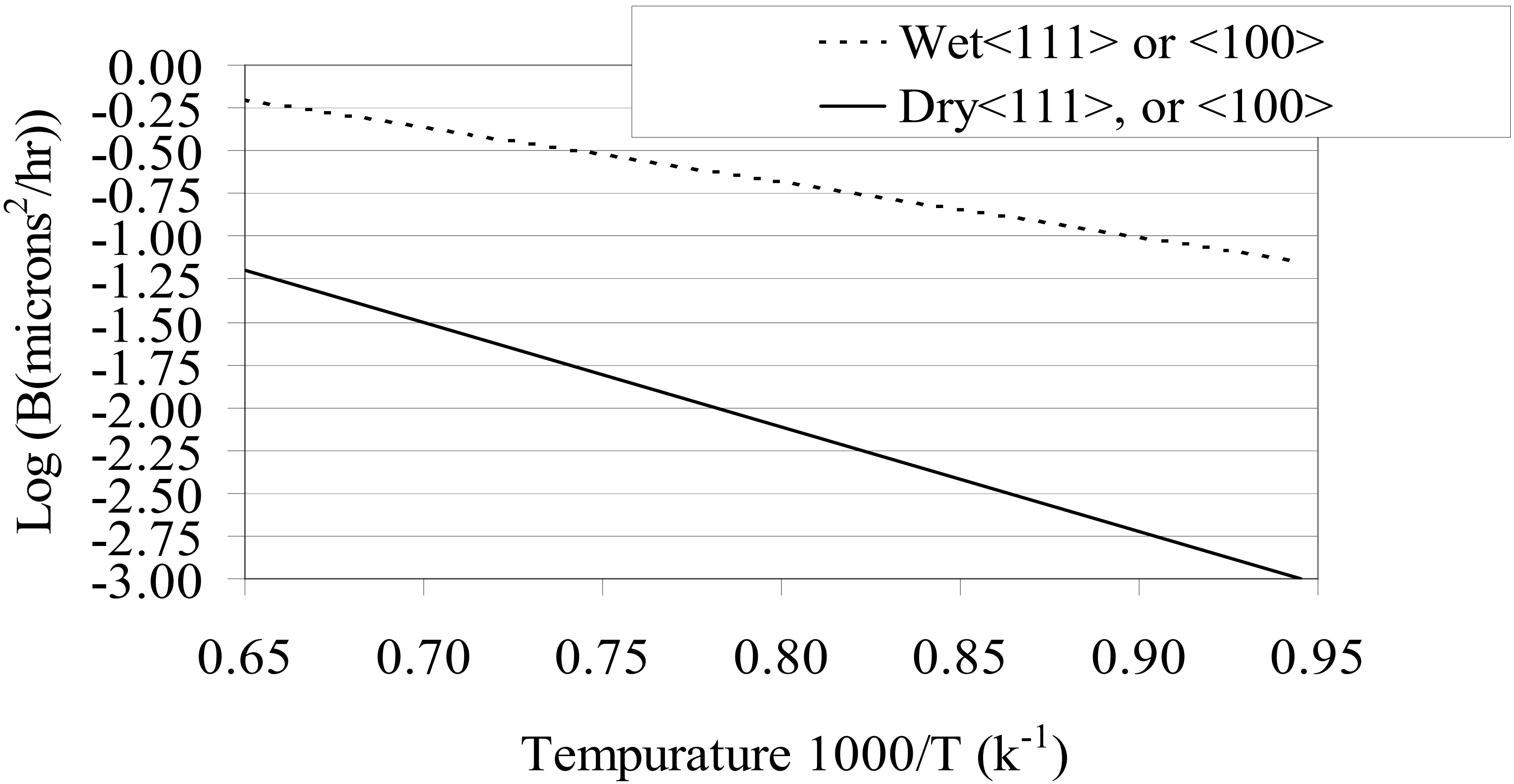


Linear Rate Constant versus Tempurature
Log(B/A(microns/hour))
1.00
0.50
0.00
-0.50
-1.00
-1.50
-2.00
-2.50
-3.00
-3.50
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
1
Tempurature 1000/T(K-1)
Dry <100>
Dry <111>



Wet Oxidation
1.25
1.00
0.75
0.50
0.25
0.00
-0.25
-0.50
-0.75
-1.00
-1.25
-1.50
Log(B/A (microns/hr))
0.70 0.73 0.75 0.78 0.80 0.83 0.85 0.88 0.90
Tempurature 1000/K-1
Wet<100>
Wet<111>

Parabolic Rate Constant versus Tempurature



Numerical Examples

- How long do we need to grow SiO_2 at $1155C^o$ using a wet process<111> to protect against a 30 minute$1100C^o$ P diffusion?
- How long do we need to grow SiO_2 at $1265C^o$ using a dry process<100> to create a MOS insulator capacitance ($C_i=\varepsilon_i/d$) of 69nF?
  - Note: For SiO2 ε_i=3.9*8.85e-14F/cm

Photolithography I

- Without photolithography there would be no integrated circuits because every process done to a wafer to fabricate diodes and transistors (implantation, oxidation, diffusion, and etching), would be done to the whole surface of the wafer. We would be limited to diodes and MOS capacitors the size of the wafer (Yes we could cut the wafer up into parts, but this is quite limited.)

Photolithography

- Our Process:
  - Singe
  - Spin on photoresist
  - Pre-Bake
  - Expose
  - Develop
  - Post-Bake
  - Etch
  - Remove photoresist

Singe

- What is it?
  - Heat wafers to about 800 ^oC for five minutes in.
- Why do we do it?
  - SiO_2 and Si attract water and absorb it.
  - Photoresist repels water, thus if the SiO_2 or Si have absorbed water, the photoresist will not stick.
  - We can also ash particles on the wafers.

Spin on photoresist

- What is it?
  - Photoresist is a photosensitive film that can be selectively patterned, and can protect the underlying structures from your etch process. It is a polymer that contains a interlocking mechanism, photosensitive chemicals, and solvents.
- Why do we spin it on?
  - Spinning it on is the quickest way to uniformly coat the wafer with photoresist.
  - It also drys out the solvent from the PR.

Spin on photoresist

- Problems?
  - Most of the PR is spun off the wafer. PR is about $900 per gallon.

Pre-Bake

- What is it?
  - Bake the wafers for 90 ^{o}C for 30 minutes.
- Why do we do it?
  - Drive out solvent
    - Convert liquid to solid
  - Relieve stress during spin on step
- It needs to be carefully optimized with exposure time. Too much softbake and the film will not be very sensitive to the developer. Too little and the film will be too sensitive.

Expose

- What is it?
  - Selectively expose the PR coated wafers with UV light with a predetermined amount of energy.
- Why do we use UV light?
  - We can resolve features down to about $\lambda/2$.

Develop

- What is it?
  – Mechanically agitate the exposed wafers in a developer solution.
- Why do we do it?
  – This removes the PR that we do not want. We have a selective pattern on the sample that will protect features from etching.

Post-Bake

- What is it?
  - We post-bake at 120^{o}C for 20 minutes
- Why do we do it?
  - This drives out all the elements that would allow the PR to be attacked by the etch.

Etch or Process

- Once we have completed these step we have to remove oxide so that we can diffuse n or p, implant or grow a different quality oxide on the wafer.
- Note: We are not able to diffuse or oxidize until we have removed the patterning PR.

Etching Goals

- Primary goal is precisely transfer the features on the mask into the underlying material.
  - Hily selective against mask layer material
  - Highly selective again material under layer to be etched.
  - Should be uniform.
  - Etch rate should be as high as possible.
  - Process should be safe.
  - Should not cause damage to the substrate or devices
  - Etch residues should be easily removed.
  - Should be clean.
  - Conductive to full automation.

Topics

- Goals
- Definitions
- Wet Techniques
- Dry Techniques
- Our Process

Definitions

- Bias: Error in the lateral dimension of image transfer.
- Tolerance: Statistical variation of the bias
- Etch Rate: Rate of film removal
  - Vertical and Horizontal
- Anisotropy: How selective to direction the etch is.
  - Anisotropic: Etches is only on direction.
  - Isotropic: Etches in all directions equally.
- Selectivity: Ratio of etch rates to underlying material (Sfs) or ratio of etch rates to mask (Sfm)
- Over Etch: How much extra etching you have to perform to clear all etched areas on a wafer to take into account variences in the thickness and etch rates across the wafer, wafer to wafer or run to run.

Numerical Examples:

$$Etch\_Rate\_Max := .2\cdot 10^{-4}\frac{cm}{s}$$

$$Etch\_Rate\_Min := .1\cdot 10^{-4}\frac{cm}{s}$$

$$Etch\_Rate\_Uniformity := \frac{Etch\_Rate\_Max - Etch\_Rate\_Min}{Etch\_Rate\_Max + Etch\_Rate\_Min}\cdot 100$$

$$Etch\_Rate\_Uniformity = 33.333$$

$$Horizontal\_Etch\_Rate := .2\cdot 10^{-4}\frac{cm}{s}$$

$$Vertical\_Etch\_Rate := .2\cdot 10^{-4}\frac{cm}{s}$$

$$L_R := \frac{Horizontal\_Etch\_Rate}{Vertical\_Etch\_Rate} \qquad L_R = 1$$

$$A := 1 - L_R \qquad A = 0$$

Mean Thinckness $h_f := .4\cdot 10^{-4}cm$

Varation $\delta := .1$ 10%

Mean Etch Rate $\nu_f := .02\cdot 10^{-4}\frac{cm}{s}$

Variation $\phi_f := .1$

Maximum line width loss occurs where material is thicknest, etch rate is slowest, and thus the time is longest.

Fraction of ever etch time $\Delta := .2$

$$t_c := \frac{h_f\cdot(1+\delta)\cdot(1+\Delta)}{\nu_f\cdot(1-\phi_f)} \qquad t_c = 29.333\,s$$

The mask has a horizontal and vertical etch rate

$$\nu_{ml} := .005\cdot 10^{-4}\frac{cm}{s} \qquad \nu_{mv} := .005\cdot 10^{-4}\frac{cm}{s}$$

Assume a 60 degree sidwall

$$\theta := \frac{60}{180}\cdot\pi \qquad \theta = 1.047$$

Total line width loss

$$W := 2\cdot\nu_{mv}\cdot h_f\cdot(1+\delta)\cdot\frac{(1+\Delta)}{\nu_f\cdot(1-\phi_f)}\cdot\left(\cot(\theta) + \frac{\nu_{ml}}{\nu_{mv}}\right) \qquad W = 4.627\times 10^{-5}\,cm$$

Wet Techniques

- HF for silicon dioxide or “Al” Etch for Al
- Selectivities over the mask and substrate are quite high.
- Cheap to buy and run
- Completely isotropic (Etches is all directions at the same time.)

Dry Techniques

- Reactive Ion Etch
  - Low pressure
  - Physical and chemical
  - Directional
  - More selective than sputtering
  - Radiation damage

Dry Techniques

- Plasma
  - higher pressure
  - chemical
  - Isotropic
  - Selective
  - No Radiation Damage

Our Process

- 45mTorr
- -600V
- 45ccm Triflouromethane (CHF_3)
- 8ccm oxygen
- Antisymetrical (RIE)
- Anisotropic
- Selective over Si

Some Reported Parameters

Material	Gas	Etch Rate	Etch Rate Ratio to other materials	To Resist
SiO_2	CHF_3	220	11(Si)	5.5
SiO_2	CHF_3	450	15 (poly-Si)	20
SiO_2	CHF_3	300	20 (Si)	13

H. Toyoda, Journal of Electronic Materials, no. 9, pp 569, (1980)

Etching

EE/MatE129

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Ion implantation

- Ions are accelerated and purified and then impacted into a semiconductor film.
- As, B, P for example
- Energy is how far the ions will go, and dose is how many ions.
- Forms and very narrow Gaussian distribution
- Damages the Crystal so wafers need to e annealed to activate the impurities and heal crystal damage
- Can very accurately control threshold voltages.

Ion Implantation

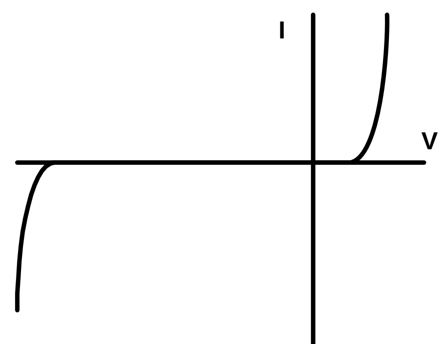
- Ions can be channeled through the lattices
- Screen oxide prevents this.

Metalization

- Metal can be deposited through CVD, sputter or thermal evaporation.
- It needs to be annealed to make an ohmic contact with the substrate.
- Tungsten might replace poly-silicon Gates
- Tungsten is already used to “plug” the vias so the Al will not punch though the pn junction.

Why are diodes important?

- Small low power lasers/detectors
- Solar Cells "Free Clean Energy" from the sun. No oil required
- Detect hazardous gasses
- Used in all transistors
- Current flows easily one way, but not the other (rectifiers)
- All these functions can be integrated on one die



The contact potential

- It is the contact potential or built in electric field that controls the useful properties of diodes. It controls at what voltage a diode will turn on, and how much voltage can be extracted from a solar cell. It is the “Vbe” used in calculating BJT DC operating points.

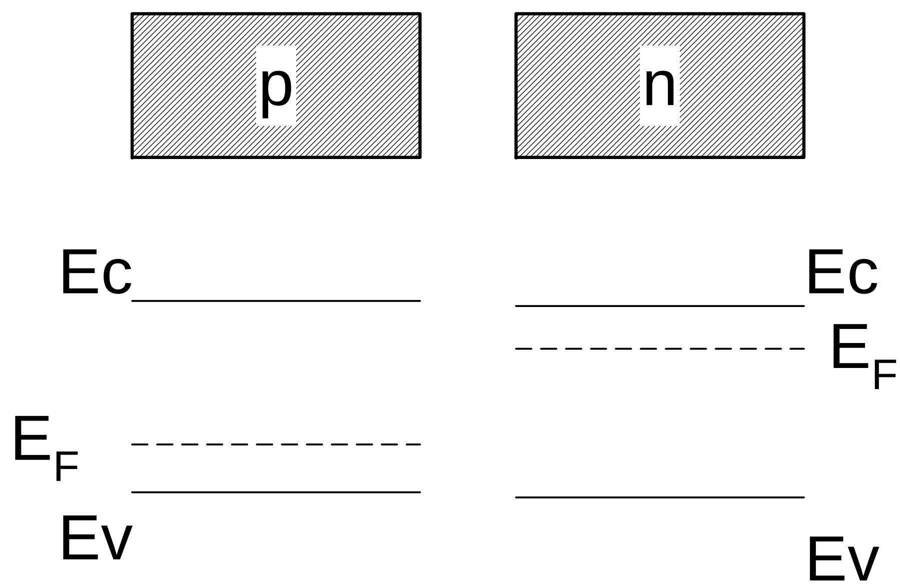
Where does the contact potential come from?

- Equilibrium (No current flows).
- When a pn junction is fabricated
  - $n_n > n_p$
  - $p_p > p_n$
- This causes the electrons to diffuse into the p side and the holes to diffuse into the n side of the semiconductor

The contact potential

- This causes an electron and hole gradient which in turn causes an electric field to be set up.
- This electric field causes a drift current to occur in the opposite direction of the diffusion current.
- In thermal equilibrium these currents are equal and opposite (No current flows.)

The contact potential



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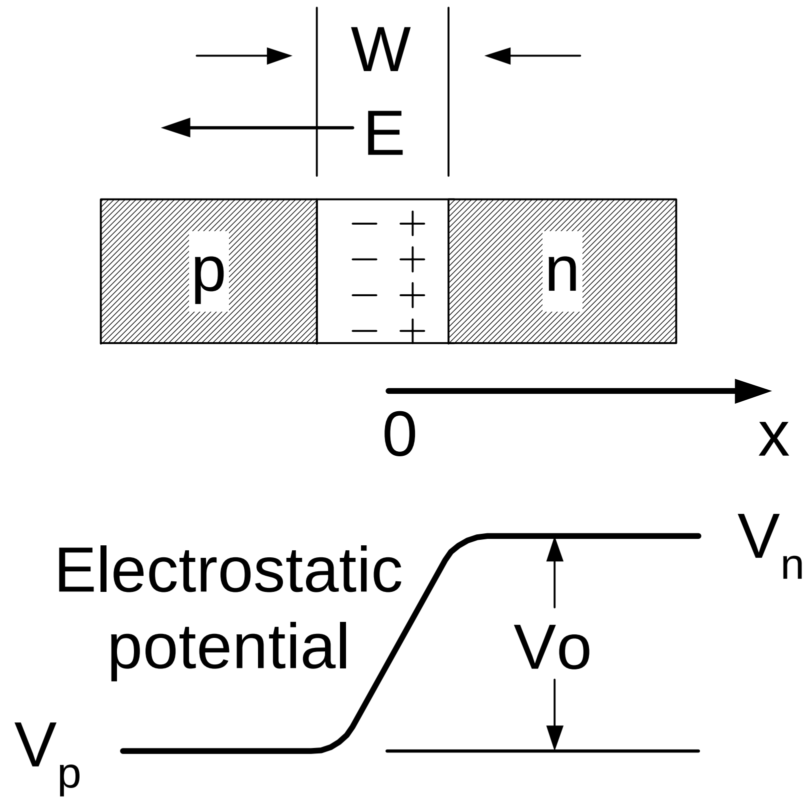
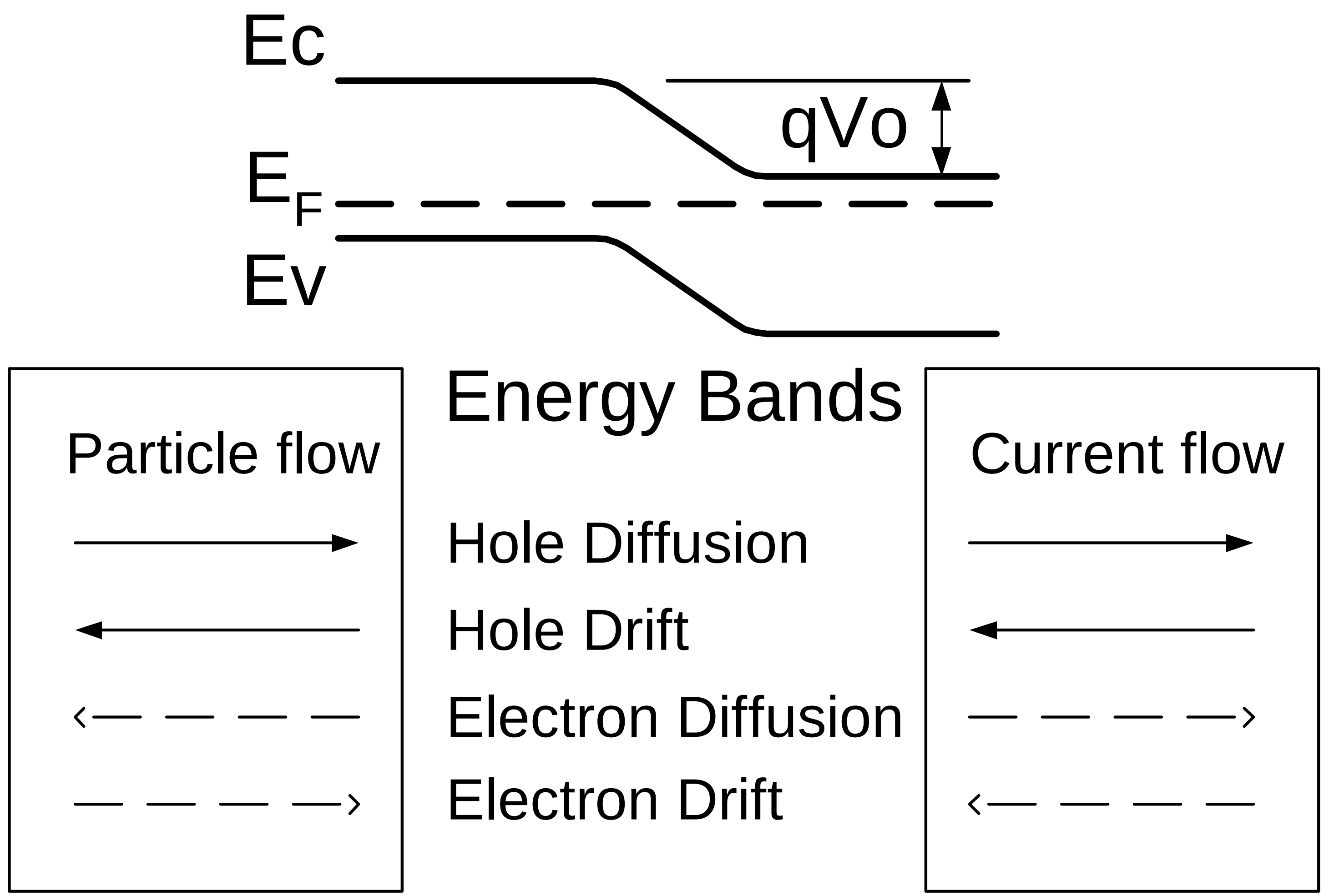


The contact potential



The contact potential

$$J_p(x) = q\left[\mu_p p(x)E(x) - D_p \frac{dp(x)}{dx}\right] = 0 \qquad E(x) = -\frac{dV(x)}{dx}$$

$$-\frac{q}{kT}\int_{Vp}^{Vn} dV = \int_{p_p}^{p_n} \frac{1}{q} dp \qquad \frac{D_p}{\mu_p} = \frac{kT}{q}$$

$$Vo = \frac{kT}{q}\ln\left(\frac{p_p}{p_n}\right), \text{assume a step junction, and that } p_p = N_a$$

$$\text{and } n_n = N_d, \text{ along with } p_p n_p = ni^2 = p_n n_n$$

$$Vo = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^{\ 2}}\right)$$

*

Equilibrium Fermi Levels

- Although the fermi level is flat throughout the semiconductor, its relative position to the conduction and valence bands is not.
- The result of this is that the distance from the Fermi level to the intrinsic level does change.
- The difference in these differences is qVo
- Being able to interpret EBDs will demonstrate to future employers that you have a basic understanding of semiconductor physics (which would be true)

Space charge at the junction

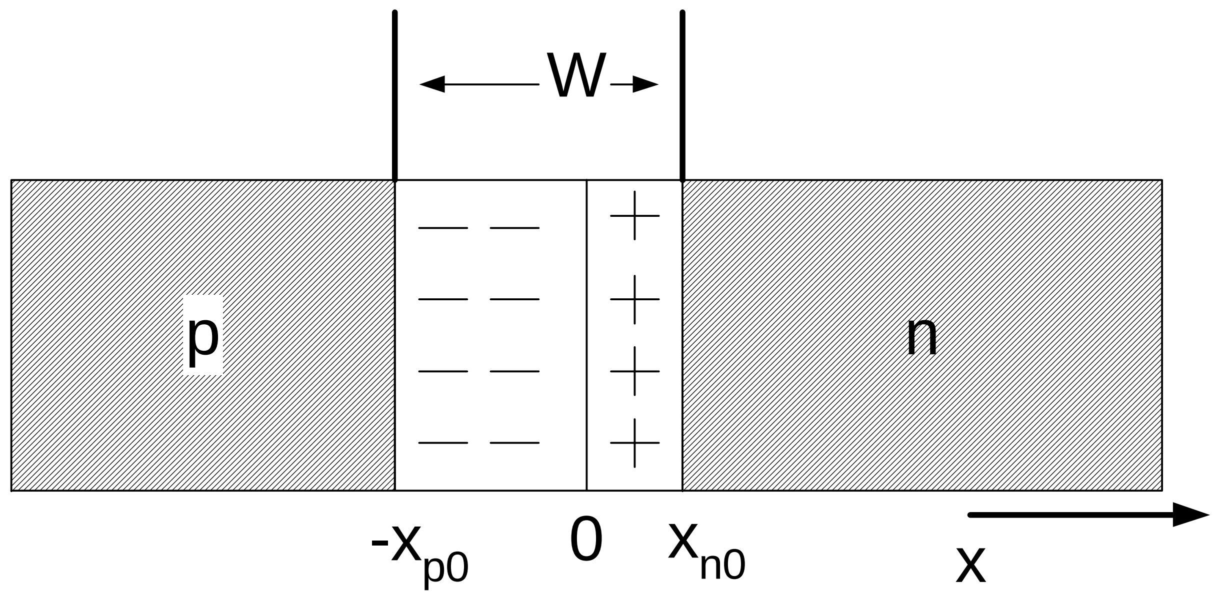
- Depletion approximation
  - All the carriers are depleted inside of W
  - Outside of W is neutral
  - At high current levels this breaks down

$$Q_+ = |Q_-|,$$

$$Q_+ = qAX_{n0}N_d$$

$$Q_- = -qAX_{p0}N_a$$

Space charge at the junction



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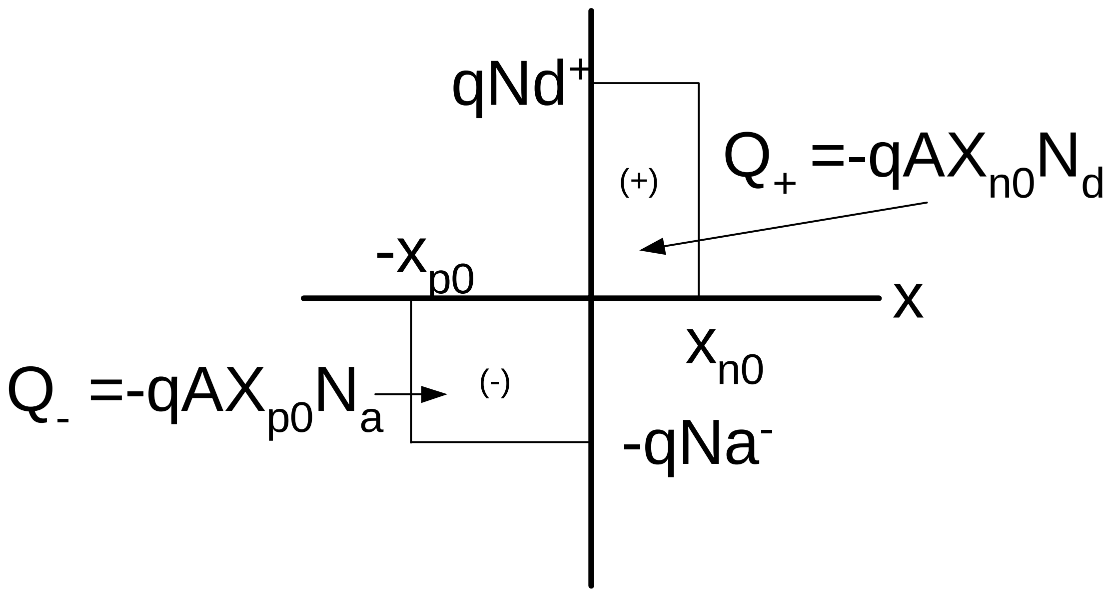

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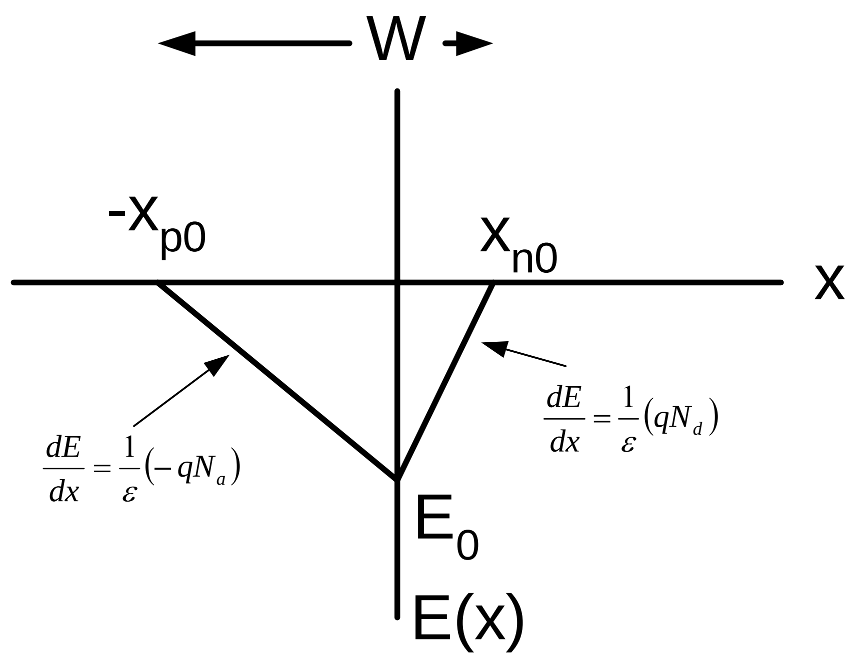


Space charge at the junction

- Poisson's equation
  - Needed to calculate electric field
  - Relates the gradient of the electric field to the local space charge

$$\frac{dE(x)}{dx} = \frac{q}{\varepsilon}\left(p - n + N_d^{\ +} - N_a^{\ -}\right)$$

$$\frac{dE(x)}{dx} = \frac{q}{\varepsilon} N_d , 0 < \mathrm{x} < \mathrm{x}_{\mathrm{no}}, N_d^{\ +} = N_d$$

$$\frac{dE(x)}{dx} = -\frac{q}{\varepsilon} Na, \text{-}\,\mathrm{x}_{\mathrm{p0}} < \mathrm{x} < 0, N_a^{\ -} = N_a$$

Space charge at the junction

- Poisson's equation
  - Integrate both sides and use the fact that the electric field must be equal on both sides of the junction. Will <Vx> Saturate going through a pn junction?

$$Eo = -\frac{q}{\varepsilon} N_d x_{no} = -\frac{q}{\varepsilon} N_a x_{po}$$

- Now we can find V_o by integrating Poison's equation again

$$V_o = \frac{1}{2}\frac{q}{\varepsilon}\frac{N_a N_d}{N_a + N_d} W^2$$

Space charge at the junction

- Now we can find the depletion width as a function of doping concentrations

$$W = \left[\frac{2\varepsilon kT}{q^2} \left(\ln \frac{N_a N_d}{n_i^{\,2}} \right) \left(\frac{1}{N_a} + \frac{1}{N_d} \right) \right]^{\frac{1}{2}}$$

$$x_{p0} = \left\{ \frac{2\varepsilon kT(V_o - V)}{q} \left[\frac{N_d}{N_a (N_a + N_d)} \right] \right\}^{\frac{1}{2}}$$

$$x_{n0} = \left\{ \frac{2\varepsilon kT(V_o - V)}{q} \left[\frac{N_a}{N_d (N_a + N_d)} \right] \right\}^{\frac{1}{2}}$$

*

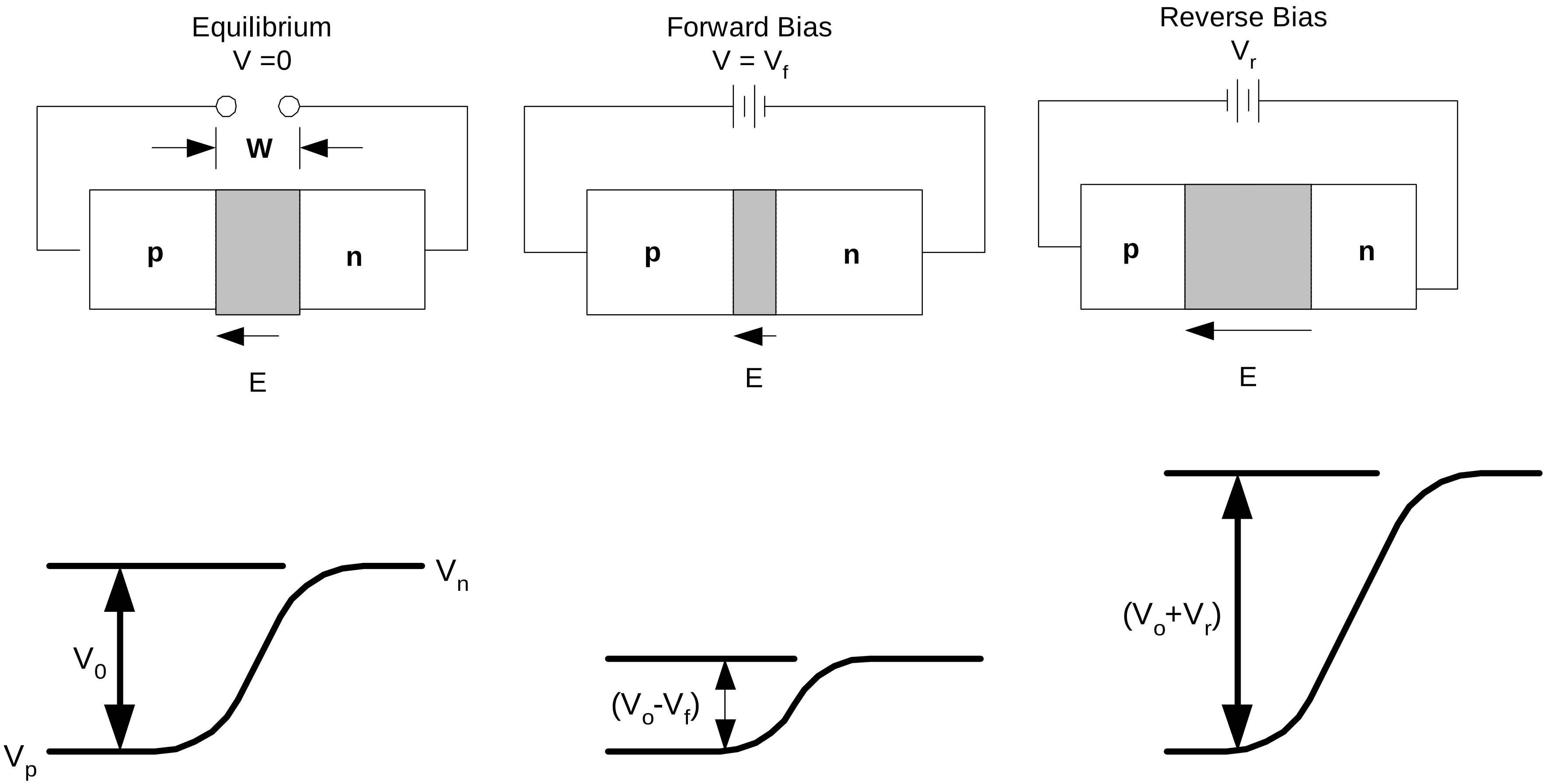
P.E.

- Nitrogen (N_a=10^{16}cm^{-3}) and Chlorine (N_d=10^{18}cm^{-3}) are used to make an abrupt pn junction in ZnSe and the radius of the circular device is .02in.
- Calculate V_o, x_{n0}, x_{p0}, E_o for this junction at equilibrium for 300K.
- Eg=2.7eV, m_e^*=.17, m_h^*=1.1, dielectric constant=$9\times8.85\times 10^{-14}$ F/cm

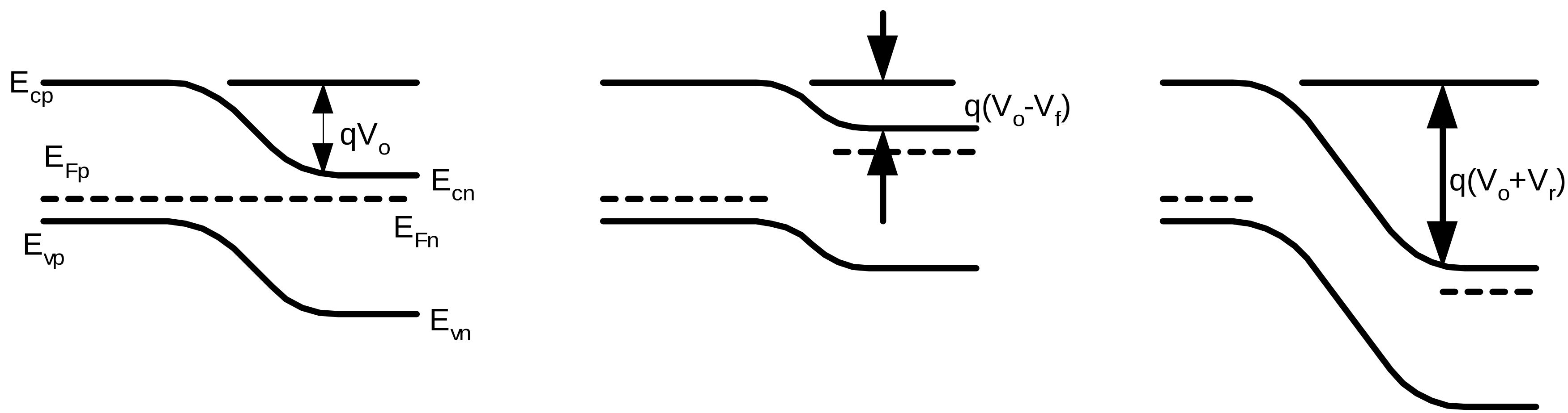
Non-equilibrium conditions in a pn junction

- Equilibrium, forward bias, reverse bias
- Carrier injection
- Calculating junction current
- Minority and majority currents
- Diode equation example

Equilibrium, forward bias, reverse bias



Equilibrium, forward bias, reverse bias



Equilibrium, forward bias, reverse bias

- Equilibrium
  - The Hole and electron drift and diffusion currents cancel each other out. No net current.
- Forward bias
  - The junction potential is lowered by an applied electric field.
- Reverse bias
  - The junction potential is increased by an applied electric field.

Equilibrium, forward bias, reverse bias

- Equilibrium
  - W does not change.
- Forward bias
  - W is smaller substitute (V_o-V) for V_o in equation for W.
- Reverse bias
  - W is larger substitute (V_o+V) for V_o in equation for W.

Equilibrium, forward bias, reverse bias

- Equilibrium
  - E_{Fp}=E_{Fn} flat throughout .
- Forward bias
  - E_{Fp}(J) and E_{Fn} (J) are separated by $q(V_f)$ (J) .
- Reverse bias
  - E_{Fp}(J) and E_{Fn} (J) are separated by $q(V_r)$ (J) .

Equilibrium, forward bias, reverse bias

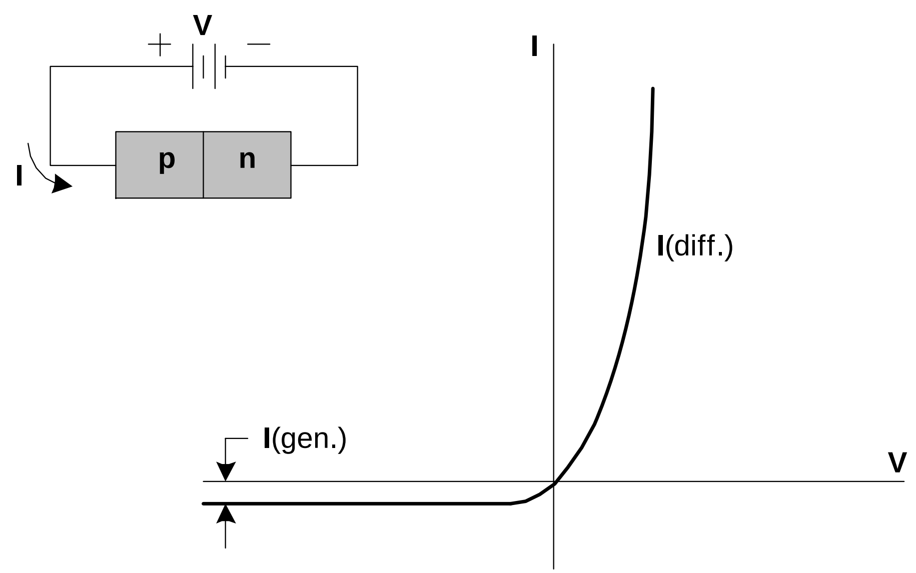
- Equilibrium
  - No net current .
- Forward bias
  - Diffusion current is increased because the barrier is lowered and thus more electrons and hole have enough energy to make it through the barrier. Electrons go from the n-side to the p-side. Holes go from the p-side to the n-side.
  - Drift current: small because this depends on the concentration of minority carriers. Thermally generated EHP's (within a diffusion length of W, are the only carriers that contribute to drift, thus independent of applied bias.

Equilibrium, forward bias, reverse bias

- Reverse bias
  - Diffusion current is decreased because the barrier is higher and thus less electrons and hole have enough energy to make it through the barrier. Electrons go from the n-side to the p-side. Holes go from the p-side to the n-side.
  - Drift current: small because this depends on the concentration of minority carriers. Thermal generated EHP's (within a diffusion length of W, are the only carriers that contribute to drift, thus independent of applied bias.

Equilibrium, forward bias, reverse bias

- Equilibrium: $I=I(Diff)-|I(gen)=0|$
- Forward bias: $I = I_o(e^{qV/kT}-1)$
- Reverse bias: $I=I_o$



Carrier injection

- Minority carriers dominate

$$I = qA\left(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p\right)\left(e^{qV/kT} - 1\right)$$

$$D_p = \frac{kT}{q}\mu_p, \; L_p = \sqrt{D_p \tau_p} \qquad p_n = \frac{p_p}{e^{qV_o/kT}} = \frac{N_a}{e^{qV_o/kT}}$$

$$D_n = \frac{kT}{q}\mu_n, \; L_n = \sqrt{D_n \tau_n} \qquad n_p = \frac{n_n}{e^{qV_o/kT}} = \frac{N_d}{e^{qV_o/kT}}$$

Ideality Factor

$$G = \left[\frac{\sigma_p \cdot \sigma_n \cdot \upsilon_{th} \cdot N_t}{\sigma_n \cdot e^{\frac{(E_t - E_i)}{k \cdot T}} + \sigma_p \cdot e^{\frac{(E_i - E_t)}{k \cdot T}}} \right] \cdot n_i$$

$$J_F = A \cdot e^{\frac{q \cdot V}{\eta \cdot k \cdot T}}$$

$$G = \frac{n_i}{\tau_g}$$

$$J_R = q \cdot \sqrt{\frac{D_p}{\tau_p}} \cdot \frac{n_i^2}{N_D} + \frac{q \cdot n_i \cdot W}{\tau_g}$$

Na much larger than Nd

$$J_F = q \cdot \sqrt{\frac{D_p}{\tau_p}} \cdot \frac{n_i^2}{N_D} \cdot e^{\frac{q \cdot V}{k \cdot T}} + \frac{q \cdot n_i \cdot W}{\tau_g} \cdot e^{\frac{q \cdot V}{2k \cdot T}}$$

Calculating junction current

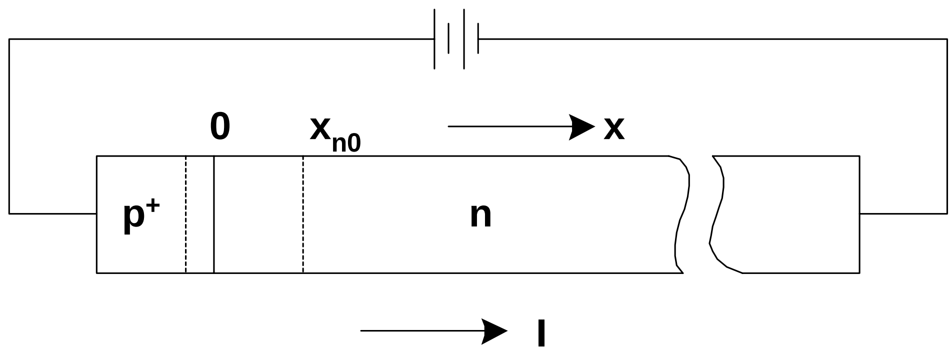
- The mobilities are for electrons in p-type material, and holes in n-type material. An electron in p-type Si material ($Na=10^{17}cm^{-3}$) would have a mobility of 1000 $cm^2/V\ s$
  - A hole in n-type Ge material ($Nd=10^{19}cm^{-3}$) would have a mobility of around 100 $cm^2/V\ s$

Calculating junction current

- Minority carrier lifetimes:

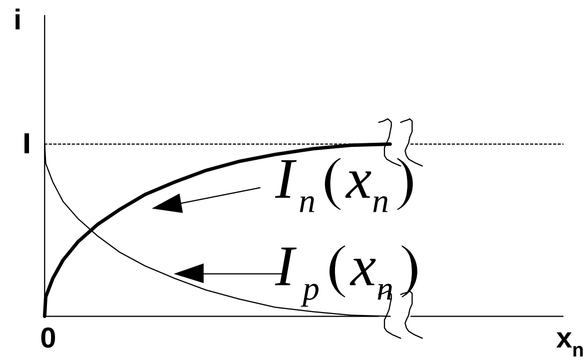
	τ_n	τ_p
Si	10×10^{-6} s	10×10^{-6} s
Ge	10×10^{-7} s	10×10^{-7} s
GaAs	1×10^{-9} s	1×10^{-9} s
ZnSe	1×10^{-9} s	1×10^{-9} s

Minority and majority currents



$$I_p(x_n) = \frac{qAD_p}{L_p}\Delta p_n e^{-x_n/L_p}$$

$$I_n(x_n) = I - I_p(x_n)$$



Numerical Example

- Continue with ZnSe Example, Calculate Igen.

$$\mu_{nZnSe} = 100 cm^2 / Vs$$

$$\mu_{pZnSe} = 16 cm^2 / Vs$$

$$\tau_n = \tau_p = 1 \times 10^{-9} s$$

Reverse bias breakdown

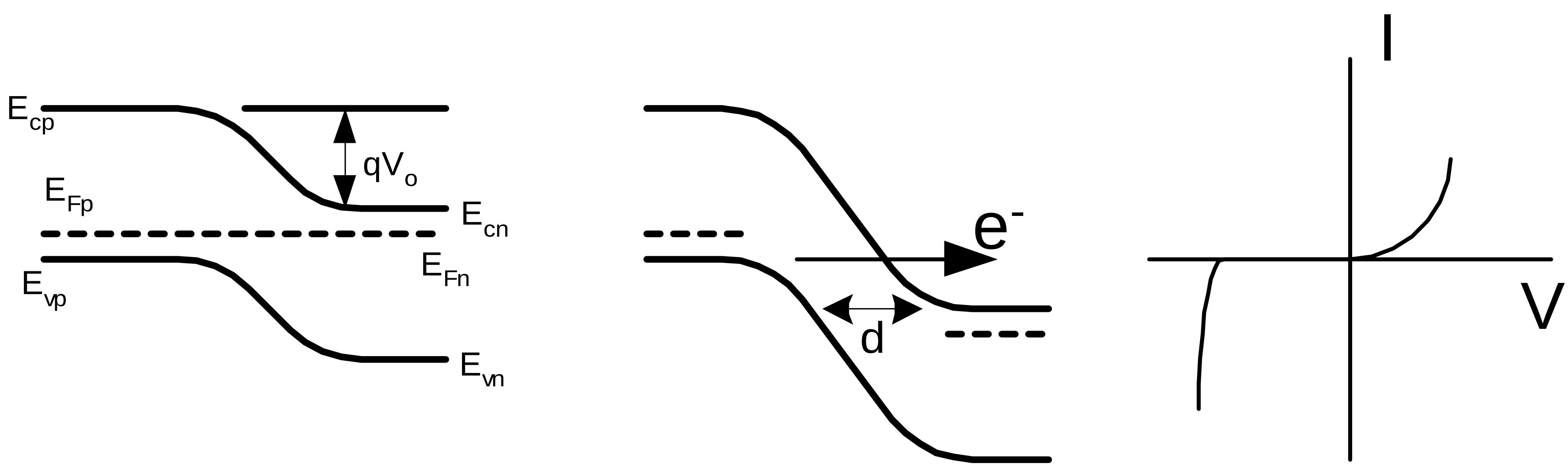
- Under reverse bias a pn junction exhibits a small voltage independent current until a critical voltage is reached V_{br}. If the bias voltage exceeds V_{br} the current increases dramatically.
- If biased properly with a current limiting diode, you can operate in reverse breakdown mode with out damaging the diode.

Reverse Breakdown

- Zener Breakdown
  - This effect applies to heavily doped junctions (p+, n+). This is a low voltage effect.
  - Barrier is thin due to high abrupt doping
  - When the reverse bias voltage is large enough, electrons can tunnel to the p-side, and holes can tunnel to the n-side (section 2.4.4)
  - Reverse bias of a p+/n+ junction
    - leads to large electric field (10^6V/cm)
    - leads to covalent electrons being "ripped away"

Reverse Breakdown

- Zener Breakdown

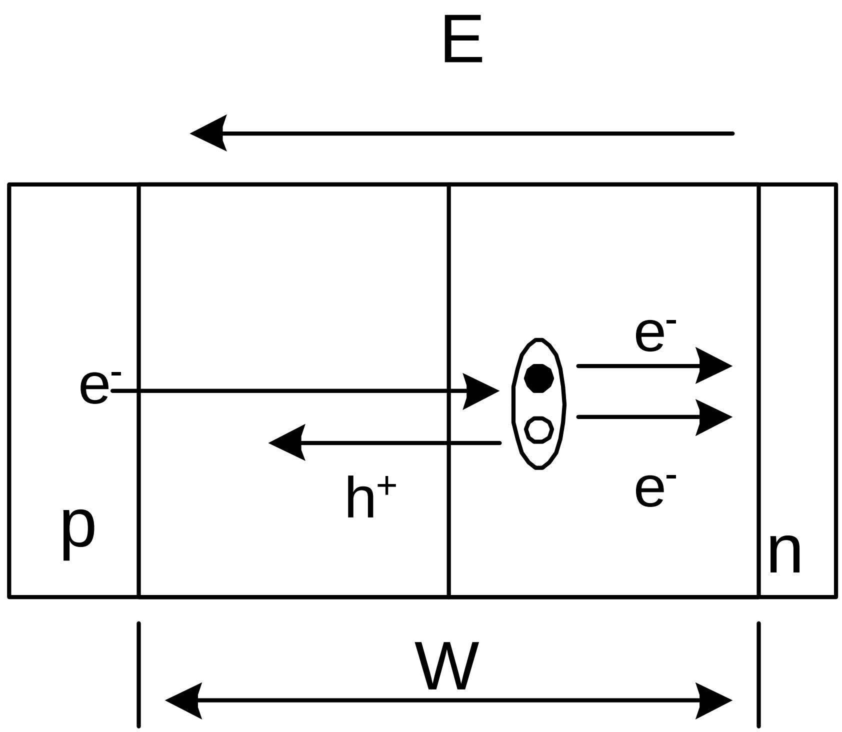


Reverse Breakdown

- Avalanche Breakdown
  - Lightly doped junctions, tunneling can not occur
    - W increases with reverse bias.
  - Impact ionization
    - A carrier can be accelerated by a high electric field with enough kinetic energy to knock an electron out of the lattices covalent bond and make an EHP. One carrier can cause many carriers to be created.
    - To design V_{br}, use figure 5-22 on page 190.

Reverse Breakdown

- Avalanche Breakdown



PE

An abrupt p-n junction has the following properties at 300K:

p side	n side
$Na=2x10^{20}cm^{-4}$	$Nd=1x10^{15}cm^{-3}$
$\tau_n=.1x10^{-6}s$	$\tau_p=10x10^{-6}s$
$\mu_p=200\ cm^{2/}Vs$	$\mu_n=1300cm^2/Vs$
$\mu_n=700$	$\mu_p=450$
$A=10^{-4}cm^2$	$A=10^{-4}cm^2$

Find the breakdown voltage if the diode is made of Ge.

Find the breakdown voltage if the diode is made of Si, and

Nd is changed to $1x10^{19}cm^{-3}$.

Transient and AC conditions

- Time variation of stored charge.
  - Time dependant continuity equation
  - p+/n diode

$$\mathrm{x_n}(0) \rightarrow \text{all hole current}$$

$$\mathrm{x_n}(\infty) \rightarrow \text{no hole current}$$

$$\mathrm{i(t)} = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt}$$

$$Q_p(t) = I\tau_p e^{-t/\tau_p}$$

Transient and AC conditions

- Time variation of stored charge.
  - Quasi-steady state approximation

$$v(t) = \frac{kT}{q} \ln\left(\frac{I\tau_p}{qAL_p p_n} e^{-t/\tau_p} + 1 \right)$$

- To decrease switching time
  - decrease n-type region to less than L_p or decrease τ_p (Au or Pt doping)

Transient and AC conditions

- Reverse recovery transient
  - This is a switching characteristic or large signal analysis (large deviations from a reference point).
  - Assume a p+/n diode biased with resistor R, driven by a square wave (+E to -E with period T)
    - Forward bias: For large E most of the voltage drops across the resistor and the current is given by I_f=E/R.

Transient and AC conditions

- Reverse recovery transient
  - Sudden application of reverse bias:
    - Current initially becomes $i=I_r=-E/R$ because the stored charge in the junction can not be removed instantly, therefor the voltage can not be changed instantly.
    - Once all the minority charge is gone the junction will become reversed biased and thus act like a large resistance because only the I_{gen} current is flowing.

Transient and AC conditions

- Reverse recovery transient
  - Sudden application of reverse bias:
    - The time it takes for the junction voltage to become zero is t_{sd}.

$$t_{sd} = \tau_p \left[erf^{-1}\left(\frac{I_f}{I_f + I_r} \right) \right]^2$$

with the quasi-steady state approximation:

$$\mathrm{t_{sd}} = \tau_p \ln\left(1 + \frac{I_f}{I_r} \right)$$

Transient and AC conditions

- Capacitance of p-n junctions
  – This is for small signal analysis. Assume a bias point and that the applied time varying voltage or current does not perturb the diode's G and C very far from their bias values.

Transient and AC conditions

- Junction capacitance:
  - Dominant under reverse bias, due to separation of positive and negative charges.

$$W = \left[\frac{2\varepsilon (V_o - V)}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{\frac{1}{2}}$$

$$|Q| = qA \frac{N_a N_d}{N_a + N_d} W$$

$$C_j = \left| \frac{dQ}{d(V_o - V)} \right| = \frac{A}{2} \left[\frac{2q\varepsilon}{(V_o - V)} \frac{N_a N_d}{N_a + N_d} \right]^{\frac{1}{2}}$$

Spice Parameters for a Diode

$$M := \frac{1}{2} \quad TT := 10^{-9}\,s \quad V_J := .7V$$

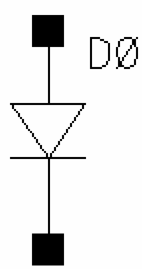
M is the grading coefficient
TT is the transits time
VJ is the built in voltage
Cd is the depletion capacitance
Cs is the charge storage capacitance

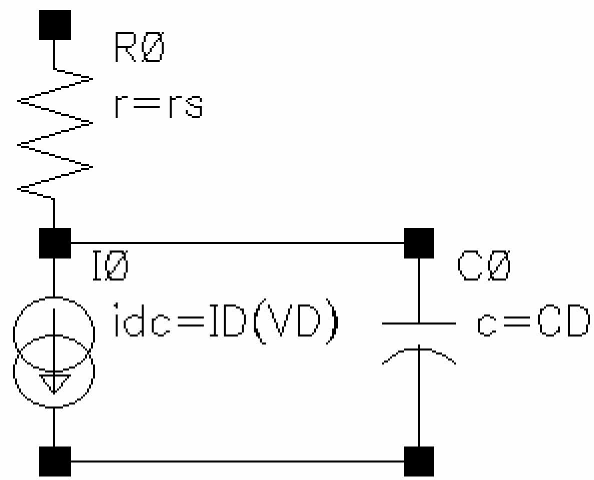
$$C_{J0} := 10^{-15}\,F$$

$$C_d := C_{J0} \cdot \left(1 - \frac{V_D}{V_J}\right)^{-M}$$

$$C_s := TT \cdot \left(\frac{d}{dV_D} I_D\right)$$

$$C_D := C_d + C_s$$





Transient and AC conditions

- Storage capacitance:
  - Dominant under forward bias, due to the voltage lagging behind the current.

$$G_s = \frac{dI}{dV} = \frac{q}{kT} I$$

$$C_s = \frac{dQ_p}{dV} = \frac{q}{kT} I \tau_p$$

$$i(ac) = G_s v(ac) + C_s \frac{dv(ac)}{dt}$$

Example Cj, Cs

- For the ZnSe example calculate Cj at –2, 0, and 2 volts.
- For the ZnSe example calculate Cs at –2, 0, and 2 volts.
- Minority lifetimes are 1ns.

There are 4 DC spice parameters for a diode

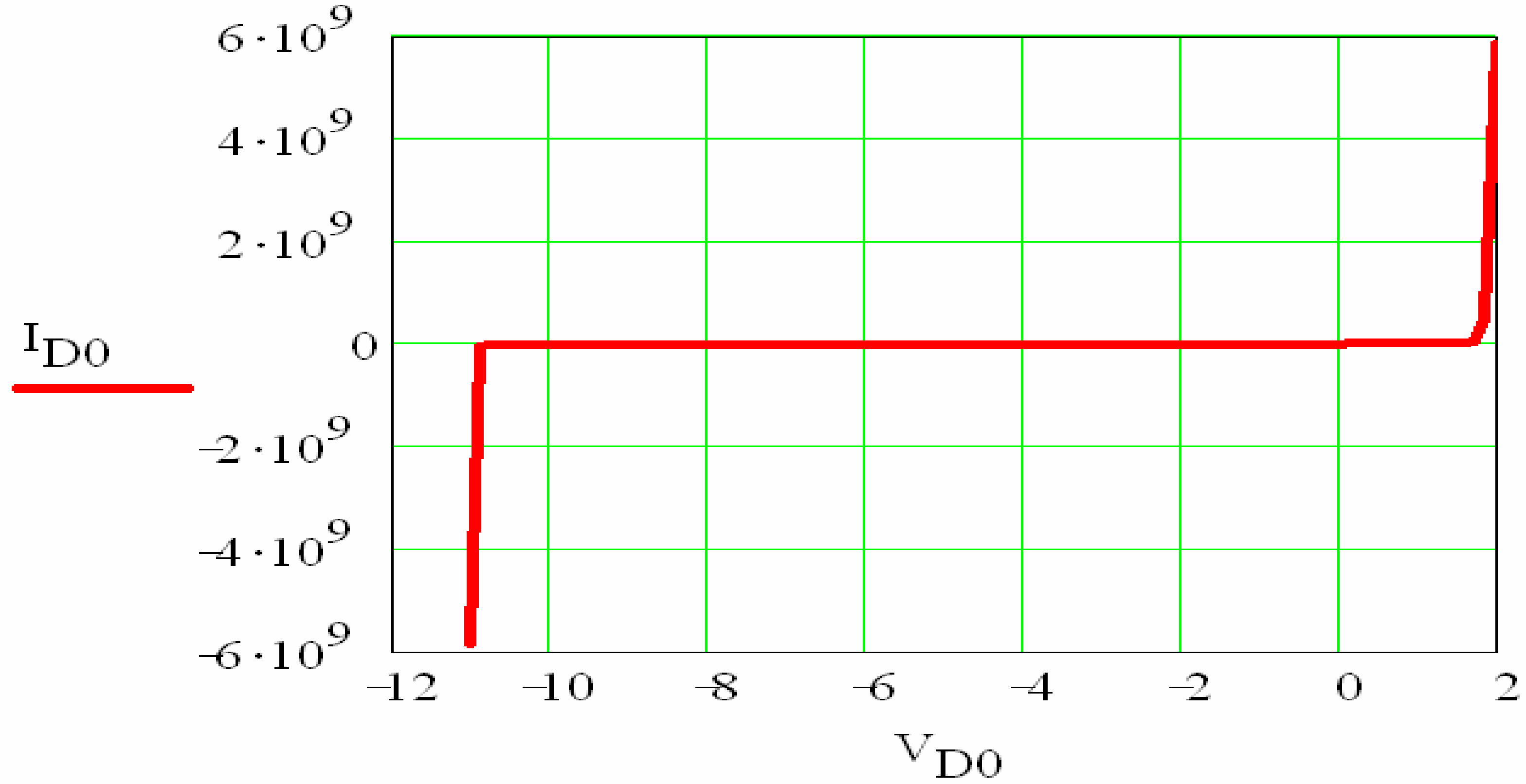
IS Saturation current (Given in Amps)
N Emission Coefficient (No Units)
RS Parasitic resistance (Given in Ω)
BV Breakdown Voltage (Given in Volts)
IBV Breakdown Current (Given in Amps)

GMIN is a small resistance
To prevent a value of zero current form Flowing. Usually set to 10^{-12}S

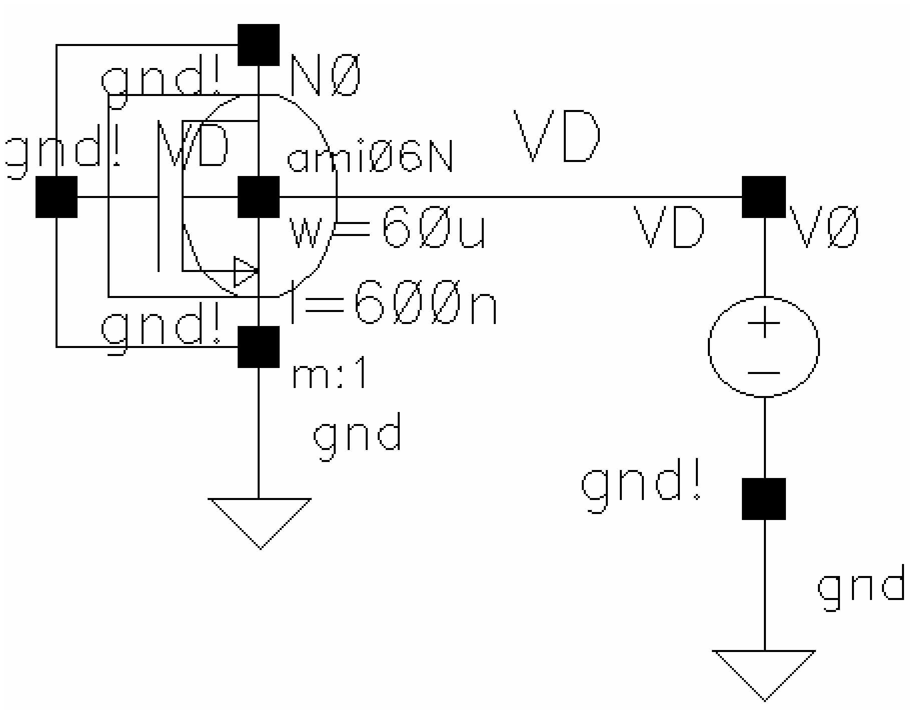
$$I_s := 1 \times 10^{-7}$$
$$n := 2$$
$$r_s := 100$$
$$V_t := .0259$$
$$BV := 10$$
$$G_{min} := 1 \times 10^{-9}$$
$$IBV := I_s \cdot \frac{BV}{V_t}$$

$$I_{D0_i} := \begin{cases} \left[I_s \cdot \left(e^{\frac{V_{D0_i}}{n \cdot V_t}} - 1 \right) + V_{D0_i} \cdot G_{min} \right] & \text{if } V_{D0_i} > -BV \\ (-IBV) & \text{if } V_{D0_i} = -BV \\ \left[-I_s \cdot \left[e^{\frac{-\left(BV + V_{D0_i}\right)}{V_t}} - 1 + \frac{BV}{V_t} \right] \right] & \text{if } V_{D0_i} < -BV \end{cases}$$

Full Diode Response

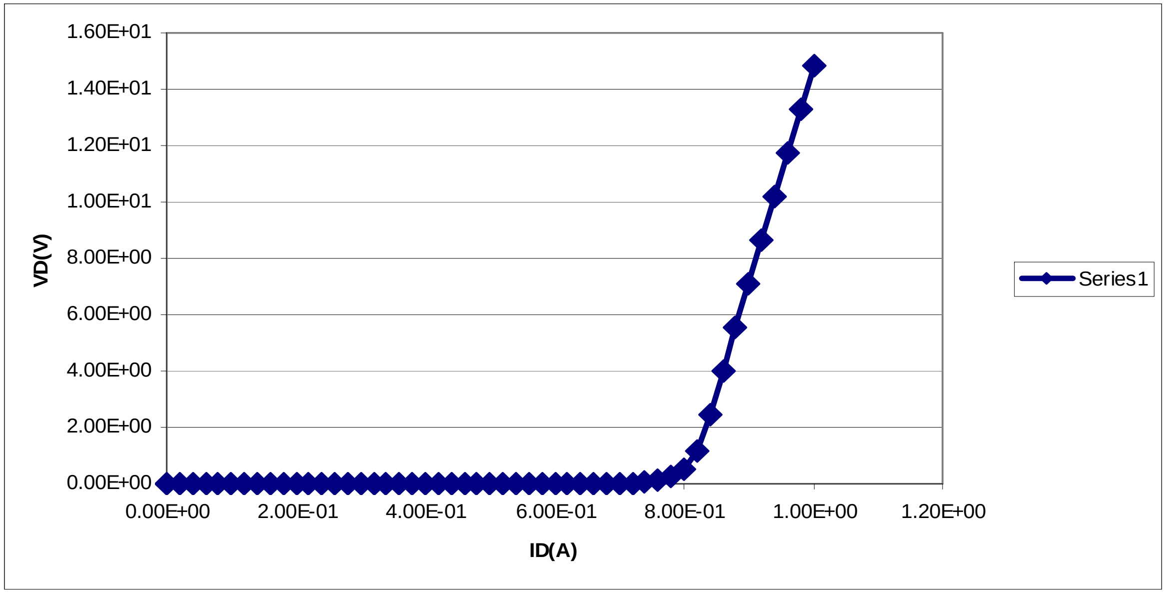


Test the diode of a NMOS

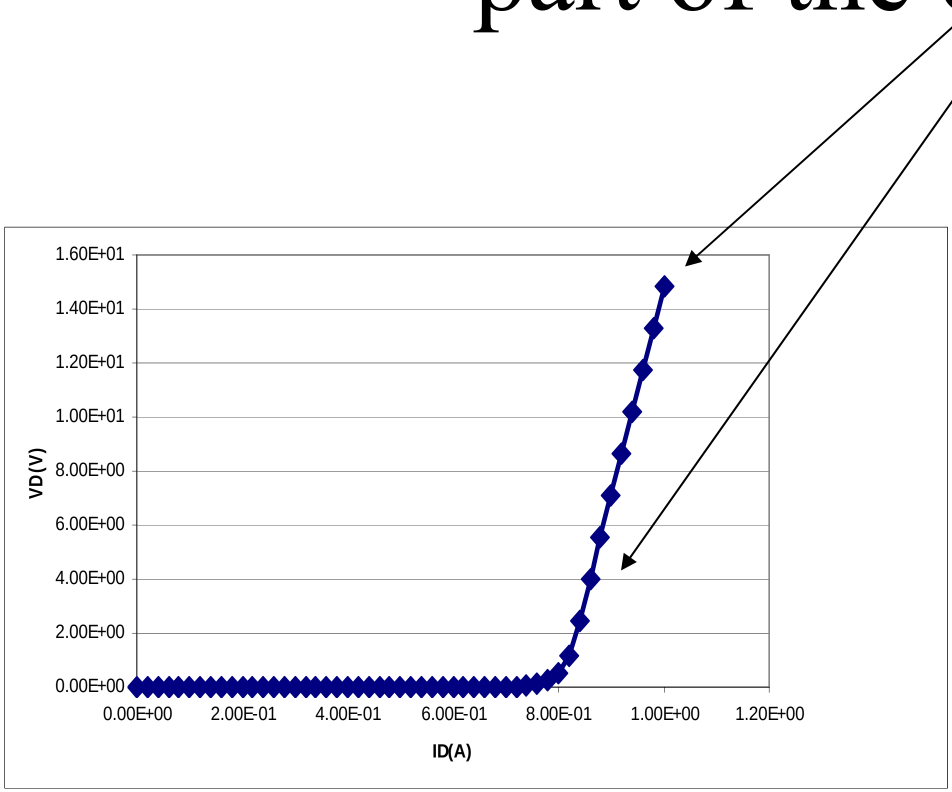


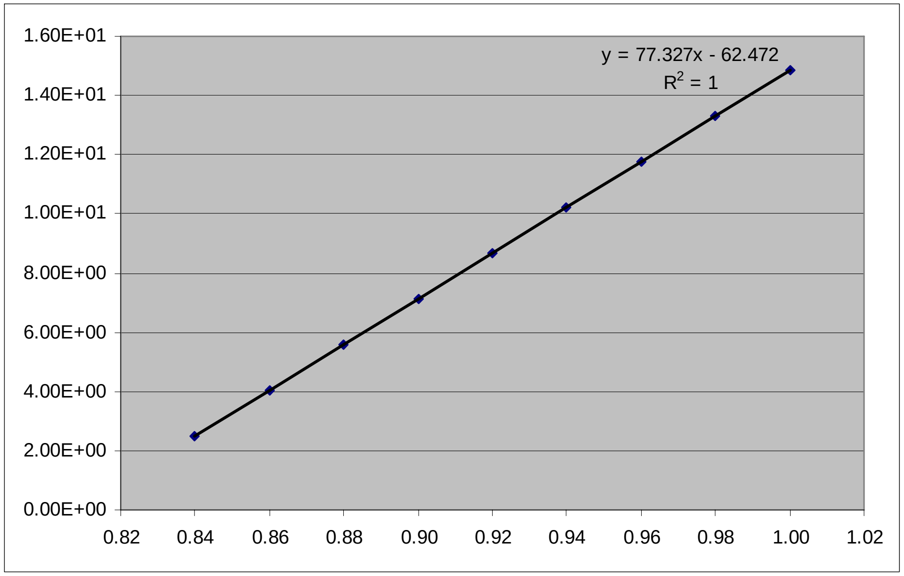
Note there are two diodes being tested.

Forward Bias Diode
Linear

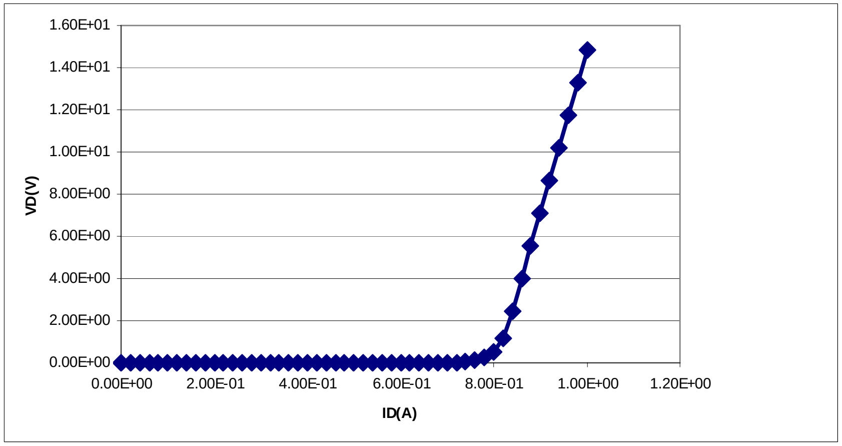


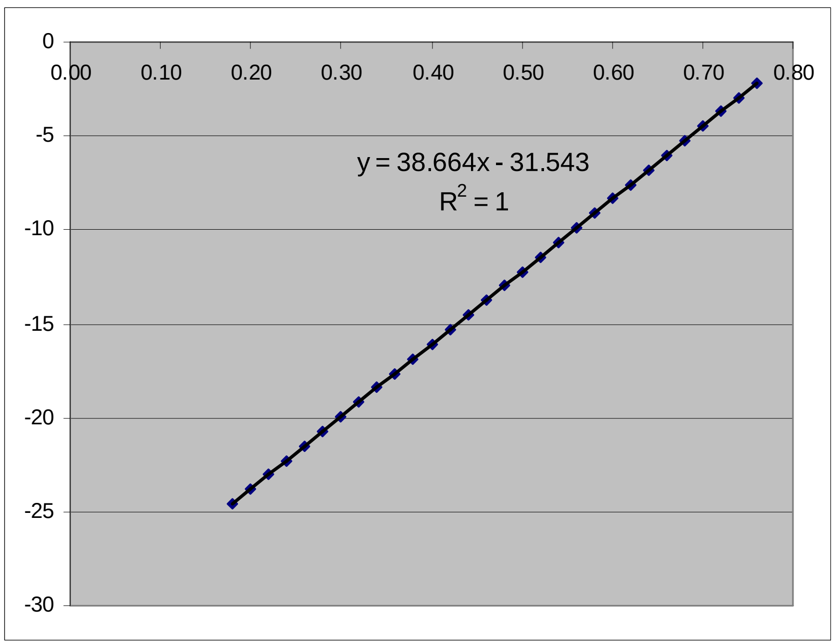
Take the RS value from the Linear part of the diode curve





Forward Bias Log Scale (RS position omitted)



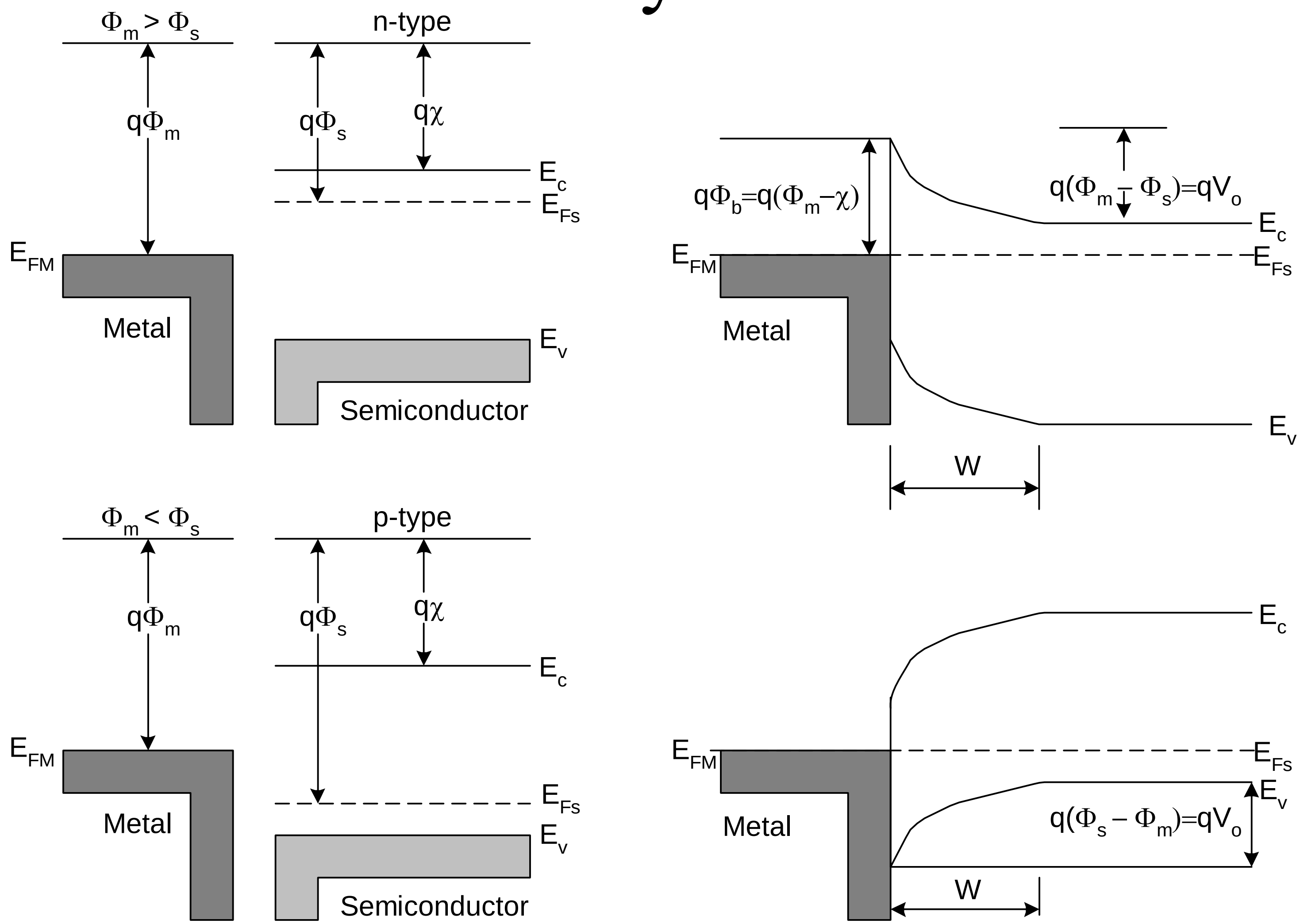


$$I_S := e^{-31.543} \qquad I_S = 2 \times 10^{-14}$$

$$n := \frac{1}{38.664 \cdot .0259} \qquad n = 0.999$$

Do not use linear
Region of Diode
Or too close to 0V.
The RS value and GMIN
Will skew the results.

Schottky barriers



Rectifying contacts

- Apply a forward bias to the Metal of the M/S(n) diode and the contact potential is reduced by V_o-V
  – Allows electrons to diffuse into metal.
- Apply a forward bias to the Semiconductor of the M/S(p) diode and the contact potential is reduced by V_o-V
  – Allows holes to diffuse into metal.

Rectifying contacts

- Apply a reverse bias to the Metal of the M/S(n) diode and the contact potential is increased by V_o+V_r.
  - Electrons have to overcome a voltage independent barrier to diffuse into metal.
- Apply a reverse bias to the Semiconductor of the M/S(p) diode and the contact potential is reduced by V_o+V_r.
  - Holes have to overcome a voltage independent barrier to diffuse into metal.

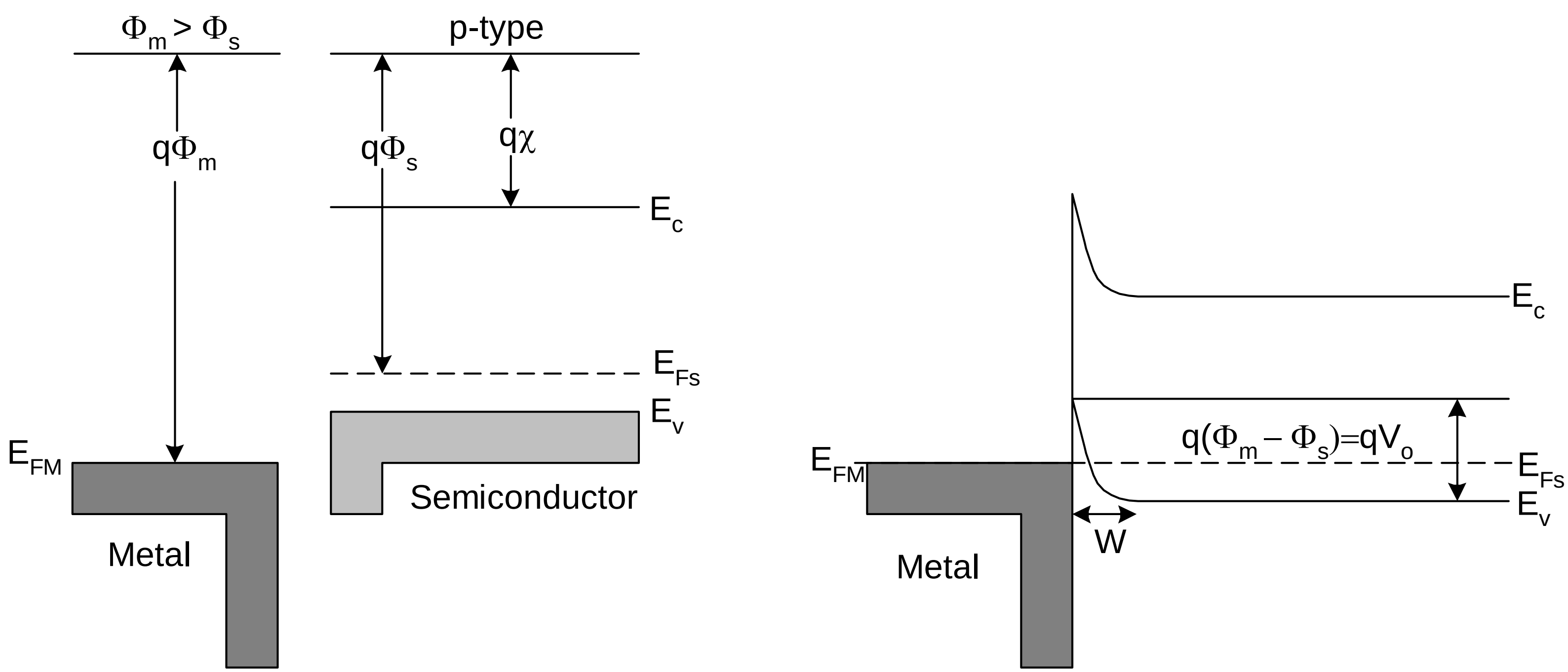
Rectifying contacts

- Current flows primarily by **majority** carriers is both cases.
- Very little charge storage occurs, which leads to **fast switching speeds**.

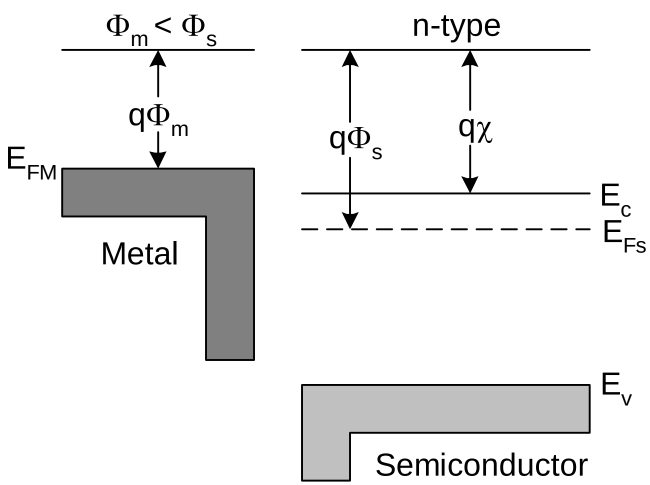
Ohmic contacts

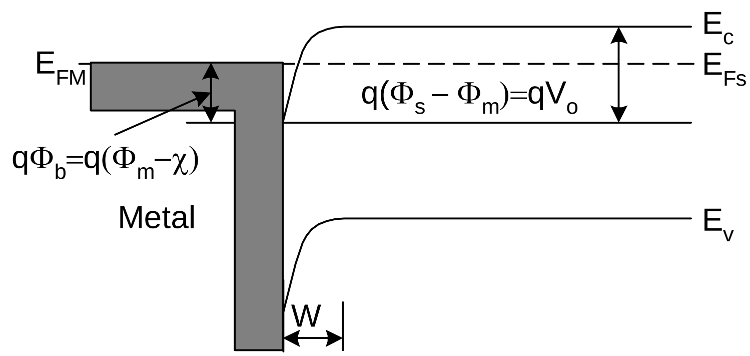
- Metal/semiconductor ohmic contacts
  - linear near the origin, non-rectifying
- Two methods of fabrication
  - Choose a metal with a workfunction that aligns the fermi levels with majority carriers. (Al for p-type Si, Au for n-type Si
  - Dope the semiconductor heavily so that W is very thin so that tunneling occurs (Al on p^+ or n^+ Si)
  - Heavy doping all ways improves ohmic behavior.

Ohmic contacts



Ohmic contacts





Real Schottky barriers

- In Si, there is a thin oxide in between the metal and semiconductor.
- Surface states arise from the crystal ending
  - This can pin the fermi level to midgap in GaAs
- If a metal semiconductor junction is alloyed the interface is blurred between metal/metal-semiconductor/semiconductor.
- Contact design is very dependant on your process.