

Question 1 (15PTS):

Please draw and label the top view and cross section of an IC N+/P Resistor that has a total resistance of 100Ω s. The junction depth is $1\mu\text{m}$, and the sheet resistance is 10Ω s per square. You may assume the contact resistance is 5Ω s. The minimum dimension for all mask features is $1\mu\text{m}$.

Question 2(15pts):

Discuss several applications of resistors on an IC.

Question 3 (20pts):

You are a process engineer designing some diode based devices. You are using Si and you may dope two layers n-type or p-type from 10^{14}cm^{-3} to 10^{19}cm^{-3} .

Please design a diode that has the maximum capacitance per unit area.

You are a process engineer designing some diode based devices. You are using Si and you may dope two layers n-type or p-type from 10^{14}cm^{-3} to 10^{19}cm^{-3} .

Please design a diode that has the minimum capacitance per unit area.

Question 4 (15pts):

**Please explain why process engineers put strain on a Silicon crystal.
(Hint: Strain slightly alters the lattice constant of the crystal.)**

Question 5(25pts):

Draw the Energy Band Diagram of a Silicon N+/P junction at thermal equilibrium if $N_A=10^{14}\text{cm}^{-3}$ and $N_D=10^{19}\text{cm}^{-3}$ at 300K.

Question 6(10pts):

You are a process engineer who has designed a diode with an abrupt junction. When you go to extract the capacitance values (CJO, M, and PHI) you notice that the best fit gives an M of .3. Please explain what might have happened to cause this.