#1 Find the small signal RF model of a MOSFET.

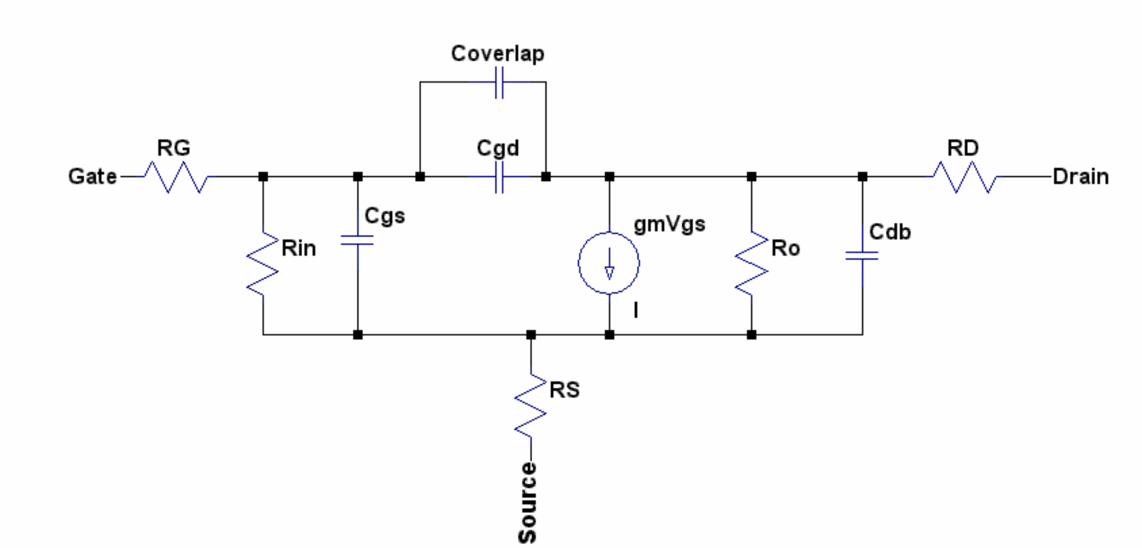

Figure 1: Small Signal RF model for a MOSFET.

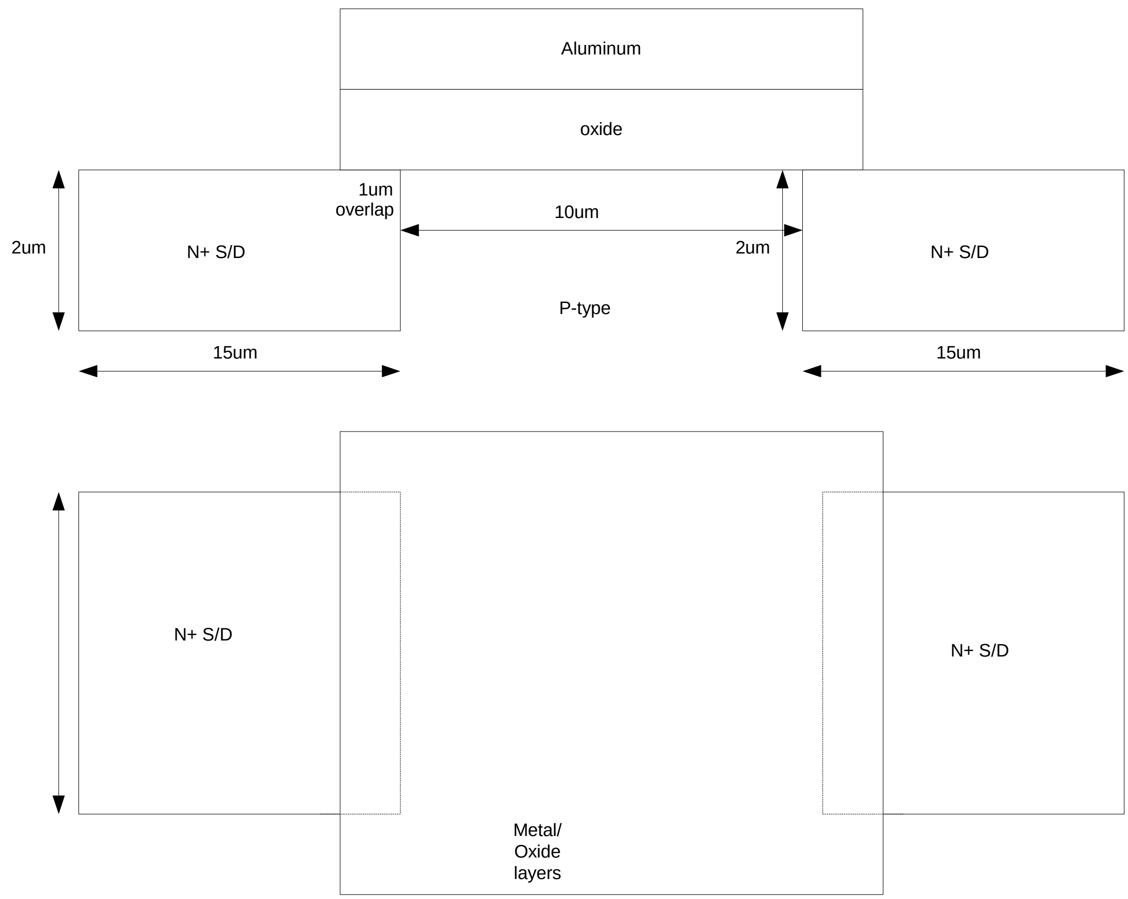

Figure 2: Top view and cross section of MOSFET.

The first thing to do is pick a bias point as the drain capacitance will depend on the drain voltage, and the output resistance depends upon the drain current. We have everything we need to calculate VT, and we can look up the mobility (assuming the mobility is cut in half due to the electrons being confined in a channel, and that it will not change with the applied voltages).

$$q := 1.6\cdot 10^{-19}C \qquad \varepsilon_{Si} := 11.8\cdot 8.85\cdot 10^{-14}\frac{F}{cm} \qquad k := 1.38\cdot 10^{-23}\frac{J}{K}$$

$$T := 300K \qquad N_A := 1\cdot 10^{17}cm^{-3} \qquad \varepsilon_{oxide} := 3.9\cdot 8.85\cdot 10^{-14}\frac{F}{cm}$$

$$n_i := 9.65\cdot 10^{9}cm^{-3} \qquad Q_i := 5\cdot 10^{10}\cdot\frac{q}{cm^2} \qquad Q_i = 8\times 10^{-9}\,C\,cm^{-2}$$

$$\phi_F := \frac{k\cdot T}{q}\cdot\ln\left(\frac{N_A}{n_i}\right) \qquad \phi_{ms} := -.6V - \frac{k\cdot T}{q}\cdot\ln\left(\frac{N_A}{n_i}\right) \qquad \phi_{ms} = -1.018\,V$$

$$Q_D := -2\cdot\left(\varepsilon_{Si}\cdot q\cdot N_A\cdot\phi_F\right)^{\frac{1}{2}} \qquad Q_D = -1.671\times 10^{-7}\frac{C}{cm^2}$$

$$d := 0.015\cdot 10^{-4}cm \qquad C_{oxide} := \frac{\varepsilon_{oxide}}{d}$$

$$V_{T0} := \phi_{ms} - \frac{Q_i}{C_{oxide}} - \frac{Q_D}{C_{oxide}} + 2\cdot\phi_F$$

$$V_{T0} = 0.51\,V \qquad U_T := .0259V$$

In the figure below you see the MOSFET in the linear and saturation mode with both channel length modulation and without. I used L=10um rather than L minus the depletion widths, because I am not interested in the current yet. I also need to pick a drain voltage to get the proper depletion width. If we assume a VDD of 5 volts and an overdrive voltage of .3 Volts((VGS-VT)=.3V) we see that a VD of 2.5 volts puts us around the middle of the saturation region, thus allowing maximum swing of the output.

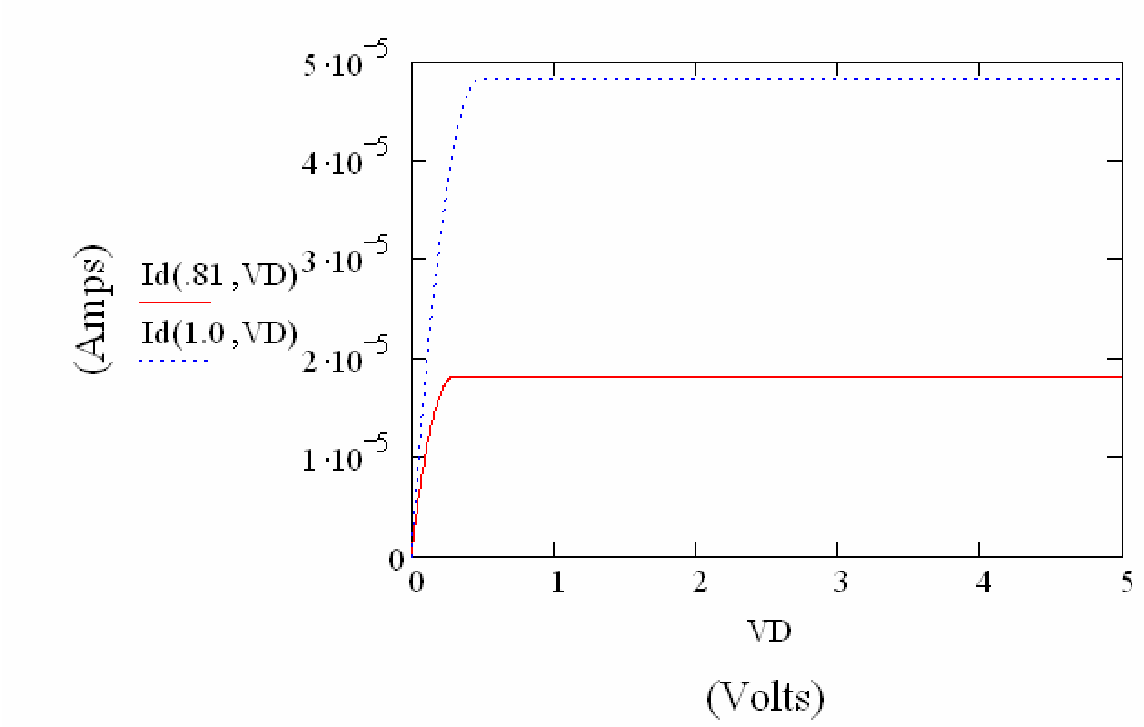

Figure 3: ID, VD, with VG as a parameter, no channel width modulation.

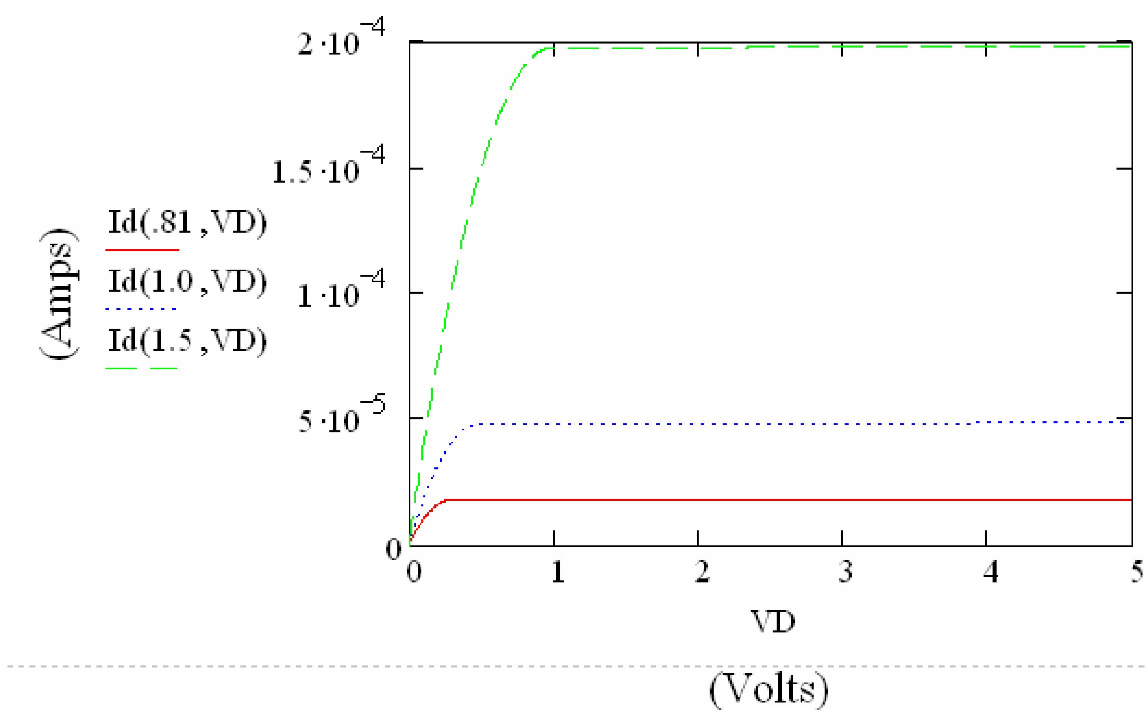

Figure 4:ID, VD, with VG as a parameter, with channel width modulation.

Now we have a VDS of 2.5 Volts we can calculate the depletion width and thus the channel length and the drain capacitance.

$$Na := 10^{17} cm^{-3}$$

$$Nd := 10^{19} cm^{-3} \qquad DD := 10 \cdot 10^{-4} cm \qquad Z := 50 \cdot 10^{-4} cm$$

$$Rj := 2.0 \cdot 10^{-4} cm$$

$$Vo := \frac{k \cdot T}{q} \cdot \ln\left(\frac{Na \cdot Nd}{n_i^2}\right) \qquad Vo = 0.955\,V$$

$$Area\_sidewall\_1 := 2 \cdot DD \cdot Rj \qquad Area\_sidewall\_1 = 4 \times 10^{-7} cm^2$$

$$Area\_sidewall\_2 := 2 \cdot Z \cdot Rj \qquad Area\_sidewall\_2 = 2 \times 10^{-6} cm^2$$

$$Area\_bottom := Z \cdot DD \qquad Area\_bottom = 5 \times 10^{-6} cm^2$$

$$Area\_Total := Area\_sidewall\_1 + Area\_sidewall\_2 + Area\_bottom$$

$$Area\_Total = 7.4 \times 10^{-6} cm^2 \qquad Vd := -2.5V$$

A positive VD is a negative voltage on the diode.

$$W\_Depletion := \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q} \cdot \frac{Na + Nd}{Na \cdot Nd} \cdot (Vo - Vd)} \qquad W\_Depletion = 2.134 \times 10^{-5} cm$$

$$C_{DB} := \frac{Area\_Total \cdot \varepsilon_{Si}}{W\_Depletion} \qquad C_{DB} = 3.621 \times 10^{-13} F$$

The overlap capacitance is the oxide capacitance due to the fact the mos over the drain is all ways in accumulation. This assumes that the depletion width is not a significant portion of the channel length.

$$overlap := 1 \cdot 10^{-4} cm$$

$$C_{overlap} := C_{oxide} \cdot Z \cdot overlap \qquad C_{overlap} = 1.151 \times 10^{-13} F$$

Rin is considered to be infinite, and thus is not considered because the oxide thickness is 5 times the thickness at which tunnel occurs (150Å vs. 30Å).

The capacitance from the gate to drain in the triode region is 1/2Cox*Z*L, and is zero in the saturation region. Cgb=0.

Cgs in saturation is 2/3's th Oxide capacitance value.

$$L := 10 \cdot 10^{-4} cm$$

$$C_{gs} := \frac{2}{3} \cdot C_{oxide} \cdot Z \cdot L \quad C_{gs} = 7.67 \times 10^{-13} F$$

This assumes that the depletion width is not a significant portion of the channel length. Is this a good assumption?

$$Vd := -2.5V$$

$$W\_Depletion\_Drain := \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q} \cdot \frac{Na + Nd}{Na \cdot Nd} \cdot (Vo - Vd)}$$

$$W\_Depletion\_Drain = 2.134 \times 10^{-5} cm$$

$$Vd := 0V$$

$$W\_Depletion\_Source := \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q} \cdot \frac{Na + Nd}{Na \cdot Nd} \cdot (Vo - Vd)}$$

$$W\_Depletion\_Source = 1.122 \times 10^{-5} cm$$

$$Leff := L - W\ Depletion\_Source - W\_Depletion\_Drain$$

$$Leff = 9.674 \times 10^{-4} cm$$

$$\frac{Leff}{L} = 0.967$$

It looks like it is a good assumption.

Gm is given by:

$$V_G := V_{T0} + .3V$$

$$\mu_n := 350 \frac{cm^2}{V \cdot s}$$

$$g_m := \frac{Z \cdot \mu_n \cdot C_{oxide}}{L} \cdot (V_G - V_{T0}) \qquad g_m = 1.208 \times 10^{-4} \frac{1}{\Omega}$$

To find Ro we can assume that channel length modulation does not affect the hand calculations much by looking at figures 3 and 4. This is not all ways the case. We just need a simple long channel equation for the saturation current.

$$I_D := \frac{Z}{2 \cdot L} \cdot \mu_n \cdot C_{oxide} \cdot (V_G - V_{T0})^2 \qquad I_D = 1.812 \times 10^{-5} A$$

$$R_o := \frac{1}{\lambda \cdot I_D} \qquad R_o = 5.519 \times 10^{7} \Omega$$

The final thing to calculate is the resistance of the gate, drain and source. The lead resistance is the same for all three terminals.

The resitance to the drain and source has to include the contact resistance ansd the resitnace of the source and drain.

We can make a worst case that the Width will be Z, the Lenth will be DD, and the hieght is Rj.

$$R_{Contact} := 10\Omega \qquad Resistivity := 8 \cdot 10^{-3} \Omega \cdot cm$$

From fig 7 page 55 of text.

$$R_j := 2 \cdot 10^{-4} cm \qquad R_{Diff} := \frac{DD}{Z \cdot R_j} \cdot Resistivity \qquad R_{Diff} = 8\Omega$$

$$R_{Drain} := R_{Lead} + R_{Contact} + R_{Diff} \qquad R_{Drain} = 18.15\Omega$$

$$R_{Source} := R_{Drain}$$

#2 There are two limits on the maximum drain voltage. (The minimum drain voltage is VG-VT, so that the device will be in saturation). The break down voltage of the drain pn junction and when the depletion widths touch (punch through or DIBLE) is another method by which we lose control of the gate. We need to find when Leff equals zero, or we can look up the breakdown voltage from figure 22 page 129. With the substrate doping we get a breakdown voltage of 10Volts, see if we still have a channel at that voltage.

$$Vd := -10V$$

$$W\_Depletion := \sqrt{\frac{2\cdot\varepsilon_{Si}}{q}\cdot\frac{Na + Nd}{Na\cdot Nd}\cdot(Vo - Vd)} \qquad W\_Depletion = 3.8\times 10^{-5}\,cm$$

$$W\_Source := \sqrt{\frac{2\cdot\varepsilon_{Si}}{q}\cdot\frac{Na + Nd}{Na\cdot Nd}\cdot(Vo - 0)}$$

$$W\_Drain := \sqrt{\frac{2\cdot\varepsilon_{Si}}{q}\cdot\frac{Na + Nd}{Na\cdot Nd}\cdot(Vo - Vd)}$$

$$Leff := L - W\_Source - W\_Drain$$

$Leff = 9.508\times 10^{-4}\,cm$ We still have a channel, so the limit is the breakdown voltage.

#3

$$V_{FB} := \phi_{ms} - \frac{Q_i}{C_{oxide}} \qquad V_{FB} = -1.053\,V$$

$$\Psi_B := \phi_F \quad C_o := C_{oxide} \qquad V_{BS} := 1V$$

$$V_T := V_{FB} + 2\cdot\Psi_B + \frac{\sqrt{2\cdot\varepsilon_{Si}\cdot q\cdot N_A\cdot\left(2\cdot\Psi_B + V_{BS}\right)}}{C_o}$$

$$V_T = 0.86\,V$$

#4

$$\Delta V_T := \frac{-q \cdot N_A \cdot W_m \cdot R_j}{C_o \cdot L} \cdot \left(\sqrt{1 + \frac{2 \cdot W_m}{R_j}} - 1 \right)$$

$$\Delta V_T = -7.399 \times 10^{-3}\,V$$

$$V_T := V_{T0} - \Delta V_T \qquad V_T = 0.517\,V$$

We do not see a significant different in VT.

#5

DIBLE causes a large current to be present when there is a large vds. In the case of the CMOS inverter when vin is zero volts, the pmos is on and the nmos is supposed to be off, but it leaks. When vin is high the noms is on and the pmos is supposed to by off but it leaks. The result is that the inverter can not drive the voltage to vdd or ground.

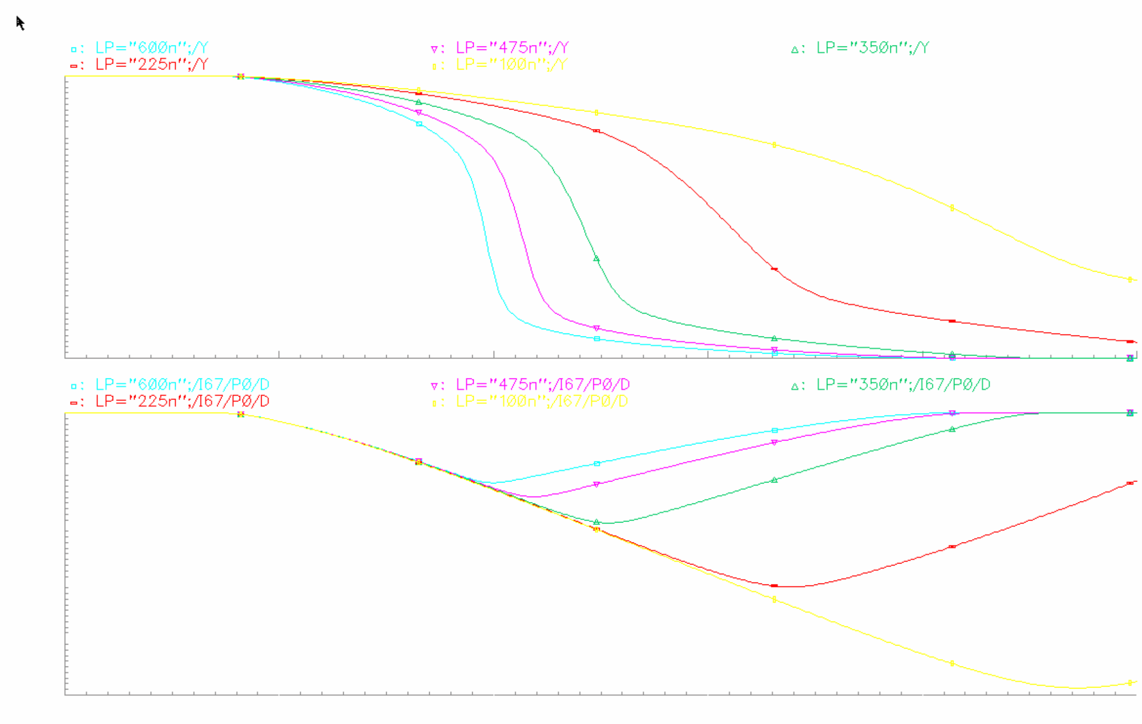

Figure 5: Vout vs. Vin , CMOS inverter with LP showing DIBLE.

The upper plot is vout vs vin, and the lower is the drain current. We see that for a small channel length of the pmos (yellow) the current never goes to zero, and vout never goes to zero.