

1. Develop an RF small signal model for an n-type Si/SiO₂ MOSFET, biased in the common source mode, with the following properties: Note I am using figure 14 on page 186. $Z=W$, and $R_j=X_j$, and $d=TOX$ from my notes.

NA	10^{17}cm^{-3}
λ	0.001V^{-1}
Q _i	$5 \times 10^{10} \text{q/cm}^{-2}$
L	$10 \times 10^{-4} \text{cm}$
Z	$50 \times 10^{-4} \text{cm}$
d	$0.015 \times 10^{-4} \text{cm}$
R _j	$2.0 \times 10^{-4} \text{cm}$
DD (Not labeled in figure)	$15.0 \times 10^{-4} \text{cm}$
Gate material	Aluminum
Height or thickness of Aluminum	$0.2 \times 10^{-4} \text{cm}$
Length of Al wires to source/drain/gate	$500 \times 10^{-4} \text{cm}$
Width of Al wires to source/drain/gate	$50 \times 10^{-4} \text{cm}$
Contact Resistance to Source or drain	10Ω

The source/drain junctions are abrupt. The first thing you probably want to do is draw a cross section of the device to make sure the dimensions make sense. Some items need a bias point. You need to find a bias point and that means you need a simple transistor model with V_T , μ_n and C_{ox} . For μ_n you can look up the mobility in the book and divide it in half. If a dimension or doping is not mentioned you need to assume one.

2. For the MOSFET described above, what will be the limit on V_D ? Explain why.
3. For the MOSFET described above, what would the V_T be if the BS voltage was 1 Volt?
4. For the MOSFET described above, what would the V_T threshold voltage roll off in the linear region?
5. Using the CMOS inverter described in Figure 28 of the text, what would happen to the V_{out} vs. V_{in} curve shown in Figure 30 if the DIBL effect was severe?