

1. Design an MIS Capacitor on a p-type  $\langle 100 \rangle$  silicon substrate to have a  $V_T$  of 0.7 V if the fixed oxide charge is  $5 \times 10^{10} \text{ q/cm}^2$ ,  $N_A = 1 \times 10^{16} \text{ cm}^{-3}$ , and the permittivity of the oxide layer is  $3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$ . The gate material is heavily doped n-poly-silicon. (Room temperature conditions apply.)
2. Calculate the maximum depletion width of the MOS diode in question 1.
3. Design an MIS Capacitor on a n-type  $\langle 100 \rangle$  silicon substrate to have a  $V_T$  of -1.0V if the fixed oxide charge is  $5 \times 10^{10} \text{ q/cm}^2$ ,  $t_{ox} = d = 600 \text{ \AA}$ , and the permittivity of the oxide layer is  $3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$ . The gate material is heavily doped n-poly-silicon. (Room temperature conditions apply.)
4. Design an MIS Capacitor on a p-type  $\langle 100 \rangle$  silicon substrate to have a  $V_T$  of .6V if the fixed oxide charge is  $3 \times 10^{10} \text{ q/cm}^2$ , and the permittivity of the oxide layer is  $3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$ . The gate material is heavily doped n-poly-silicon.
5. Draw the EGB of an MIS Capacitor on a p-type  $\langle 100 \rangle$  silicon substrate where  $V_G = V_T$ . (Room temperature conditions apply.)
6. As you remember, the number of grid points affects the time a TCAD simulation has to run, and the accuracy of the simulation. In the case of the MIS diode from question #1, up to what point would you need a fine grid to accurately simulate the MIS diode?
7. The figure below shows the measured CV data of a MIS capacitor on p-type  $\langle 100 \rangle$  silicon substrate with an aluminum gate ( $\phi_{ms} = -.6 \text{ eV} - UT \times \ln(N_A/n_i)$ ) (The Insulator is  $\text{SiO}_2$ .) Extract  $d$ , ( $t_{ox}$ )  $N_A$ ,  $V_T$ , and fixed oxide charge. (Room temperature conditions apply.) Hint, you do not have to scale the measured data by the area.

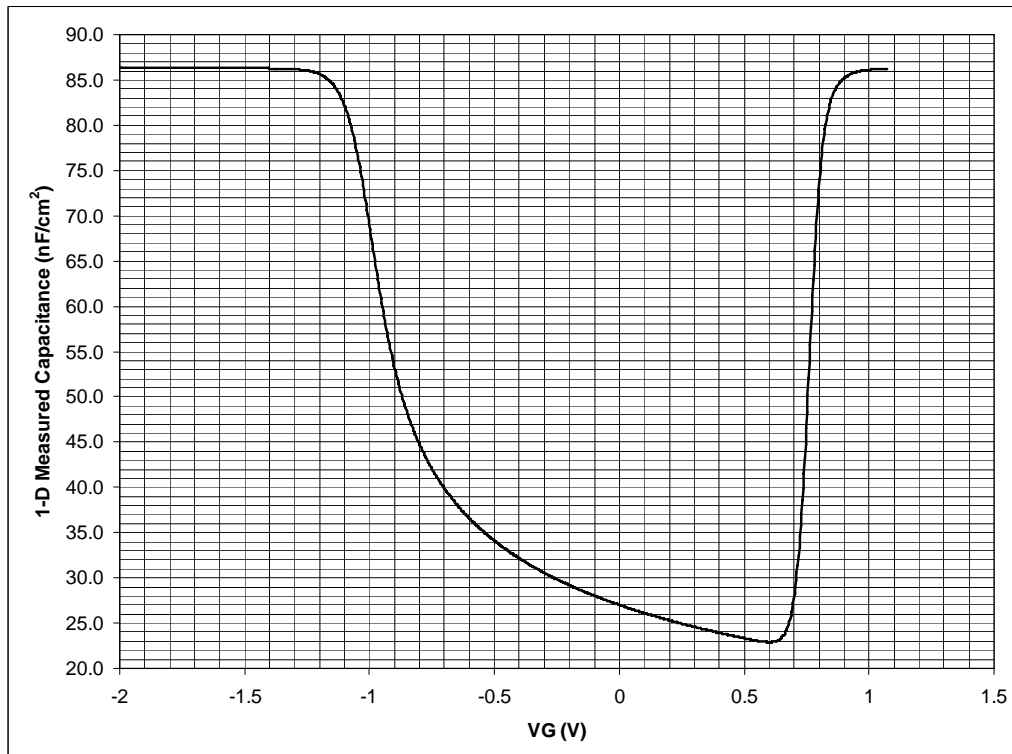


Figure 1: Measured 1-D CV plot of MIS capacitor.

8. What determines the MOS capacitance in accumulation mode? Does it depend on applied voltage?
9. What determines the MOS capacitance in depletion mode? Does it depend on the voltage applied?
10. Draw a picture of the device you are going to simulate in TCAD. Describe what you are going to measure, and extract. Include any relationships you will find or confirm.
11. Down load and run a few sample experiments from the TCAD file for your project. Some TCAD files exist for some projects. Others need to be created. You need to work with me on this.
12. \*\* Derive the relationship for the temperature dependence of the threshold voltage of a MOS capacitor.