

Question 1 (20 PTS):

You are designing a ring oscillator that is to oscillate as fast as possible. You usually need a set pin to start the ring oscillator properly. Which circuit would you use for your fastest ring oscillator?

Explain why for full credit. Reference Figure 2 for a NAND2.

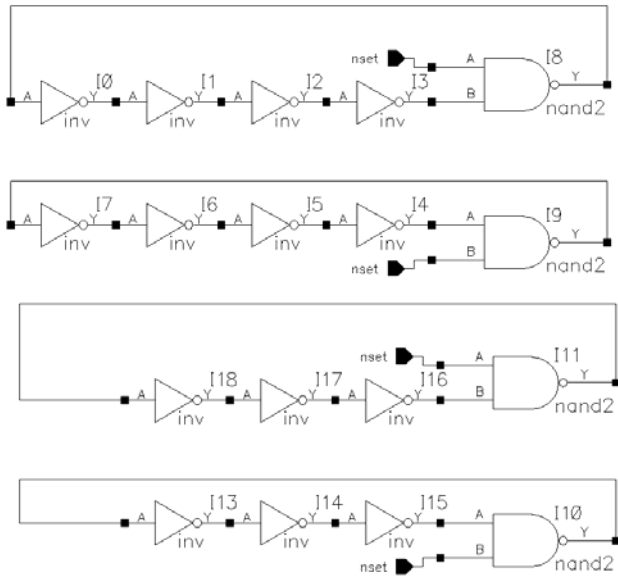


Figure 1: Proposed Ring Oscillator circuits.

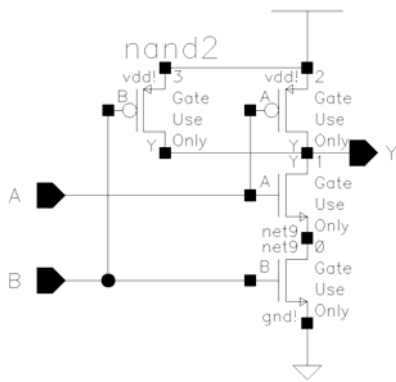


Figure 2: NAND3

Question 2 (20PTS):

You are designing a circuit. You see the following message (Figure 3). What does this message mean, and what should you do next? Explain for full credit.

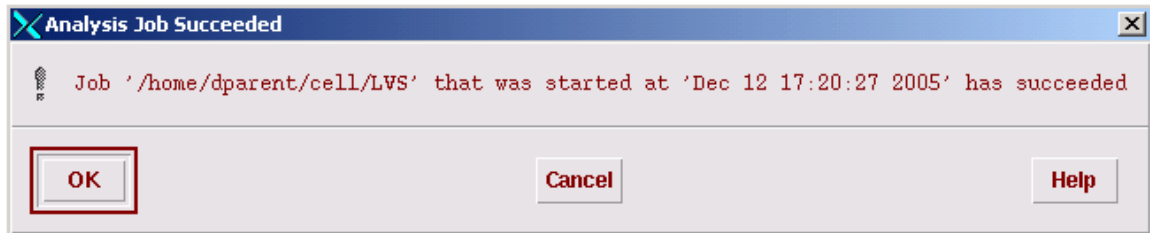


Figure 3: LVS job succeeded.

Explain all the reasons we do an LVS check (10PTS.)?

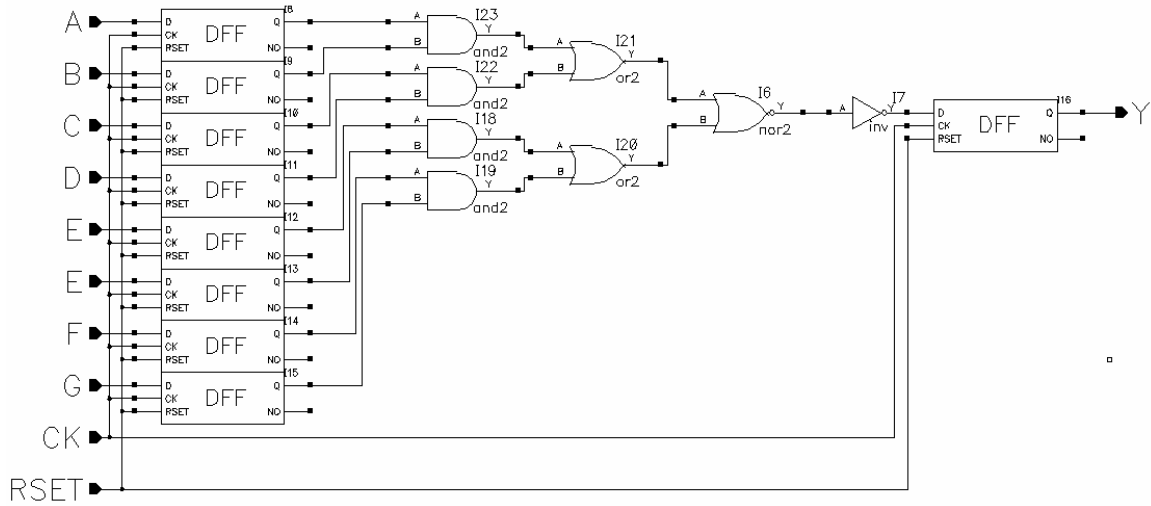


Figure 4: Logic.

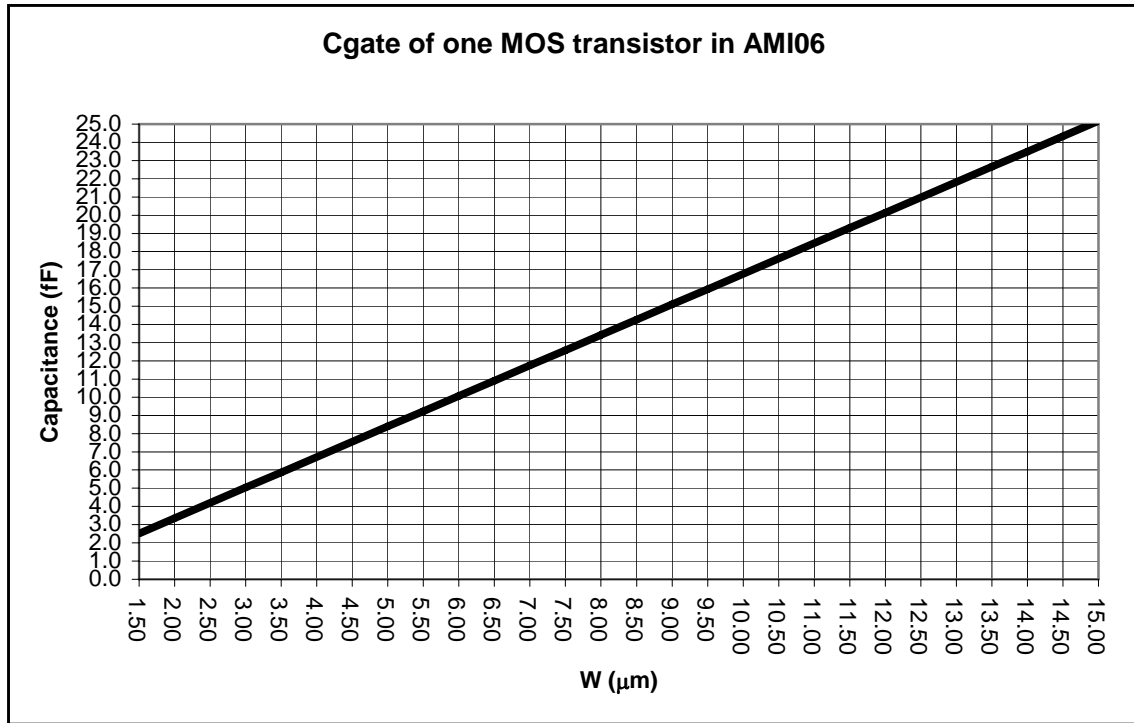


Figure 5: CG vs. WN.

INVERTER

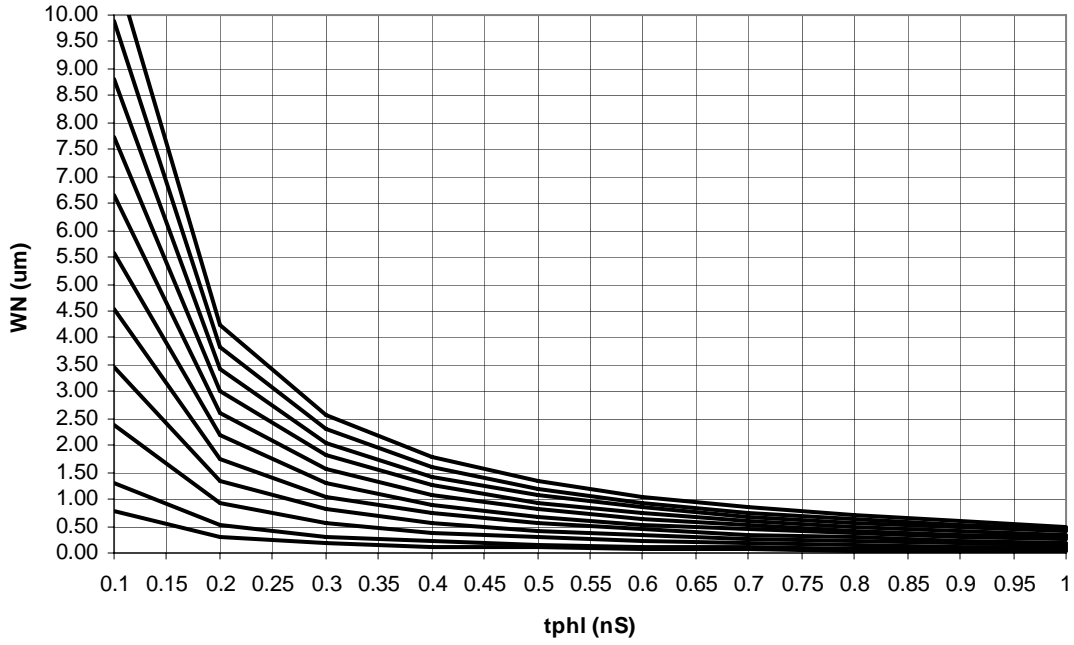


Figure 6: INV.

NAND2

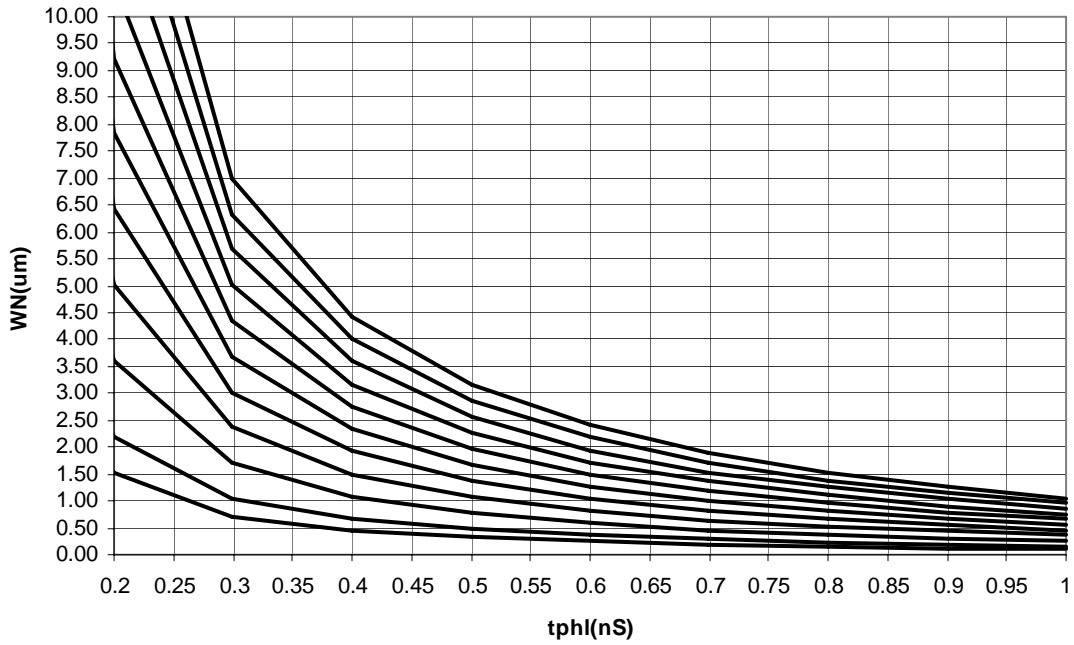


Figure 7: NAND2

NOR2

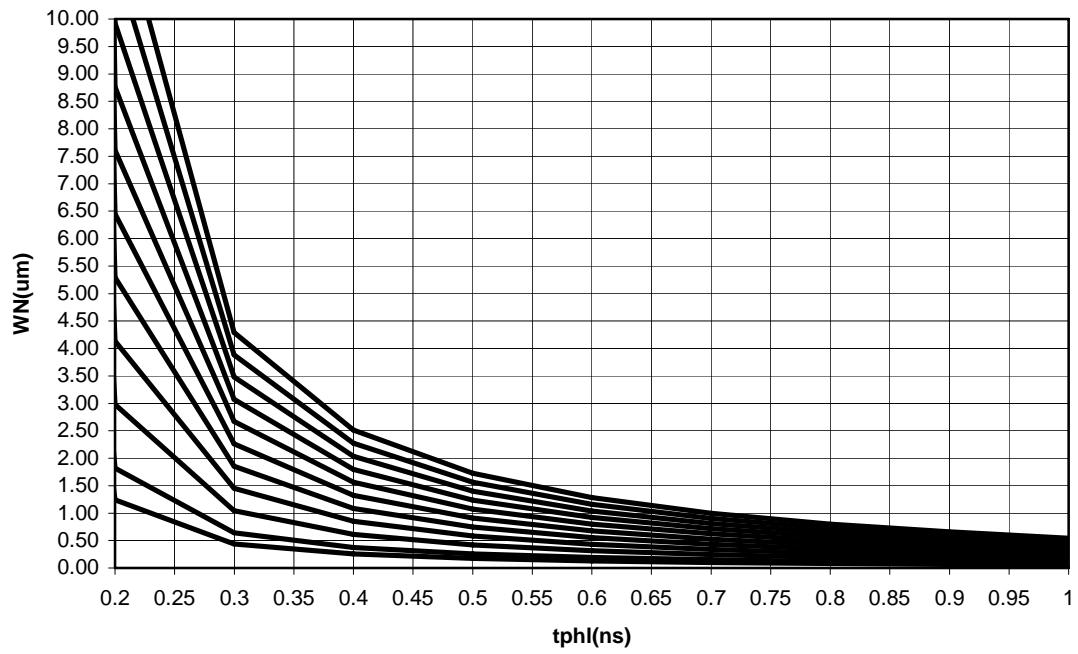


Figure 8: NOR2.

NAME:

Question 4 (20PTS):

Figure 9 shows some hand calculations for a circuit that is to operate at 550ps (no flips flops). The calculations are based on extracted A and R values from a spice schematic. There is a problem with the calculations. Explain what the problem is and all the ways to fix it. Explain for full credit.

CELL	WN Load (cm)	WP Load (cm)	Cg or Cin of load F	τ_{phl} s	A Ω	NSN	NSP	N	M	R	WN cm	WP cm
	Given	Given										
INV			2.5000E-14	5.50E-11	10300	1	1	1	1	2.16	1.13E-04	2.44E-04
nand2	1.13E-04	2.44E-04	3.3586E-14	5.50E-11	4940	2	1	3	2	0.912	1.73E-04	1.58E-04
nand2	1.73E-04	1.58E-04	7.9585E-15	5.50E-11	4940	4	1	3	2	0.912	1.99E-04	1.81E-04
nand2	1.99E-04	1.81E-04	1.7726E-14	5.50E-11	4940	4	1	3	2	0.912	4.25E-04	3.88E-04
nand2	4.25E-04	3.88E-04	1.9550E-14	5.50E-11	4940	4	1	3	2	0.912	4.67E-04	4.26E-04
INV	4.67E-04	4.26E-04	1.3873E-14	5.50E-11	10300	1	1	1	1	2.16	6.32E-05	1.36E-04
XOR	6.32E-05	1.36E-04	4.8032E-15	5.50E-11	5680	2	2	6	6	1.116	-2.62E-04	-2.92E-04
INV	-2.62E-04	-2.92E-04	-1.3319E-14	5.50E-11	10300	1	1	1	1	2.16	-5.84E-05	-1.26E-04
INV	-5.84E-05	-1.26E-04	-8.8807E-15	5.50E-11	10300	1	1	1	1	2.16	-3.86E-05	-8.33E-05
nand2	-3.86E-05	-8.33E-05	-1.1812E-14	5.50E-11	4940	2	1	3	2	0.912	-5.65E-05	-5.15E-05

Figure 9: Hand Calculations.

Question 5 (20PTS):

Draw a set of test vectors that show a setup violation for a positively edge triggered Flip-Flop with a setup time of 1ns.

Draw a set of test vectors that show a hold violation for a positively edge triggered Flip-Flop with a hold time of 1ns.

Question 6 (20PTS):

Using the AOI technique, design a CMOS circuit to implement the following logic function: Minimize area and delay. (Show Euler path, but do not draw it-no stick diagram!). Explain for full credit.

$$Z = \text{not}((AB + CD + EFG))$$

Show the PNET and the NNET connected into a circuit

Question 7 (20PTS):

Figure 10 shows identical NOR3 gates wired to measure VNORTH. Which configuration has the lowest VNORTH? Why?

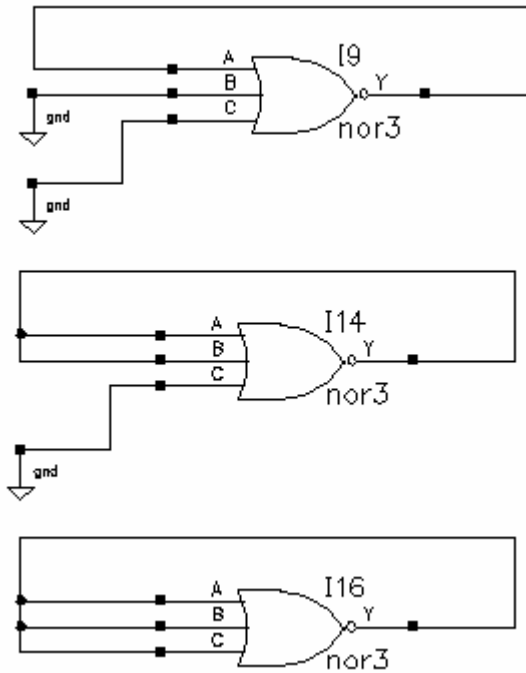


Figure 10: Nor3s.

Question 8 (10PTS):

You are designing a two input nand gate in a .18 microns process ($V_{DD}=1.8V$) Your test bench is pictured below (Figure 11). You have run your simulation (Figure 12). Estimate using Figure 11 the rise and fall time as well as the propagation delay low to high and hi to low for this simulation. Label each on the figure 11.

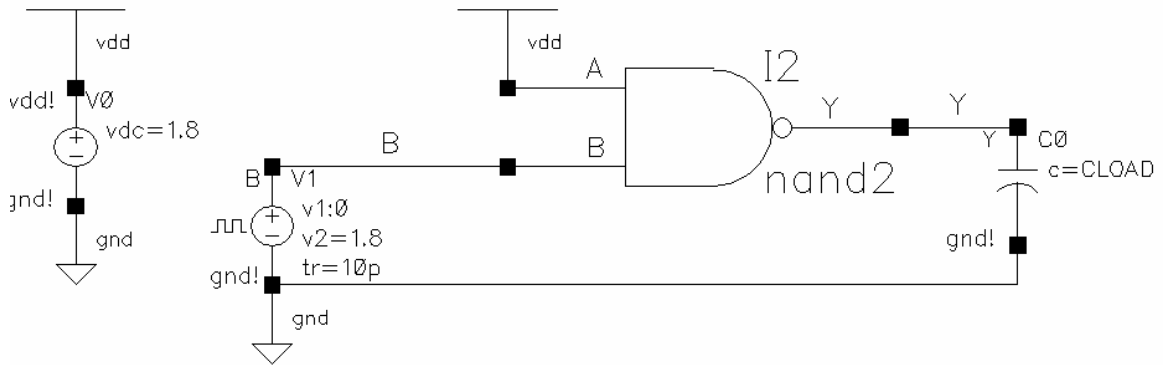


Figure 11: Nand2 Testbench.

tsmc18 nand2_tb schematic : Dec 12 17:11:58 2005

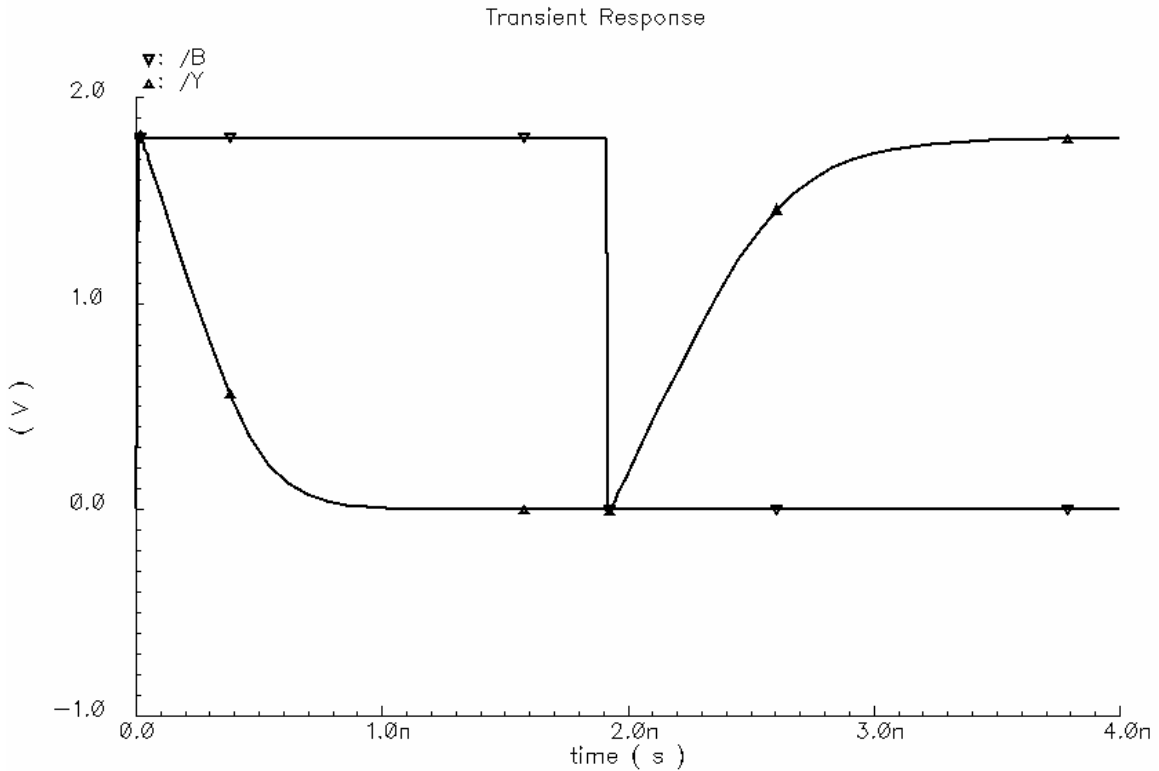


Figure 12: Transient response for a 2 input nand gate.

Question 9 (10PTS):

When should you use a super buffer? Explain for full credit.