

EE-166 Class 13

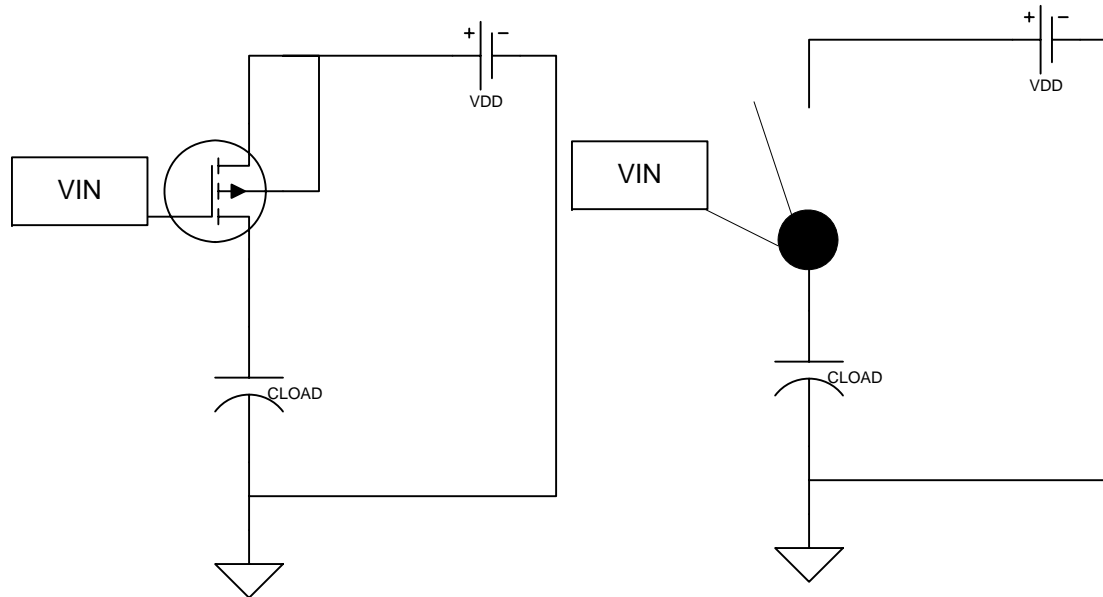
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SJSU

Switch Model of MOSFETS

- We can think of PMOSFETs in the following manner:
 - When $V_{IN}=5$ the source and drain are not connected
 - When $V_{IN}=0$ the source and drain are connected
- We can think of NMOSFETs in the following manner:
 - When $V_{IN}=5$ the source and drain are connected
 - When $V_{IN}=0$ the source and drain are not connected

PMOSFETs

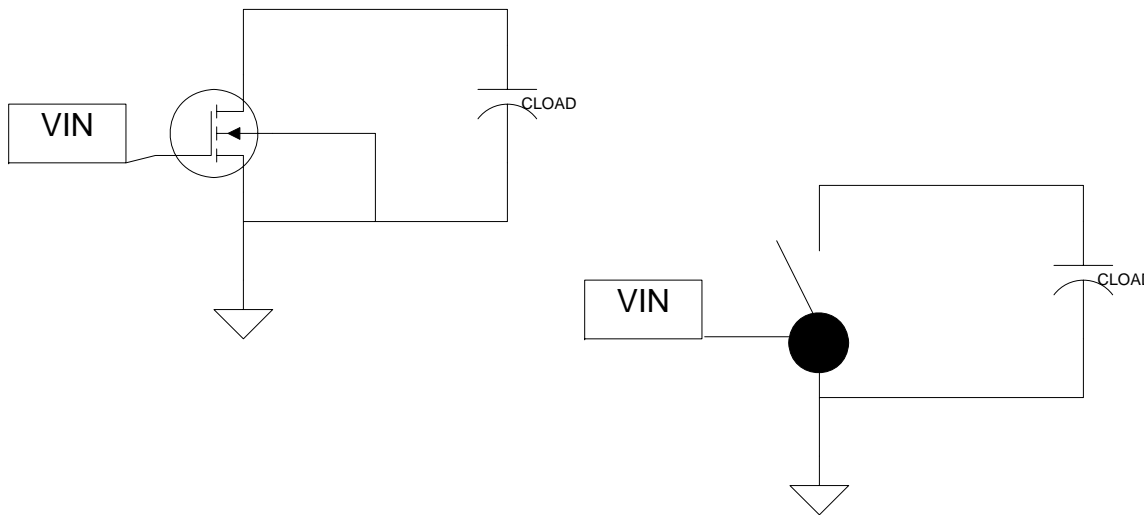
- Consider the following circuit:



- When the switch is closed, Cload is charged up to VDD.
- There is no path to discharge Cload.

NMOSFETs

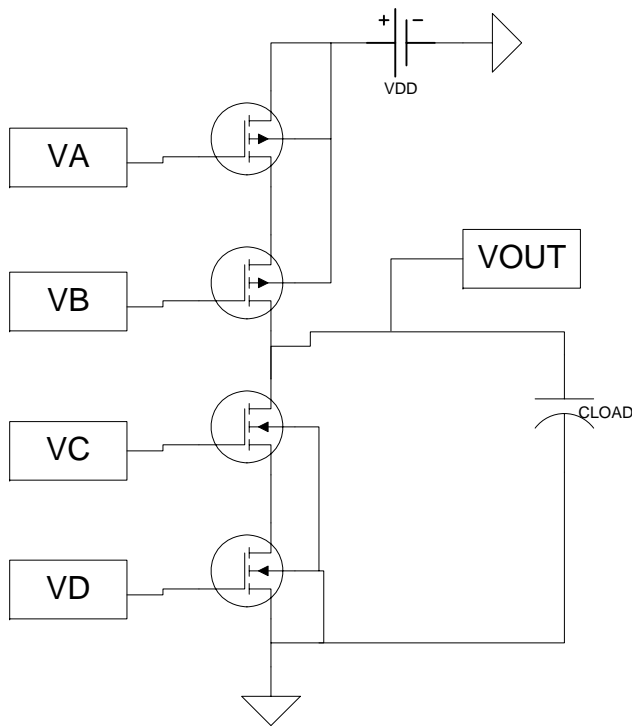
- Consider the following circuit:



- When the switch is closed, C_{LOAD} is discharged down to GND.
- There is no path to charge C_{LOAD} .

Example

- Determine the transfer function of the following circuit:

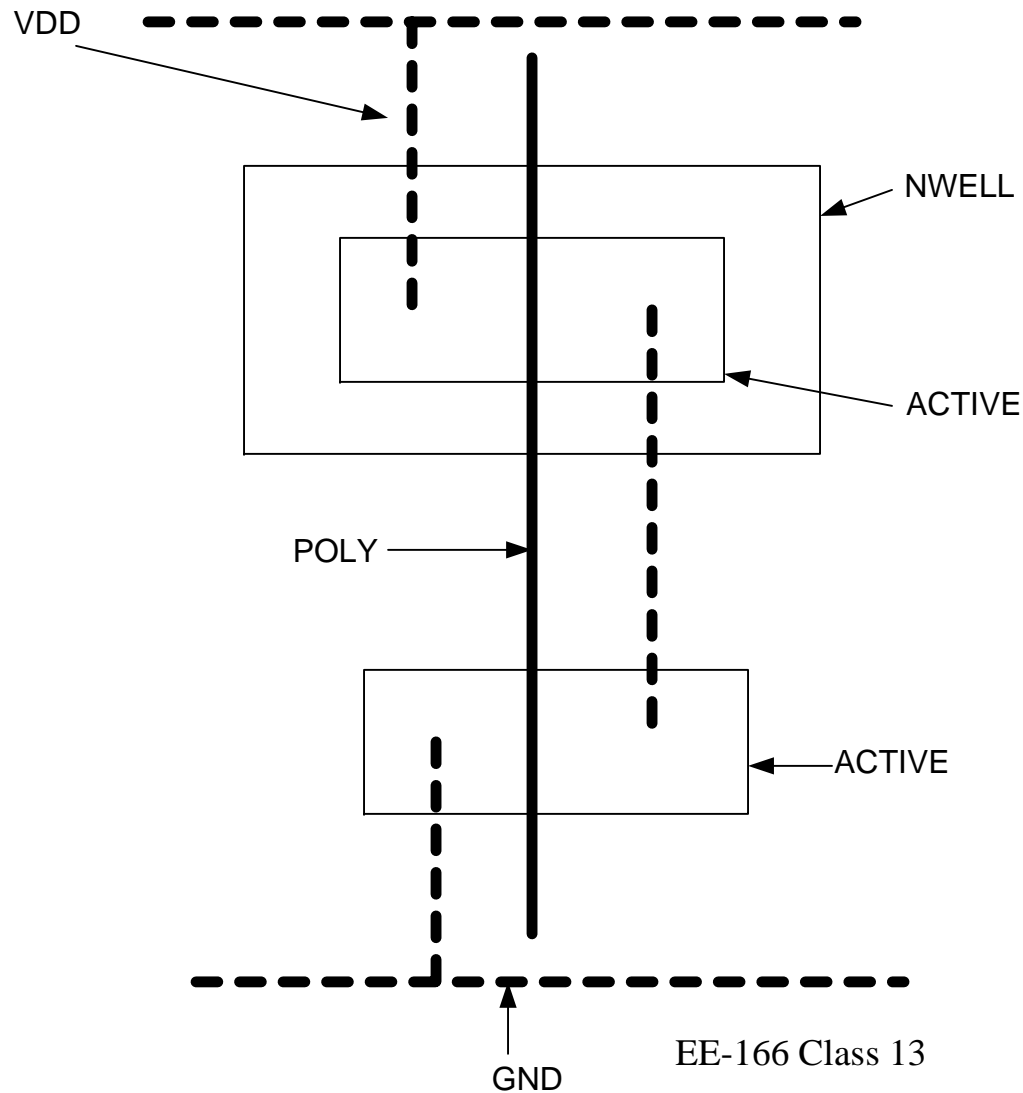


VA	VB	VC	VD	VOUT
0	0	0	0	
0	0	0	5	
0	0	5	0	
0	0	5	5	
0	5	0	0	
0	5	0	5	
0	5	5	0	
0	5	5	5	
5	0	0	0	
5	0	0	5	
5	0	5	0	
5	0	5	5	
5	5	0	0	
5	5	0	5	
5	5	5	0	
5	5	5	5	

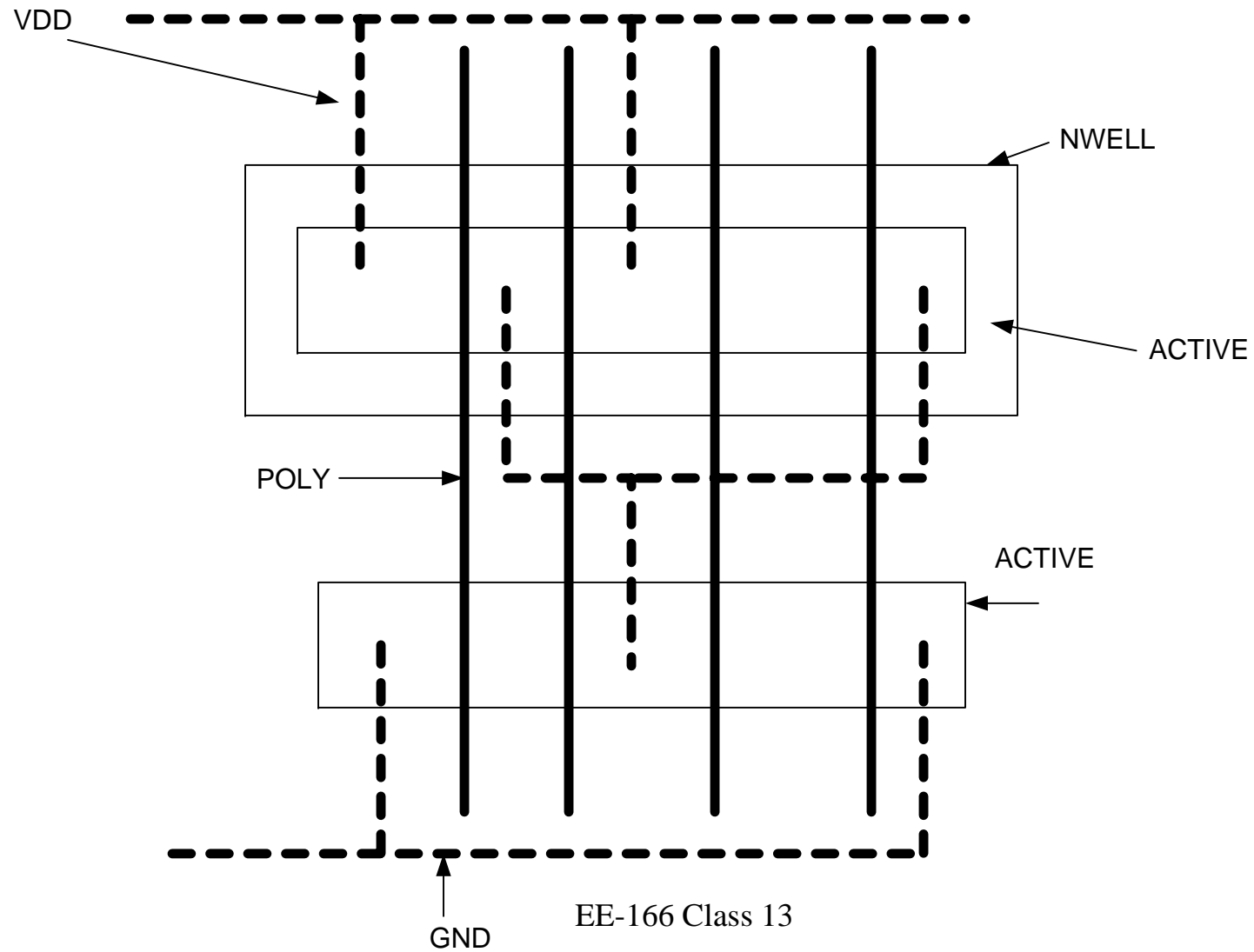
Stick Diagram

- We need a simpler way to represent our layouts so we can “rough in” where everything is going to go.
- Stick diagrams are our solution. They show:
 - NWELL, Poly, Active, Metal layers, and connections.
 - You do not even need color markers!

Inverter Representation



Random Functionality



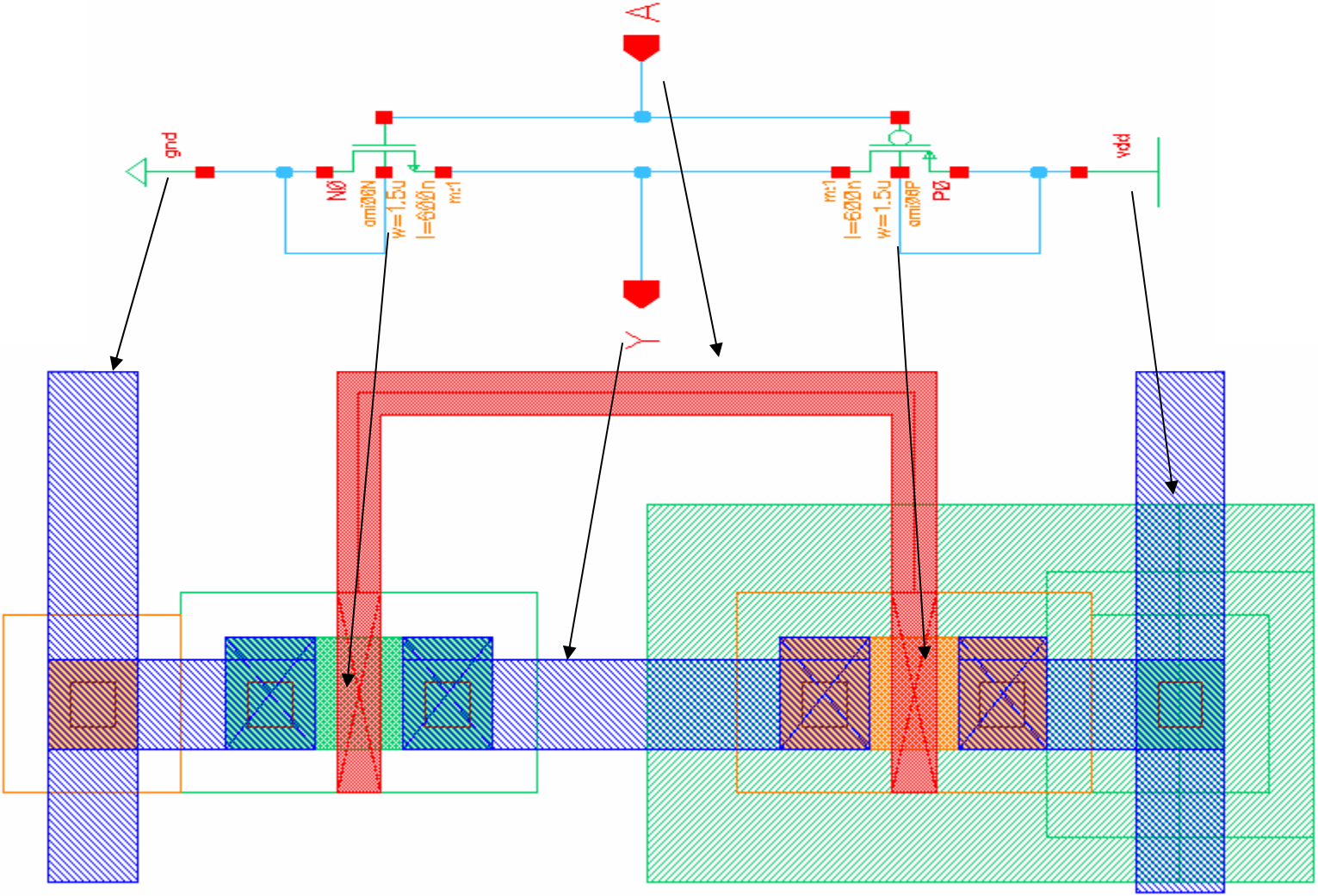
Additional Uses for the Stick Diagram

- Clock Routing/Trees
- Block Placement
- VDD Routing
- VSS (GND) Routing
- Pad Placement

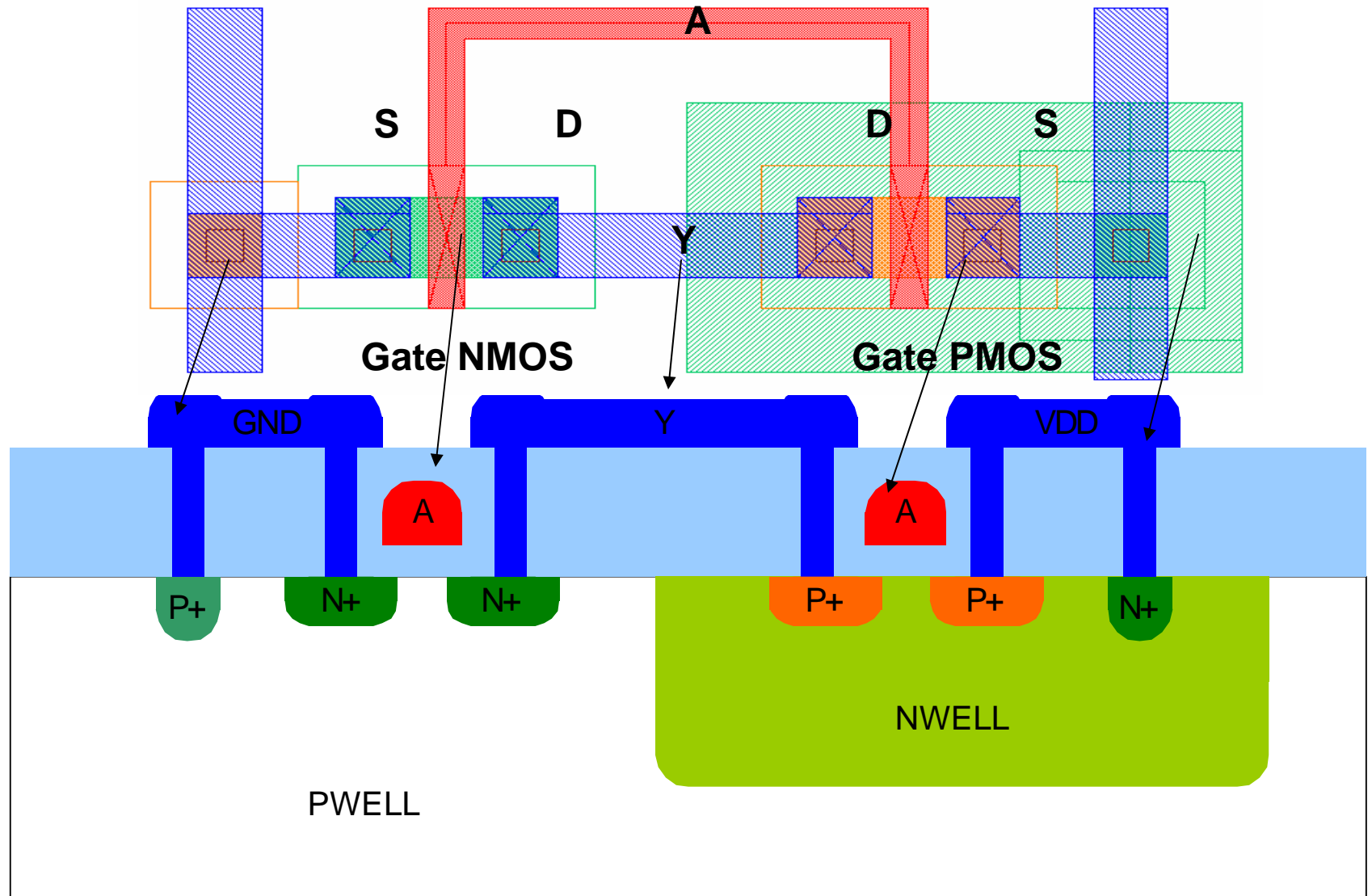
Layout

- Layout is the process of drawing how the circuit will look underneath a microscope.
 - Each layer represents very specific instructions to the fabrication house.
 - You need to know the basic CMOS fabrication steps to understand what each layer does

CMOS Inverter Schematic and Layout



CMOS Inverter Layout and Cross Section



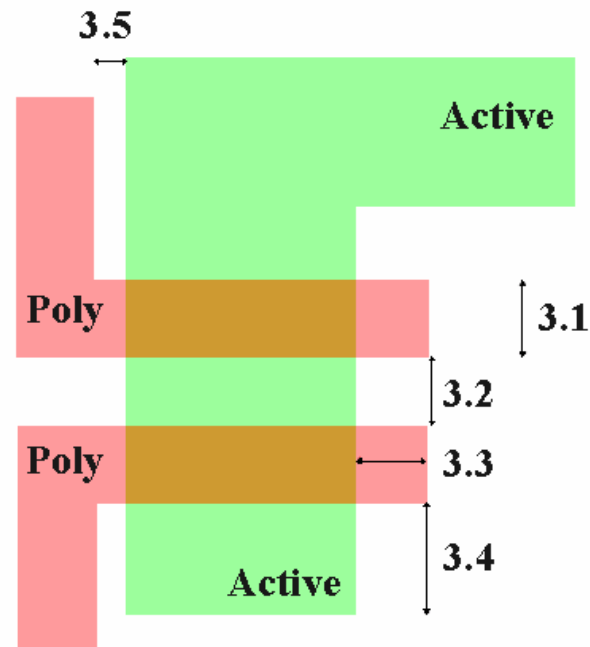
Design Rule Checking

- Every layer has its own rules with respect to minimum size, spacing and overlap to other layers. This is done to insure that all the devices work even after variances of the real world creep in.
- Running DRC, check for violations in your layout file.

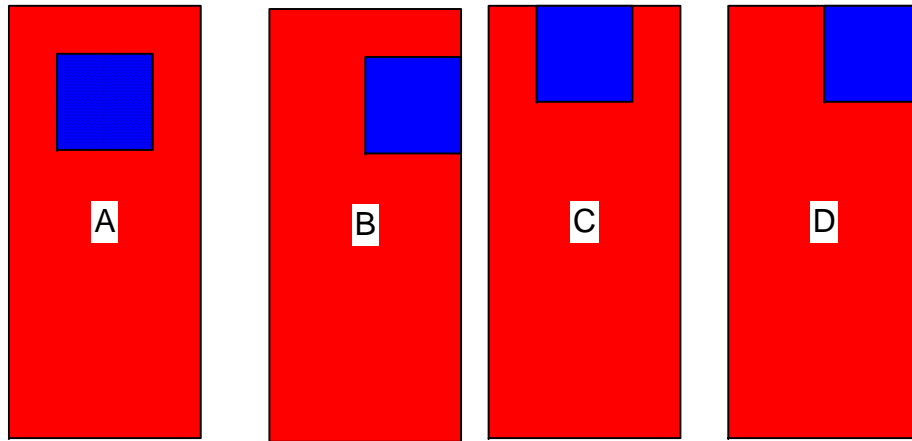
<http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html>

Design Rule Checking

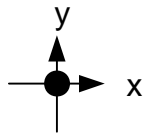
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



Alignment Errors



We need to have a minimum overlap of the metal to contact to take into account the inherent errors in alignment.



- A- No Errors
- B- Worst Case x misalignment
- C- Worst Case y misalignment
- D- Worst case x and y

Design Rules for a Process

- For high yields we need to have a process that can withstand large process variations
 - $\frac{1}{2}$ of our smallest feature size is equal to λ .

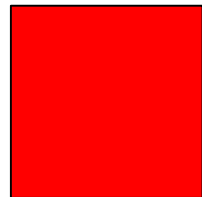
□ λ is equal to 45nm μm



Minimum contact width 2λ



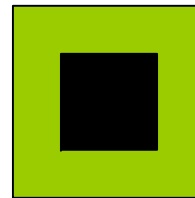
Minimum Diffused (N^+) width 2λ



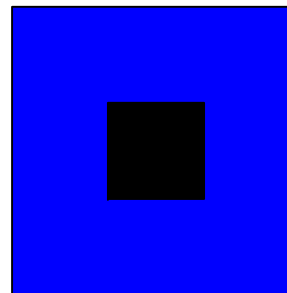
Minimum Gate Oxide Length (N^+) width 4λ



Minimum Metal width 2λ



Minimum Diffused/contact overlap 1λ



Minimum Metal/contact overlap 2λ

Layout vs. Schematic

- Once your circuit is laid out, and passes DRC, you need to extract a circuit from the picture you drew and compare it to the schematic you designed and verified (LVS)
- After a successful LVS you need to re-run your simulation to make sure you are still within Specification.

Basic Processing Steps

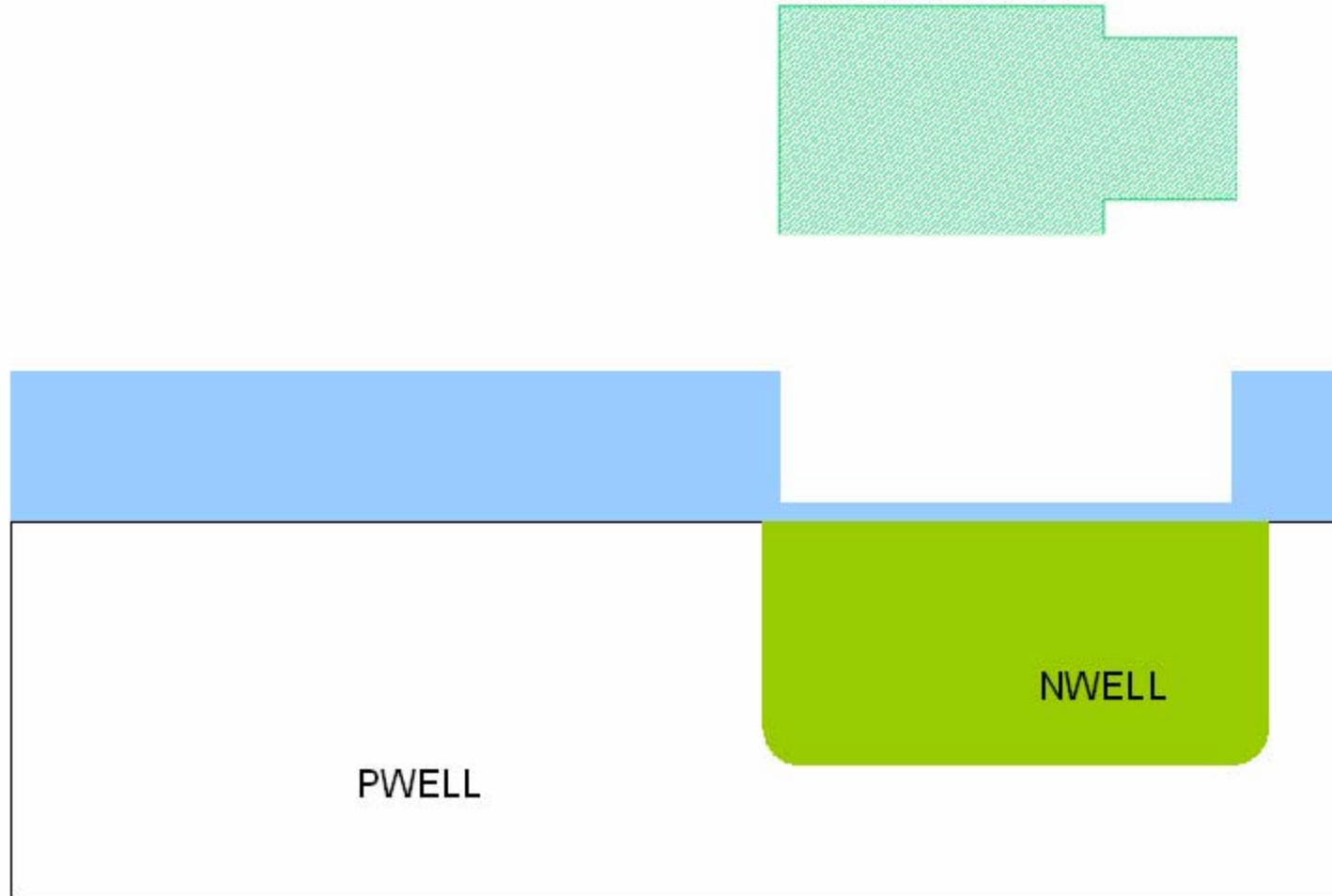
- Grow Silicon Dioxide
- Create NWELL regions (Implant)
- Etch Active regions and grow gate oxide
 - VT adjust Implant (NACTIVE=PACTIVE)
- Deposit Poly Silicon (POLY1)
 - Dope, then Pattern

Basic Processing Steps

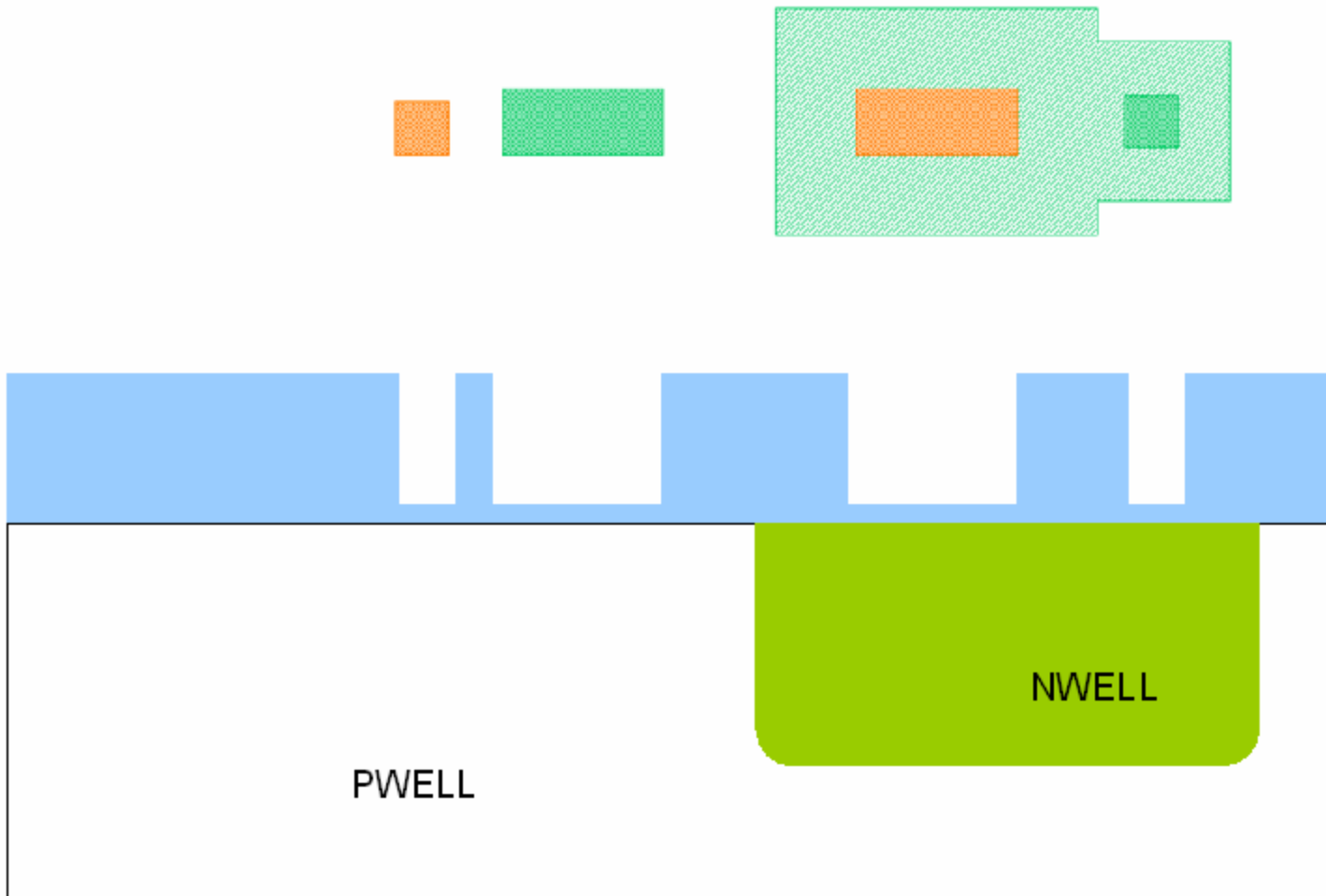
- Implant P+ Source and Drain for PMOS and body contact for NMOS (PSEL)
- Implant N+ Source and Drain for NMOS and body contact for PMOS (NSEL)
- Create Contact windows (CONT)
- Deposit and pattern metal layer (METL1)

NWELL

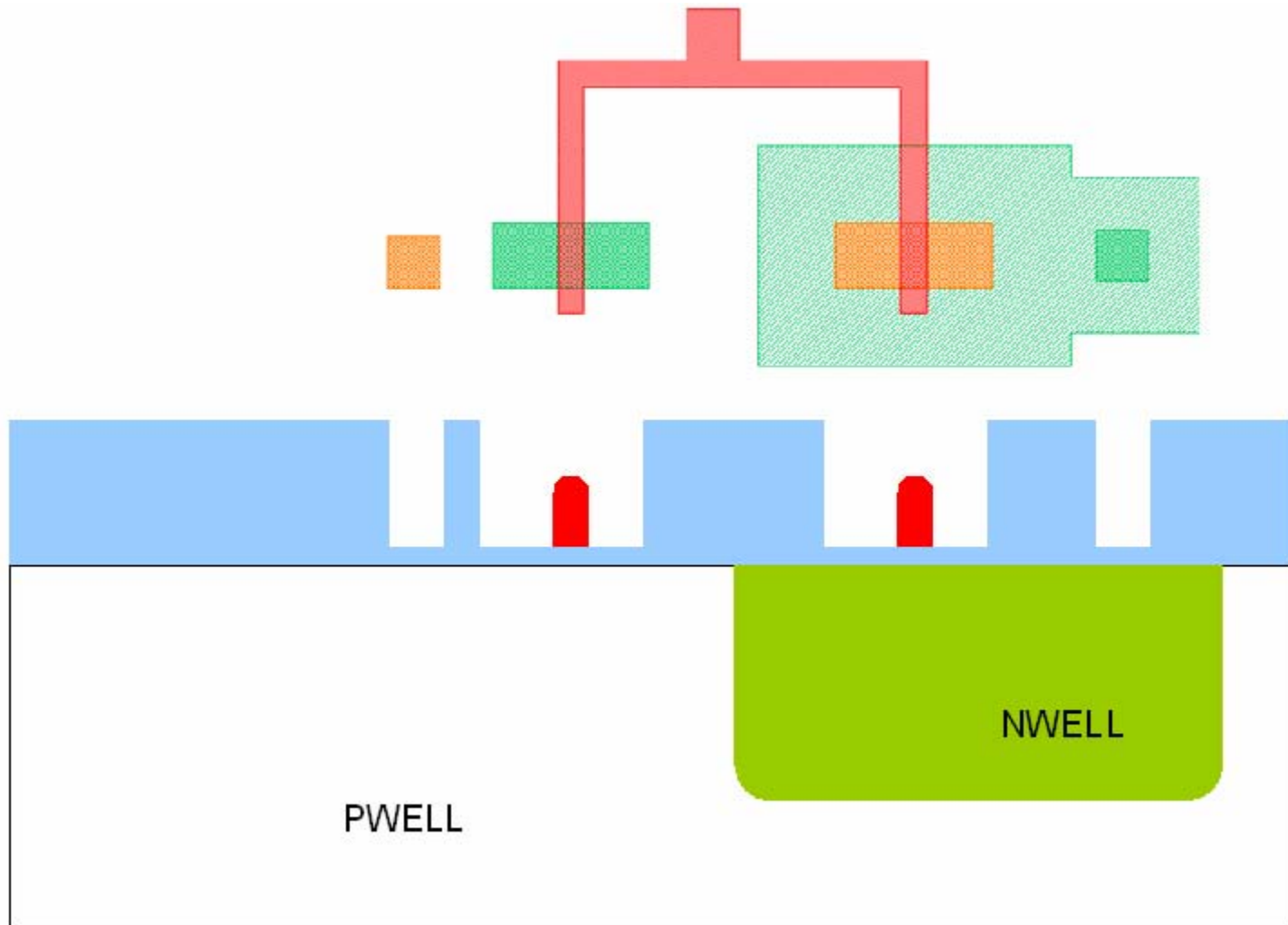
Note: Channel Stop implants not shown.



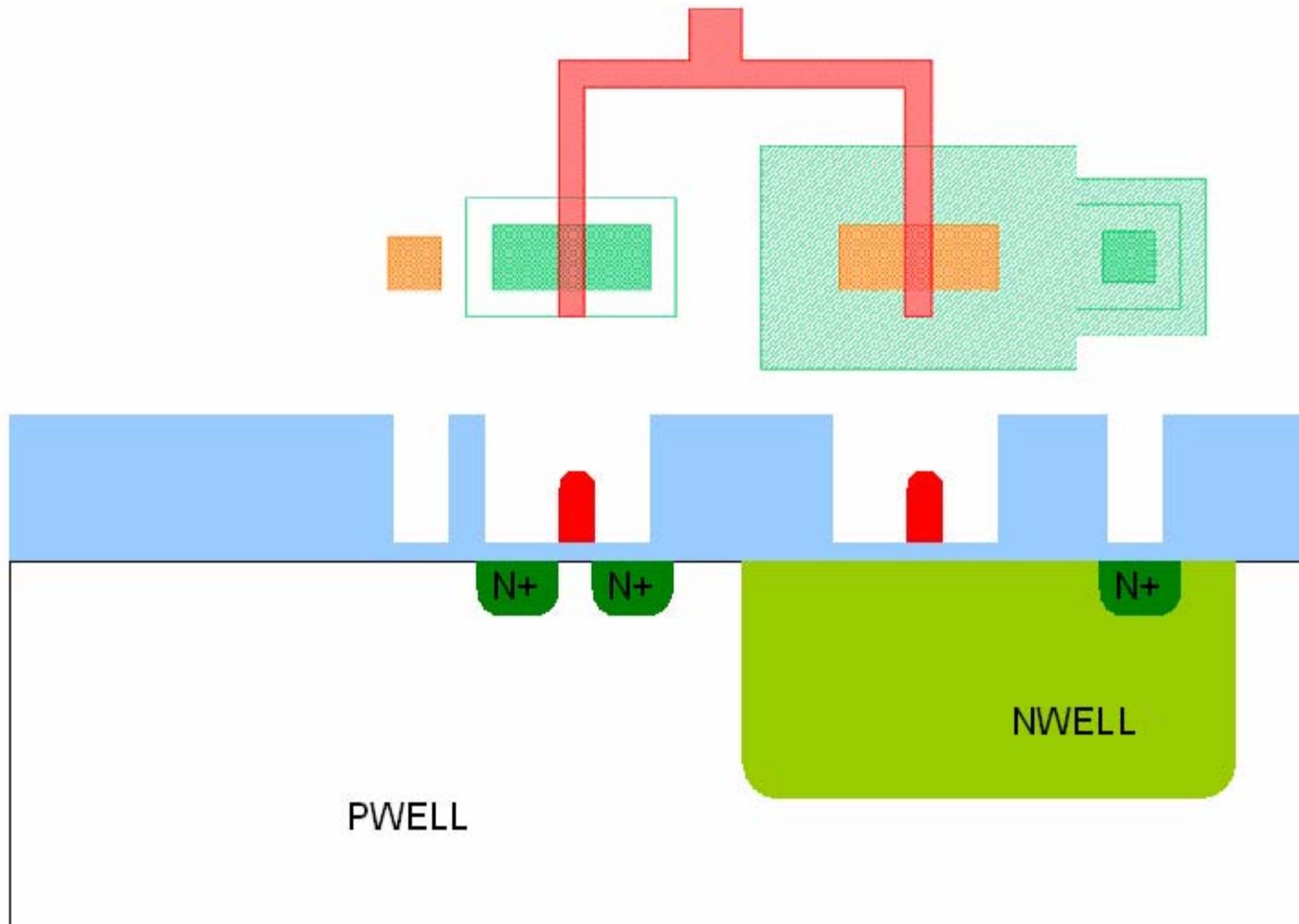
Active



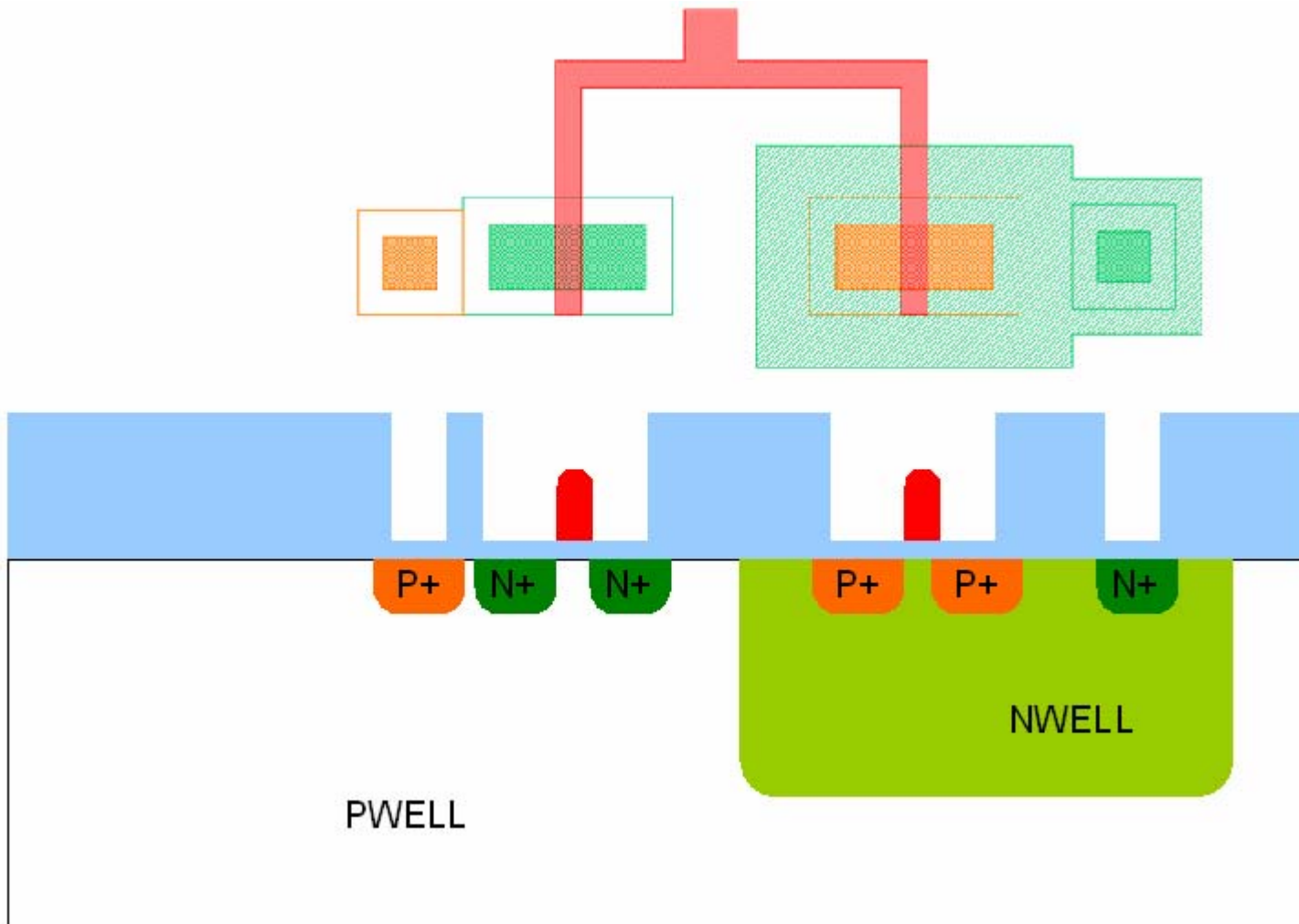
Poly



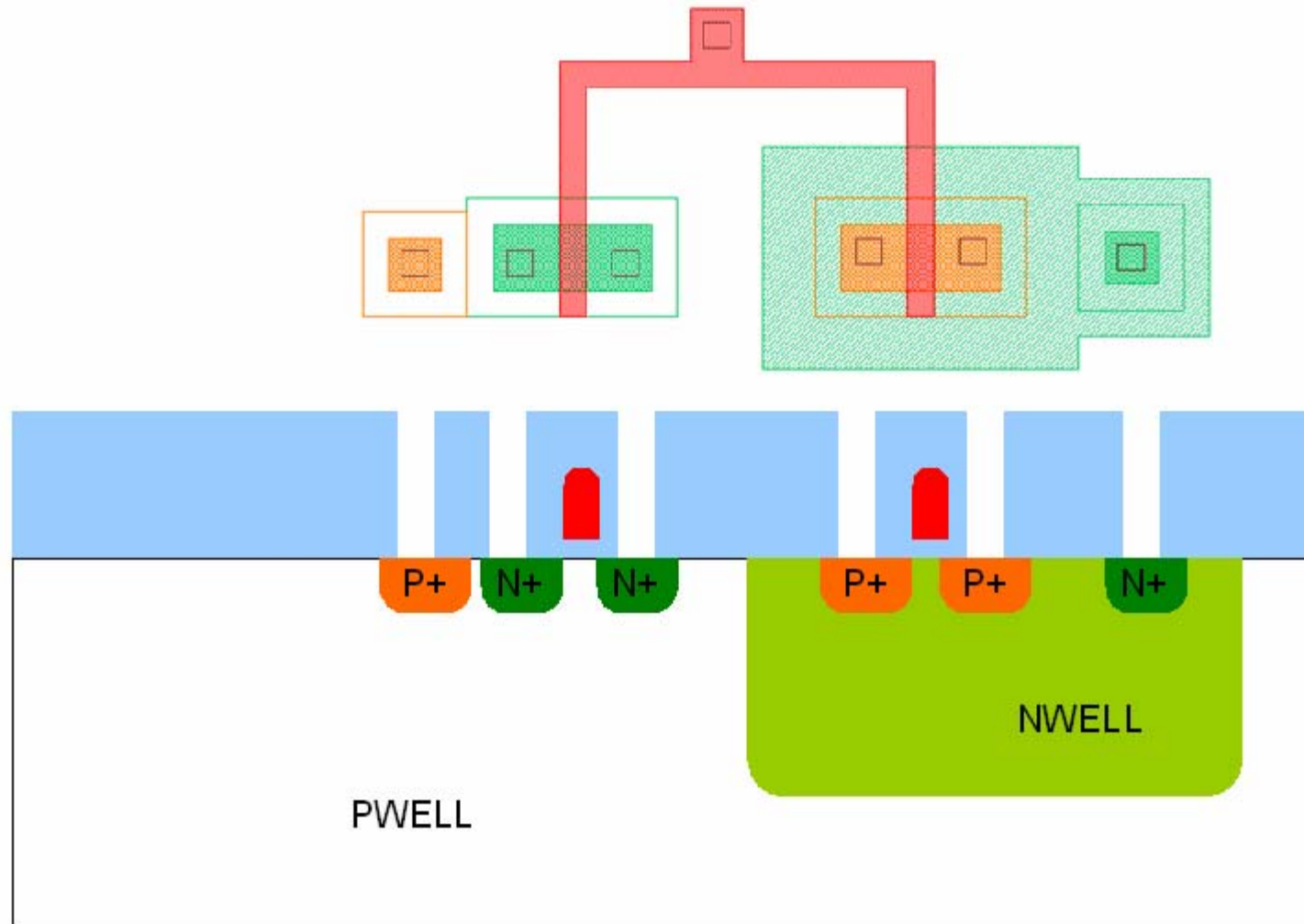
N Select



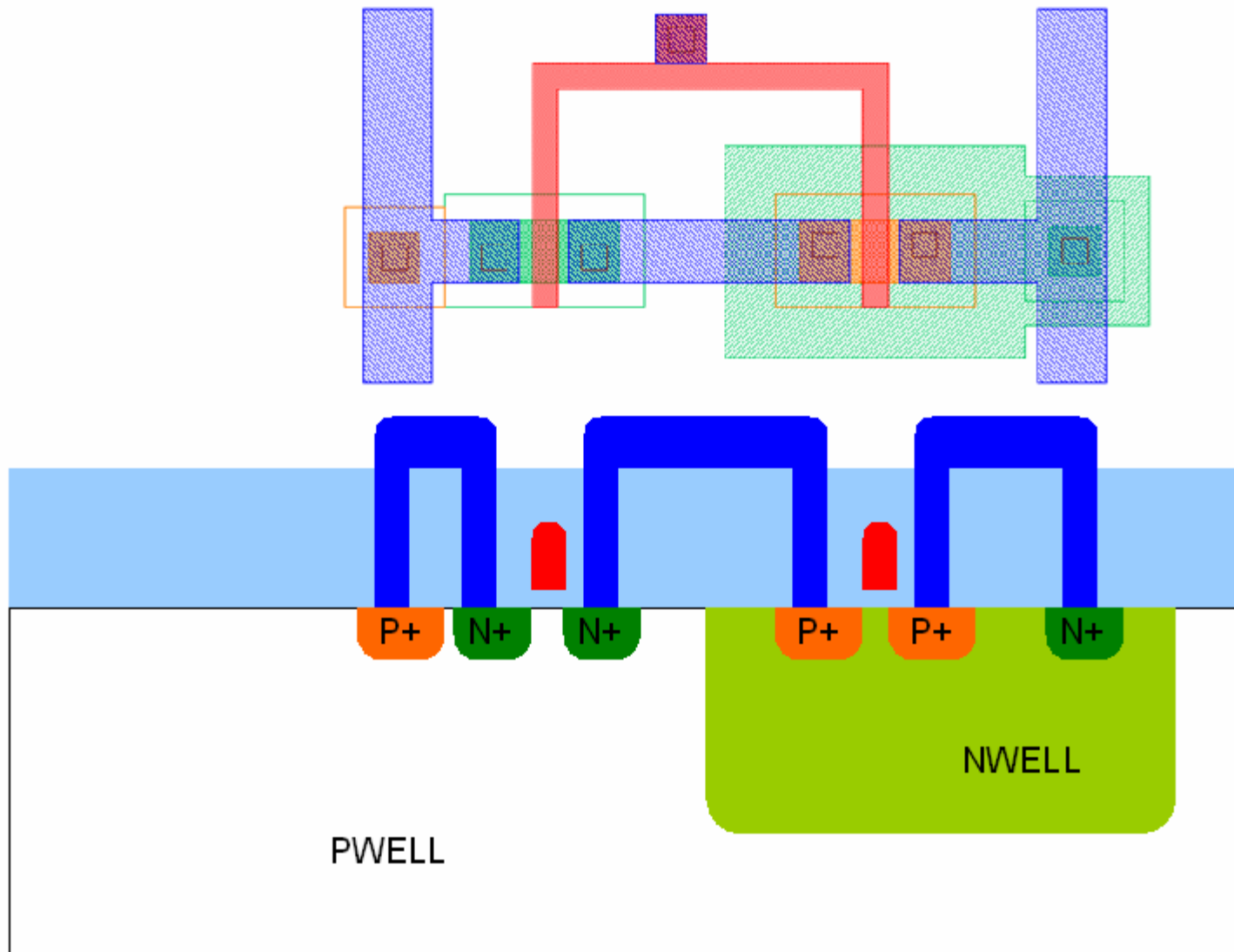
P Select



Blanket CVD Oxide and Contact (cc)



Metal 1



Vias in IC design

- In PCB manufacture Vias (Hole between layers go through the whole board.
- In IC Design a via connects only two metal layers.

