

**Question 1(50pts):**

1. Design a 2 input NOR gate to have worst-case propagation delays of .21ns driving a 20f F load.
  - a. Show Hand Calculations
  - b. Verify in Spice (make modifications as required) to be with in plus or minus 5%.
  - c. Show detailed stick diagram
  - d. Layout Circuit **(Use cell height of 30μm)**
  - e. DRC
  - f. LVS
  - g. Verify specification of extracted circuit

Measure in spice  $V_{NNORTH}$ .

The screen grabs must be of a professional quality as if they were going into a final report.

<http://www.engr.sjsu.edu/~dparent/ICGROUP/graphics.pdf>

$$\begin{aligned}
 S_g &:= 1 & C_g &:= 20 \cdot 10^{-15} \text{F} & C_{int} &:= 0 \text{F} & \tau_{PHL} &:= .21 \cdot 10^{-9} \text{s} & D_{Drain} &:= 1.5 \cdot 10^{-4} \text{cm} \\
 N_{SP} &:= 2 & N_{SN} &:= 1 & N_{NW} &:= 2 & M &:= 3 & L_N &:= .6 \cdot 10^{-4} \text{cm} \\
 m1 &:= -5 \cdot 10^{12} \frac{\Omega}{\text{s}} & m2 &:= -250 \cdot 10^6 \text{Hz} & b_1 &:= 12.8 \cdot 10^3 \Omega & b_2 &:= 1.83 \\
 A &:= m1 \cdot \tau_{PHL} + b_1 & R &:= m2 \cdot \tau_{PHL} + b_2 & R_{NW} &:= \frac{S \cdot R \cdot N_{SP}}{N_{SN}} & A &= 1.175 \times 10^4 \Omega & R &= 3.555 \\
 W_N &:= \frac{C_g + C_{int} + C_{JSWN} \cdot 2 \cdot D_{Drain} \cdot (N + M)}{\frac{\tau_{PHL}}{N_{SN} \cdot L_N \cdot A} - (N + M) \cdot R \cdot (C_{JSWN} \cdot 2 + C_{JN} \cdot D_{Drain})} & W_N &= 2.131 \times 10^{-4} \text{cm} \\
 W_P &:= R \cdot W_N & W_P &= 7.575 \times 10^{-4} \text{cm}
 \end{aligned}$$

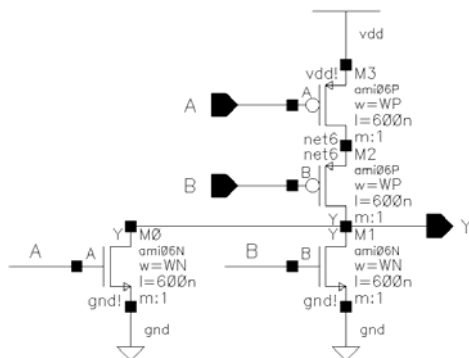


Figure 1: Schematic of NOR2.

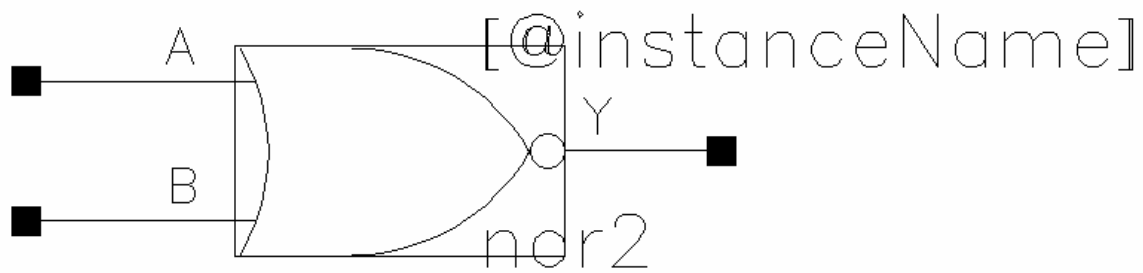


Figure 2: Symbol of NOR2.

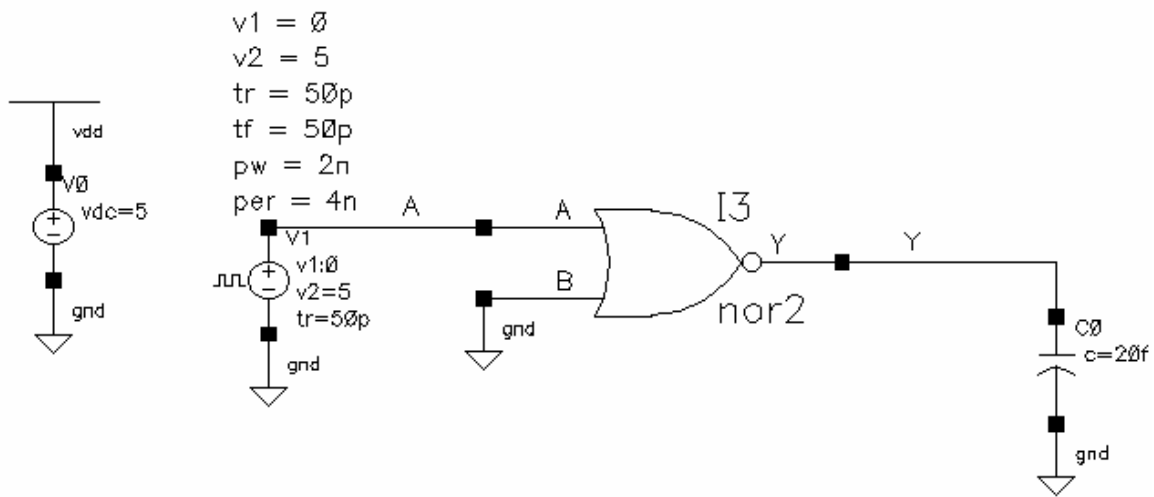
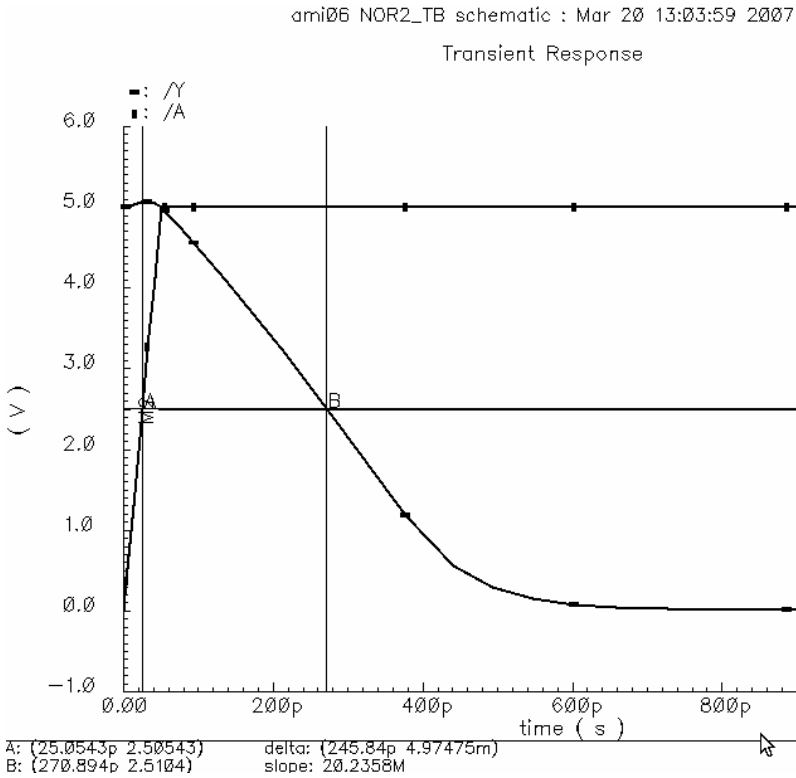
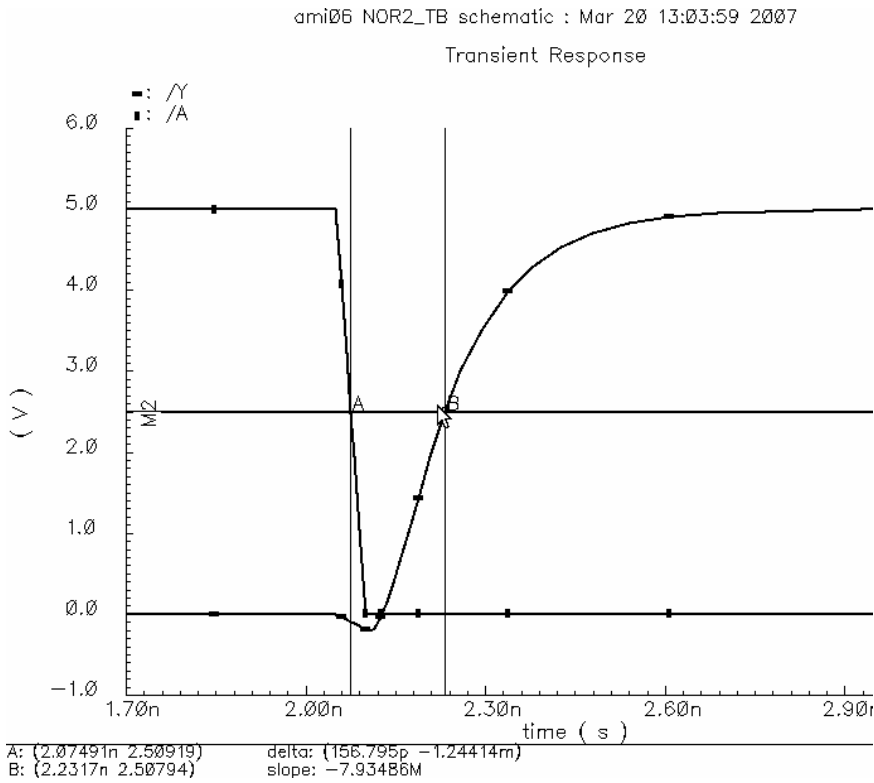


Figure 3: Testbench for NOR2, Worst Case.



**Figure 4: Propagation Delay High to Low for NOR2, first run.**



**Figure 5: Propagation Delay low to High for first run NOR2.**

NAME:

Run		Cross Point 2	Cross Point 1	Delay	Specification	Relative Error	Old W	New W
1	NMOS	272	25	247	210	17.61904762	2.1	2.47
1	PMOS	2231	2075	156	210	-25.7142857	7.6	5.645714
2	NMOS	195	25	170	210	-19.047619	2.47	1.999524
2	PMOS	2268	2075	193	210	-8.0952381	5.645714	5.18868
3	NMOS	235	25	210	210	0	1.999524	1.999524
3	PMOS	2273	2075	198	210	-5.71428571	5.18868	4.892184

Figure 6: Delay, and WN WP choices for three runs.

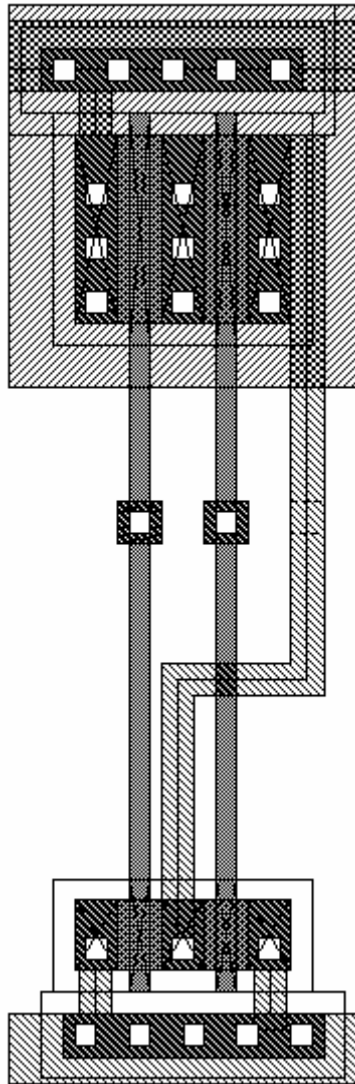
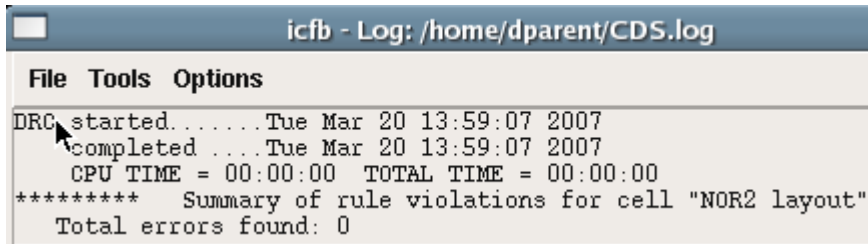


Figure 7: NOR2 Layout.

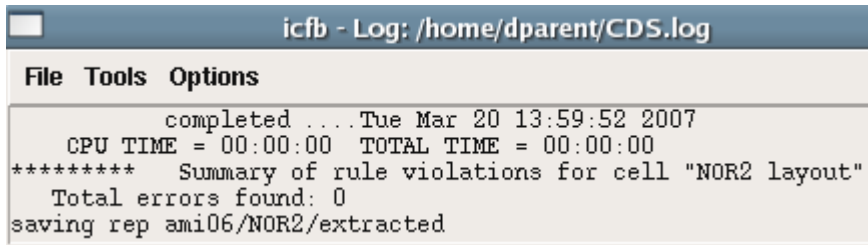


```

icfb - Log: /home/dparent/CDS.log
File Tools Options
DRC started.....Tue Mar 20 13:59:07 2007
completed ....Tue Mar 20 13:59:07 2007
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NOR2 layout"
Total errors found: 0

```

Figure 8: DRC Clean!

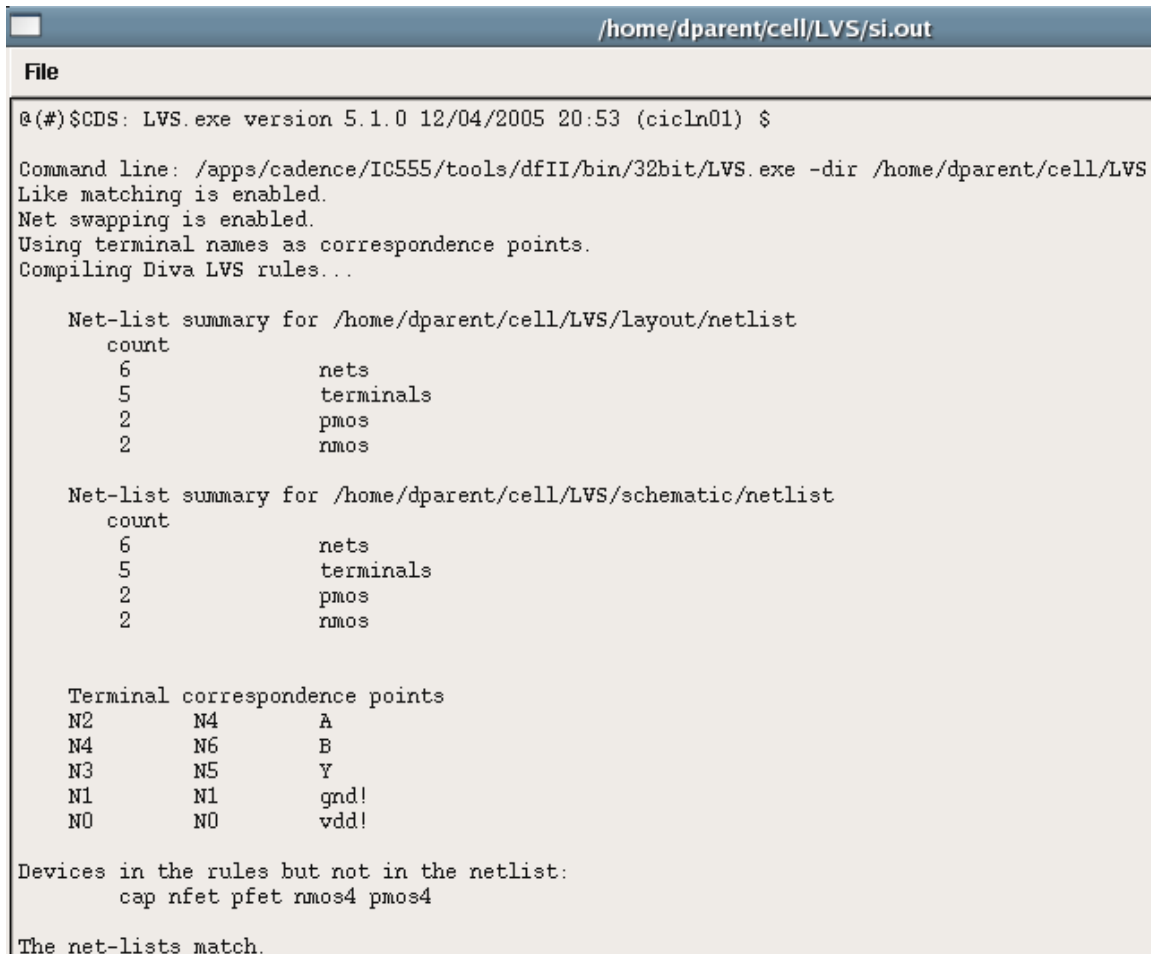


```

icfb - Log: /home/dparent/CDS.log
File Tools Options
completed ....Tue Mar 20 13:59:52 2007
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NOR2 layout"
Total errors found: 0
saving rep ami06/NOR2/extracted

```

Figure 9: Extraction Clean!



```

/home/dparent/cell/LVS/si.out
File
@(#)$CDS: LVS.exe version 5.1.0 12/04/2005 20:53 (cicln01) $
Command line: /apps/cadence/IC555/tools/dfII/bin/32bit/LVS.exe -dir /home/dparent/cell/LVS
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/dparent/cell/LVS/layout/netlist
count
  6          nets
  5          terminals
  2          pmos
  2          rmos

Net-list summary for /home/dparent/cell/LVS/schematic/netlist
count
  6          nets
  5          terminals
  2          pmos
  2          rmos

Terminal correspondence points
N2      N4      A
N4      N6      B
N3      N5      Y
N1      N1      gnd!
N0      N0      vdd!

Devices in the rules but not in the netlist:
  cap nfet pfet rmos4 pmos4

The net-lists match.

```

Figure 10: LVS Passes!

```
icfb - Log: /home/dparent/CDS.log
File Tools Options
***** Summary of rule violations for cell "NOR2 layout"
Total errors found: 0
saving rep ami06/NOR2/extracted
Building analog_extracted view for NOR2
Done
```

Figure 11: Analog Extracted is generated.

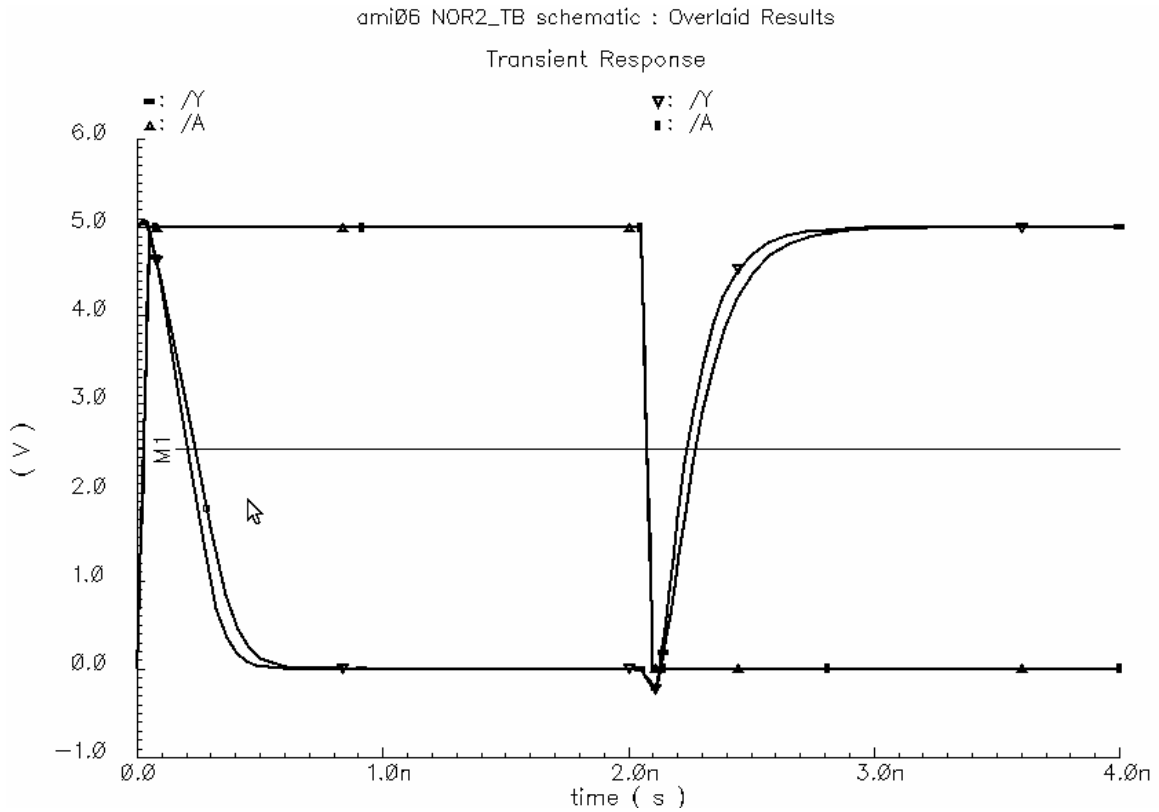


Figure 12: Analog Extracted and Schematic Transient Response of NOR2.

```
* # FILE NAME: /HOME/DPARENT/CADENCE/SIMULATION/NOR2_TB/SPECTRES/SCHEM
* begin cppStatements
#include </home/dparent/cadence/simulation/NOR2_TB/spectreS/schematic/
* end cppStatements

* netlist/NOR2_TB.C.raw
* Netlist output for spectreS.
* Generated on Mar 20 14:08:15 2007

* global net definitions
.GLOBAL vdd!

simulator lang= spectre
* File name: ami06_NOR2_TB_schematic.s.
* Subcircuit for cell: NOR2_TB.
* Generated for: spectreS.
* Generated on Mar 20 14:08:15 2007.

xi3 (a 0 y) NOR2_g1
c0 (y 0) capacitor c=20e-15 m=1.0
v1 (a 0) vsource type= pulse val0=0.0 vall=5.0 period=4e-9 rise=50e-
+fall=50e-12 width=2e-9 fundname= Fname14
v0 (vdd! 0) vsource type= dc dc=5.0

simulator lang= spice

simulator lang= spectre
simulator lang= spice

* File name: ami06_NOR2_analog_extracted.s.
* Subcircuit for cell: NOR2.
* Generated for: spectreS.
* Generated on Mar 20 14:08:15 2007.

simulator lang= spectre
```

Figure 13: Output from Simulation... Netlist... Display Final showing analog extracted being used.

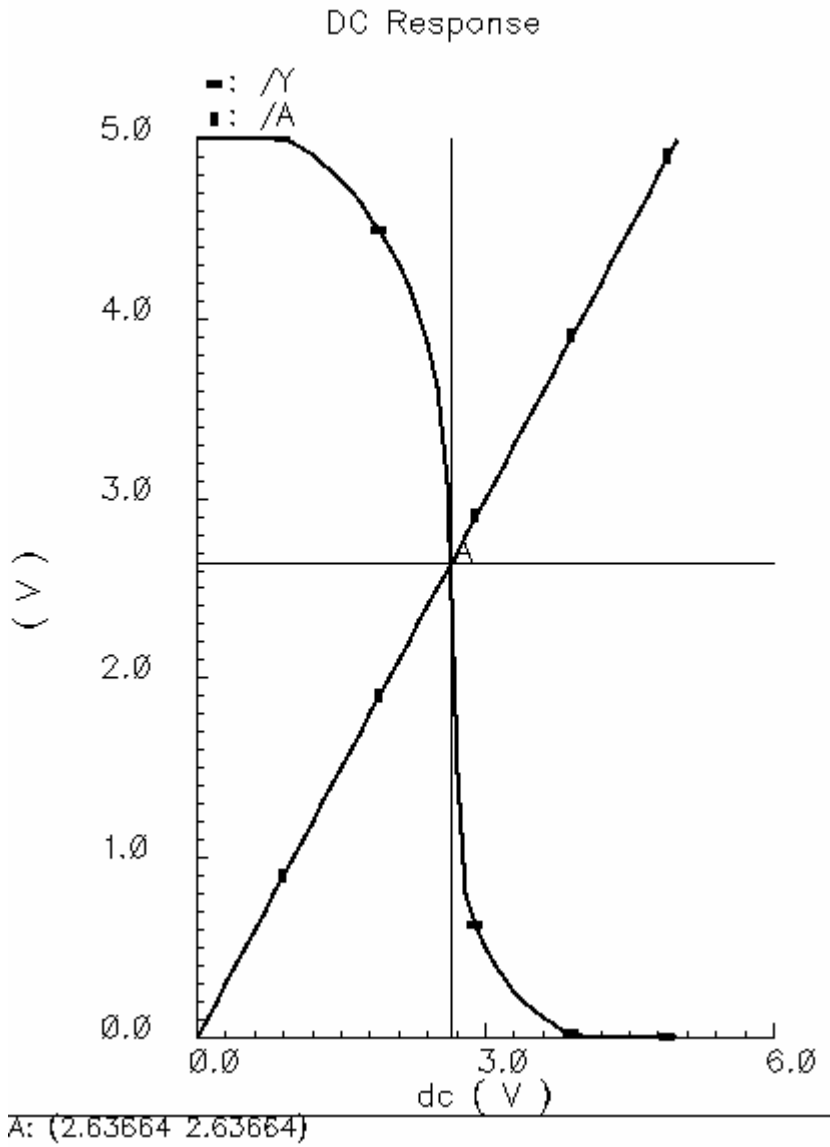
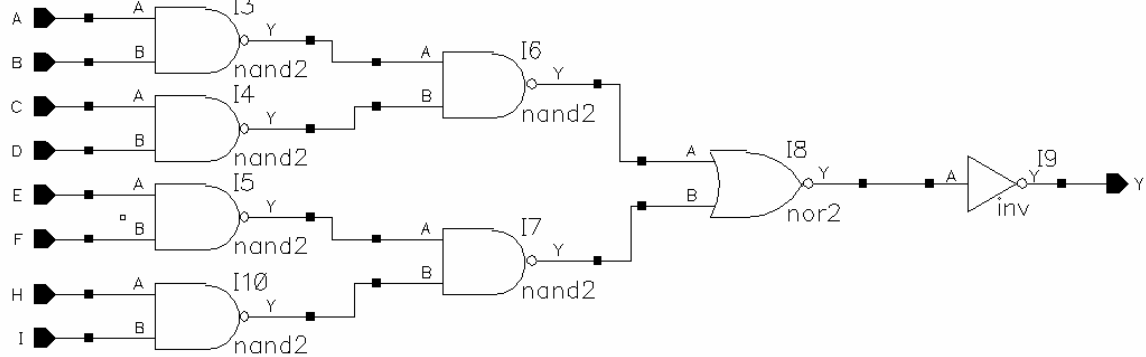


Figure 14: VNORTH.

NAME: \_\_\_\_\_

**Question 2(50pts):**

Design WN and WP for the circuit to meet a total propagation delay of .8ns. Assume that the Cg the inverter is driving is 90fF. Show all work.



There are 4 logic levels so the delay should be .8ns/4 or .2ns per level.

Using the excel sheet:

CELL	LL	WN Load (cm)	WP Load (cm)	Cint F	Cg or Cin of load F	Cg+Cint F	τ <sub>phl</sub> s	τ <sub>plh</sub> s	A Ω	S	NSN	N	M	R	WN cm	WP cm
inv	1			0.00E+00	9.0000E-14	9.0000E-14	2.00E-10	2.00E-10	1.18E+04	1.0000	1	1	1	1.780	3.79E-04	6.75E-04
nor2	2	3.79E-04	6.75E-04	0.00E+00	1.7680E-14	1.7680E-14	2.00E-10	2.00E-10	1.18E+04	1.0000	1	2	3	3.560	2.23E-04	7.95E-04
nand2	3	2.23E-04	7.95E-04	0.00E+00	1.7089E-14	1.7089E-14	2.00E-10	2.00E-10	1.18E+04	1.0000	2	1	3	2.0890	3.07E-04	2.74E-04
nand2	4	3.07E-04	2.74E-04	0.00E+00	1.9496E-14	1.9496E-14	2.00E-10	2.00E-10	1.18E+04	1.0000	2	1	3	2.1000	3.54E-04	3.54E-04

We see that the Wn, WP values increase for the nand2. This means the gates are going too fast. This probably means the nor2 is going to fast. We can take .1 away from the inverter and give it to the other gates:

CELL	LL	WN Load (cm)	WP Load (cm)	Cint F	Cg or Cin of load F	Cg+Cint F	τ <sub>phl</sub> s	τ <sub>plh</sub> s	A Ω	S	NSN	N	M	R	WN cm	WP cm
inv	1			0.00E+00	9.0000E-14	9.0000E-14	1.00E-10	1.00E-10	1.23E+04	1.0000	1	1	1	1.805	9.59E-04	1.73E-03
nor2	2	9.59E-04	1.73E-03	0.00E+00	4.5156E-14	4.5156E-14	2.33E-10	2.33E-10	1.16E+04	1.0000	1	2	3	3.543	3.23E-04	1.15E-03
nand2	3	3.23E-04	1.15E-03	0.00E+00	2.4657E-14	2.4657E-14	2.33E-10	2.33E-10	1.16E+04	1.0000	2	1	3	2.0886	3.03E-04	2.68E-04
nand2	4	3.03E-04	2.68E-04	0.00E+00	1.9182E-14	1.9182E-14	2.33E-10	2.33E-10	1.16E+04	1.0000	2	1	3	2.1000	2.57E-04	2.57E-04

The testbench to design for the worst case

Input	State
A	At least one of A or B Low
B	At least one of A or B Low
C	High
D	Toggle
E	At least one of E or F Low
F	At least one of E or F Low
H	At least one of H or I Low
I	At least one of H or I Low

NAME:

**Question 3 (50 PTS):**

You have designed a 2 input NOR Gate to have an average worst-case propagation delay of .2ns. You need to verify this worst-case average propagation delay in a real silicon part. Design a circuit that will allow you to measure this delay with an oscilloscope that can read 100MHz frequency signals or less. Make sure to draw the circuit!

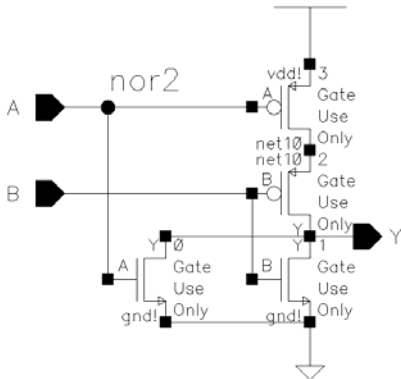


Figure 15: Schematic of an NOR2.

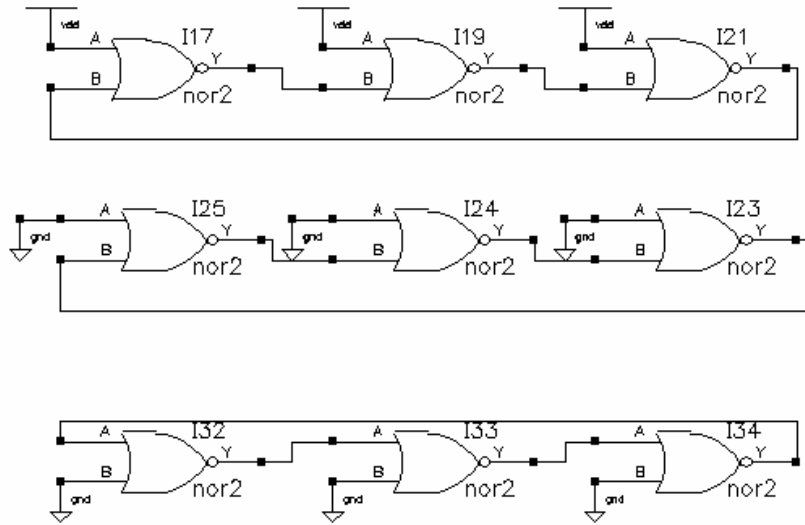
For the worst case for a NOR2 it is Pin A that needs to toggle as this pin will maximize the number of drain/source capacitances that need to be charged and discharged. The number of stages is:

$$N := \frac{1}{2 \cdot 2 \cdot 10^{-9} \cdot 100 \times 10^6} \quad N = 25$$

The circuit would have 25 stages of the out pin Y being fed into pin A of the next stage while all pin B's are held low. The output of the 25 stage would be fed into the input pin a of the first stage.

Which ring oscillator below oscillates the slowest?

NAME:



The Top circuit does not oscillate as one pin is tied high. This will make the output of any nor gate always low. The bottom circuit has its pin A toggling, which will cause the maximum number of capacitances to charge and discharge, thus will make the circuit oscillate the slowest.

**Question 4 (50 PTS):**

Draw a cross section cut from A to B. Label all the capacitance not shorted to ground.

