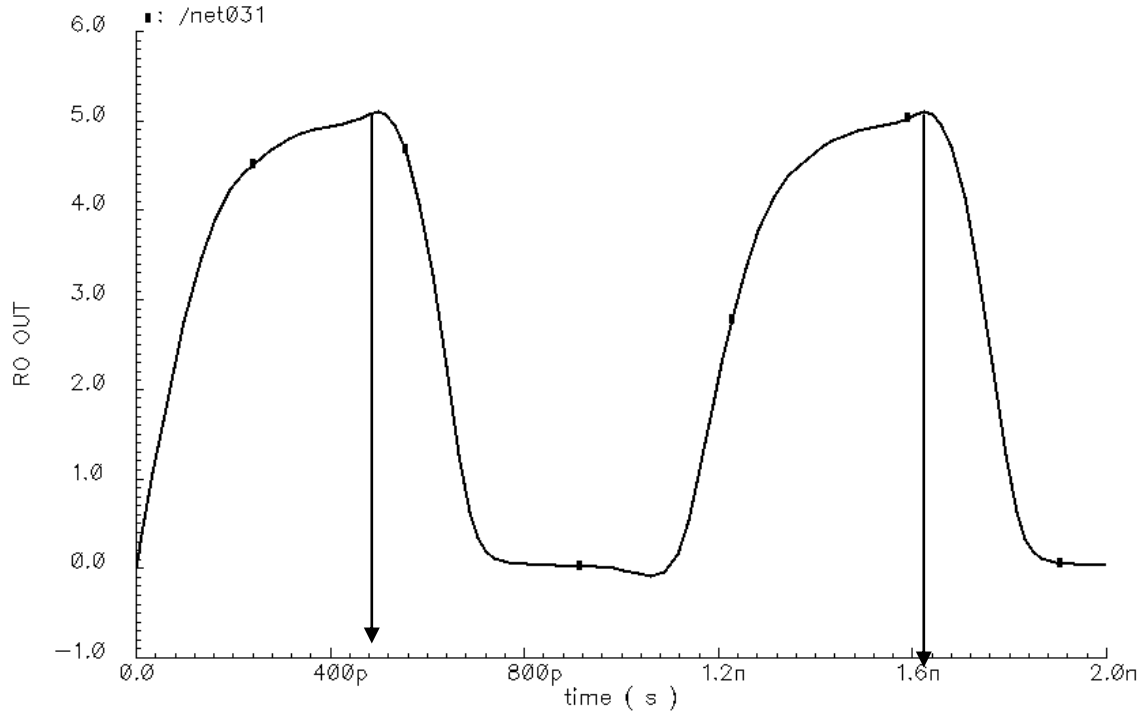


Question 1(25pts):

You have just measured the output of a 15-stage ring oscillator. What is the average propagation delay of this circuit? (10PTS)

ami06 nmos_tb schematic : Feb 28 13:17:55 2006

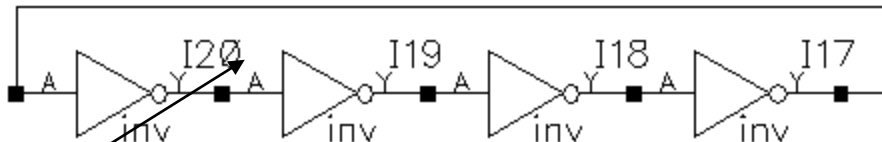
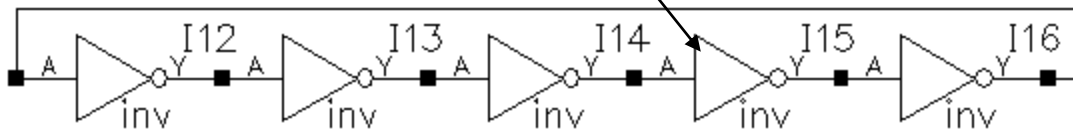
Transient Response



$$T = 1.62\text{ns} - 0.440\text{ns} = 1.18\text{ns}$$

$$T_{pave} = T/5 = 0.236\text{ns}$$

Which circuit below oscillates at the highest frequency? (5PTS)(Explain)



Not an RO!

Which circuit below oscillates at the lowest frequency? (5PTS)(Explain)

Question 2(25pts):

Using our process parameters design a CMOS inverter (Driver) to have symmetric propagation delays of .12ns driving a CMOS inverter (Load) with $W_N=7\mu\text{m}$, $W_P=14\mu\text{m}$.
(6pts)

$$C_g = 12\text{fF} + 23.5\text{fF} = 35.5\text{fF} \text{ (From Chart)}$$

$$W_N = 2.75\mu\text{m}, W_P = 2 \times 2.75\mu\text{m} = 5.50\mu\text{m} \text{ (From chart)}$$

Using our process parameters design a CMOS inverter (Driver) to have symmetric propagation delays of .1ns driving a CMOS inverter (Load) with $W_N=10\mu\text{m}$, $W_P=20\mu\text{m}$.
(6pts)

$$C_g = 17\text{fF} + 34\text{fF} = 51\text{fF}$$

$$W_n = 5.5\mu\text{m}, W_P = 2 \times W_n = 11\mu\text{m}$$

Using our process parameters design a CMOS inverter (Driver) to have symmetric propagation delays of .90 ns driving a CMOS inverter (Load) with $W_N=10\mu\text{m}$, $W_P=20\mu\text{m}$.
(6pts)

You could try to extend the graph, but it will be hard as the curves are exponentially rising as delay gets smaller. .09ns is very close to .1ns, so we could try to just use the values from the previous problem. We could also use the excel model:

WN Load (cm)	WP Load (cm)	Cg or Cin of load F	τ_{phl} s	τ_{plh} s	A Ω	S	NSN	NSP	N	M	R	WN cm	WP cm	
1.00E-03	2.00E-03	5.0346E-14	9.00E-11	9.00E-11	1.24E+04	1.0000		1	1	1	1	1.808	6.41E-04	1.16E-03

Calculate the power of the last inverter you designed if the frequency was 400MHz and the activity factor (α) was equal to one (7pts)

$$V_{DD} = 5\text{V}, f = 400\text{MHz}, C_g \text{ of Driver } (W_n = 6.41\mu\text{m}, W_p = 11.6\mu\text{m}) = 30\text{fF} \text{ (Excel)}$$

$$C_{out} \text{ of driver } (W_n = 6.41\mu\text{m}, W_p = 11.6\mu\text{m}) = 12\text{fF} + 22\text{fF} = 34\text{fF}$$

$$C_{Load} = C_g + C_{out} = 30\text{fF} + 34\text{fF} = 64\text{fF}$$

$$\text{Assume } \alpha = 1$$

$$\text{Power} = 1 \times 64\text{fF} \times 400\text{MHz} \times 5^2 = 640\mu\text{W}.$$

Question 3(50PTS):

- 1) Using our process parameters design a CMOS inverter to have symmetric propagation delays of .09ns driving an inverter with a $W_N=15\mu\text{m}$ and $W_P=30\mu\text{m}$:
 - 2) In Spice, adjust W_n or W_p to get within 10% of the above specification.
 - 3) Attach a screen grab of your circuit, and waveform-see the appendix of the tutorial to see how to do this.
- Calculate the transient power the circuit will use and compare it to the measured power from spice.

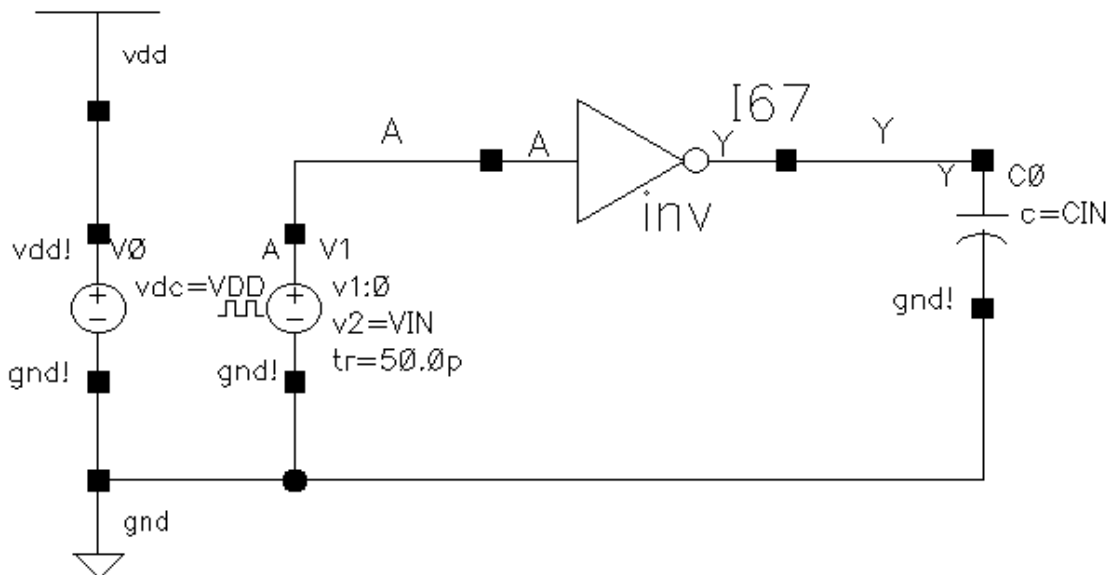
Note:

A common problem that people encounter on this set, is that no matter what W_N or W_P you enter it does not change the spice results. This is usually because you are still reading the analog_extracted view from when you did the tutorial. In the library manager delete the analog_extracted view. If you are trying to use variables and get an error about no variables present fix it the same way delete the analog_extracted view.

Also set the rise and fall times to 50ps.

Hand Calculations for excel model:

WN Load (cm)	WP Load (cm)	Cg or Cin of load F	tphi s	tphi s	A Ω	S	NSN	NSP	N	M	R	WN cm	WP cm
1.50E-03	3.00E-03	7.5520E-14	9.00E-11	9.00E-11	1.24E+04	1.0000	1	1	1	1	1.808	9.47E-04	1.71E-03



Editing Design Variables – Virtuoso® Analog Design Environment

OK Cancel Apply Apply & Run Simulation Help

Selected Variable

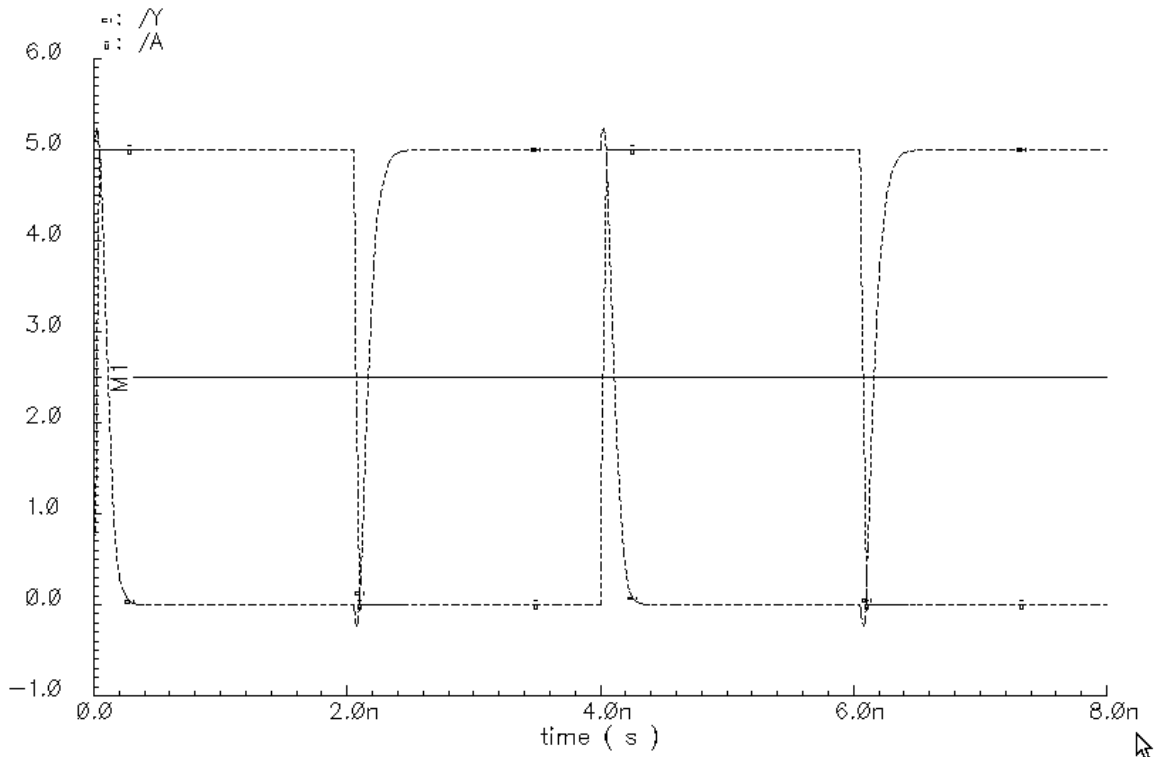
Name: WP
 Value (Expr): 17.1u

Add Delete Change Next Clear Find

Cellview Variables Copy From Copy To

Table of Design Variables

#	Name	Value
1	WP	17.1u
2	WN	9.47u
3	VIN	5
4	VDD	5
5	LP	600n
6	LN	600n
7	CIN	75f

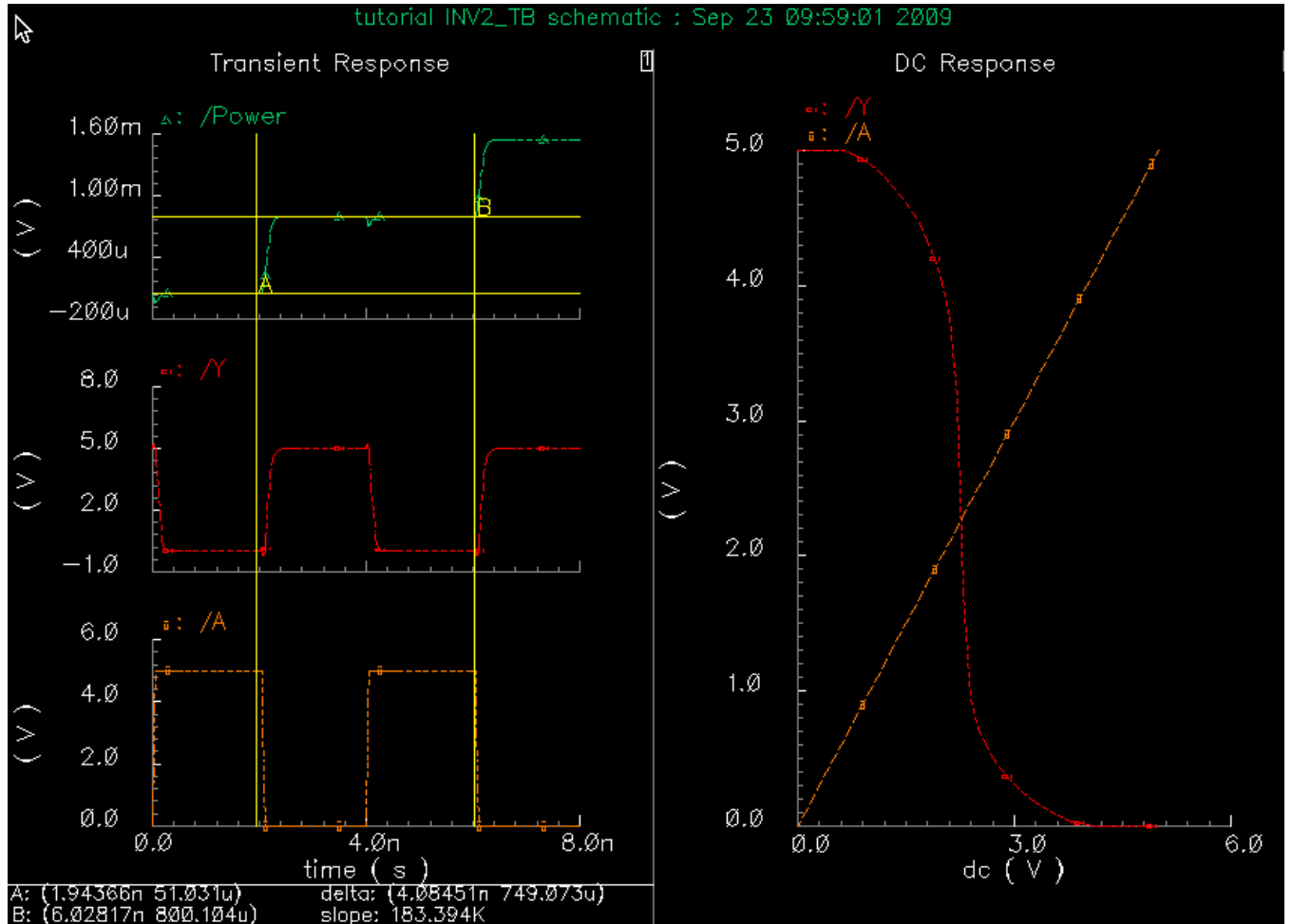


Curve table:

	Y value	Curve2	Curve1
M1	2.5	112.8407523p	25p
		2.1649478738n	2.075n
		4.1127632436n	4.025n
		6.1649696486n	6.075n

	Time Vin crosses Vdd/2 (ps)	Time Vout crosses Vdd/2 (ps)	Delay Measured (ps)	Delay Spec (ps)	Error (%)
tphl	25	112.8	87.8	90	-2.44444
tplh	2075	2165	90	90	0

Since we are within 10% the Wp/Wn values are 17.1/9.47.



Question 4 (25PTS):

1. Calculate V_{TH} for the inverter you designed above.

$$L_N := .6 \cdot 10^{-4} \text{ cm} \quad L_P := L_N$$

$$K_{NP} := 46.3 \cdot 10^{-6} \frac{\text{A}}{\text{V}^2} \quad K_{PP} := 30 \cdot 10^{-6} \frac{\text{A}}{\text{V}^2}$$

$$V_{TN} := .6\text{V} \quad V_{TP} := -.82\text{V} \quad V_{DD} := 5\text{V}$$

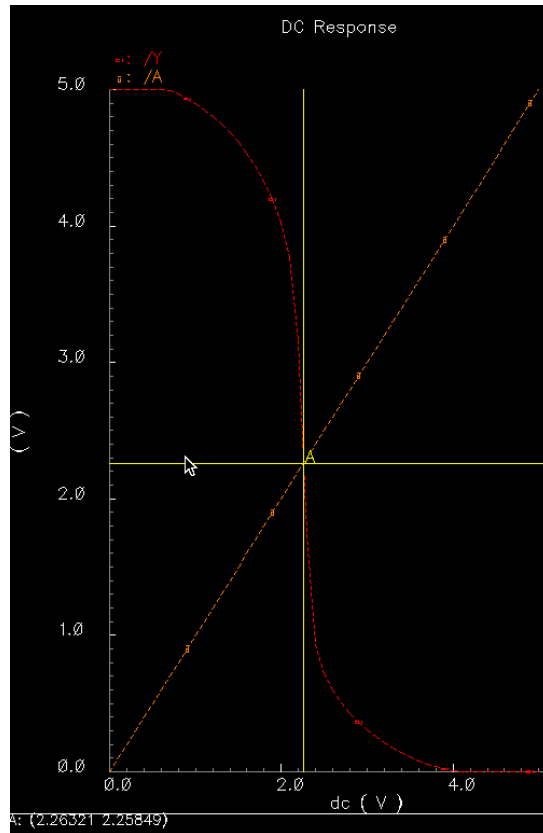
$$W_N := 9.47 \cdot 10^{-4} \text{ cm} \quad W_P := 17.1 \cdot 10^{-4} \text{ cm}$$

$$K_R := \frac{K_{NP} \cdot W_N}{K_{PP} \cdot W_P} \quad K_R = 854.70 \times 10^{-3}$$

$$V_{INVTH} := \frac{V_{TN} + \sqrt{\frac{1}{K_R}} \cdot (V_{DD} + V_{TP})}{1 + \sqrt{\frac{1}{K_R}}}$$

$$V_{INVTH} = 2.46 \times 10^0 \text{ V}$$

2. In spice, measure V_{TH} . Attach a screen grab of your circuit, and waveform-see the appendix of the tutorial to see how to do this.



V_{th} measured is 2.26V

3. What would happen to V_{TH} if:
- W_n was doubled? Down
 - W_p was doubled? Up
 - Both W_n and W_p were doubled? Stay Mostly the same
 - L_n was doubled? Up
 - L_p was doubled? Down
 - Both L_n and L_p were doubled? Stay Mostly the same
 - Everything was doubled? Stay Mostly the same

Question 5 (75PTS):

Identify the specification of your project. Speed, power, logic function and area need to be reported and justified.