

Question 1(25pts):

Draw a stick diagram of you project circuit shown how you will distribute the power and the clock. Do not show the details of each cell, just how you would connect power, gnd, ck, reset, and route the major signals.

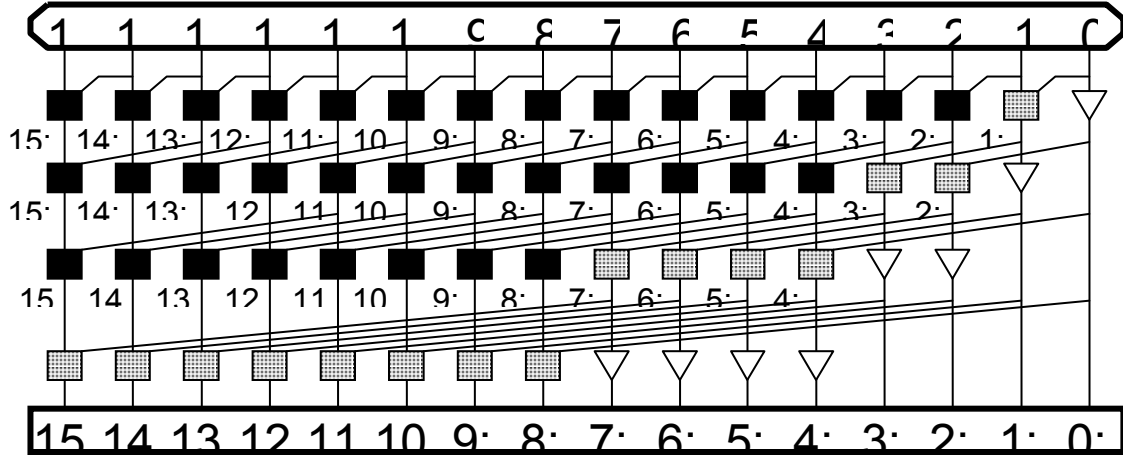
Question 2(25pts):

Design a chain of inverters to drive a clock signal with minimum delay. The propagation delays must be symmetric. The load that this driver has to drive is comprised of 30000 DFFs, which have a C_{in} each of 20fF.

What is the power dissipation of this driver?

Question 3 (25PTS):

Please estimate the wiring capacitance of the two longest wires in the following schematic. Assume that the capacitance is 2fF per micron on length. Use typical cell heights and widths (based on your own project).



Question 4 (125):

Document that you have verified the layout of the group's Project. Show DRC, Extraction, LVS reports for all cells. This must be done in a professional manner.

NA