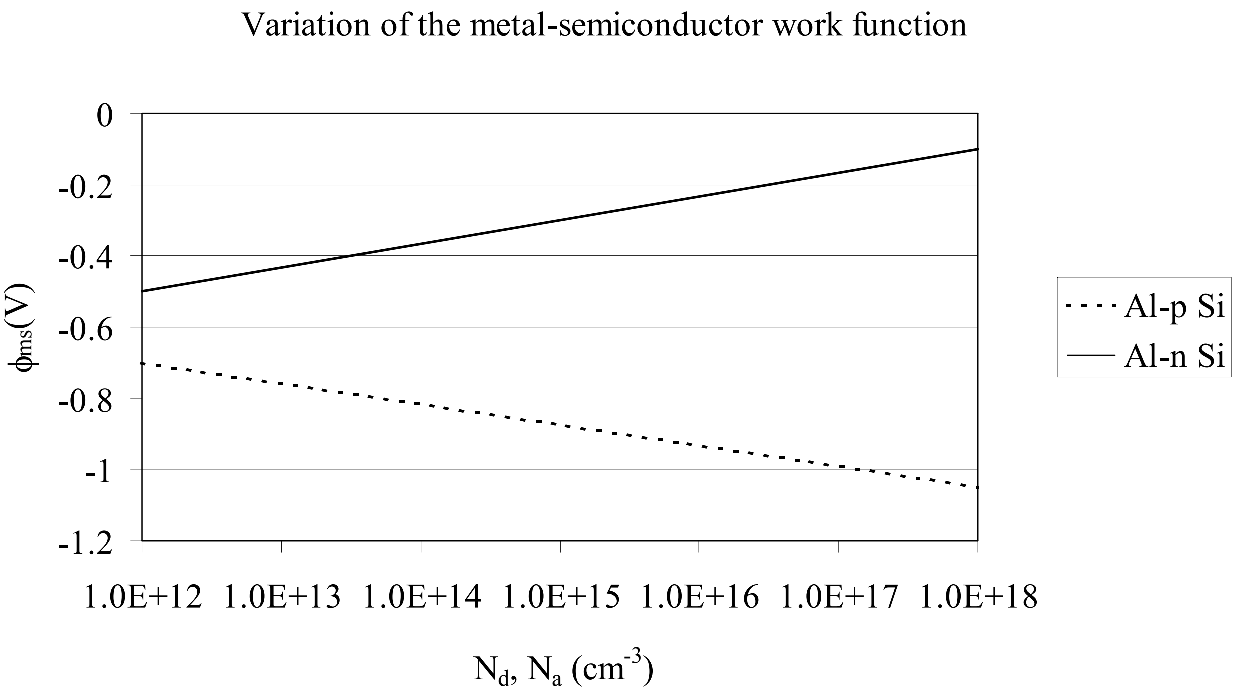
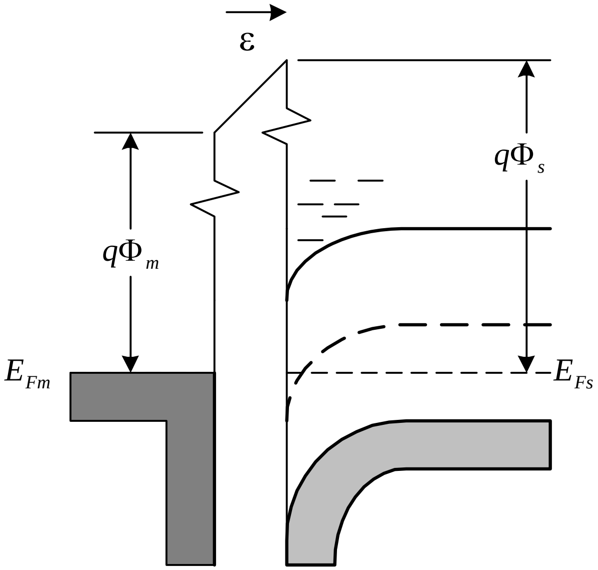
Effects of Real Surfaces

- Work Function Difference:
  - Doping level changes ($\phi_{ms} = \phi_m - \phi_s$)
  - Always negative
  - To take into account band bends down (can even cause a channel to exist).
- Interface Charge:
  - Q_m (Mobile ionic), Q_{ot} (Oxide trapped), Q_f (Oxide fixed), Q_{it} (Interface trap)

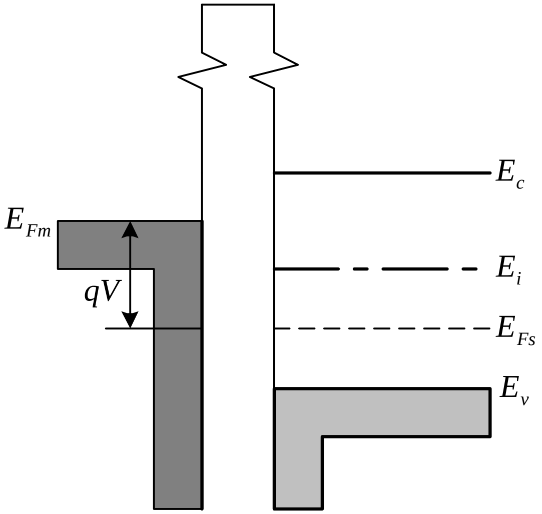
Work Function Difference



Effects of Real Surfaces

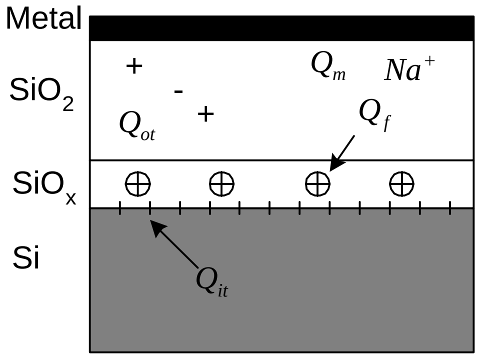


(a) Equilibrium
V=0

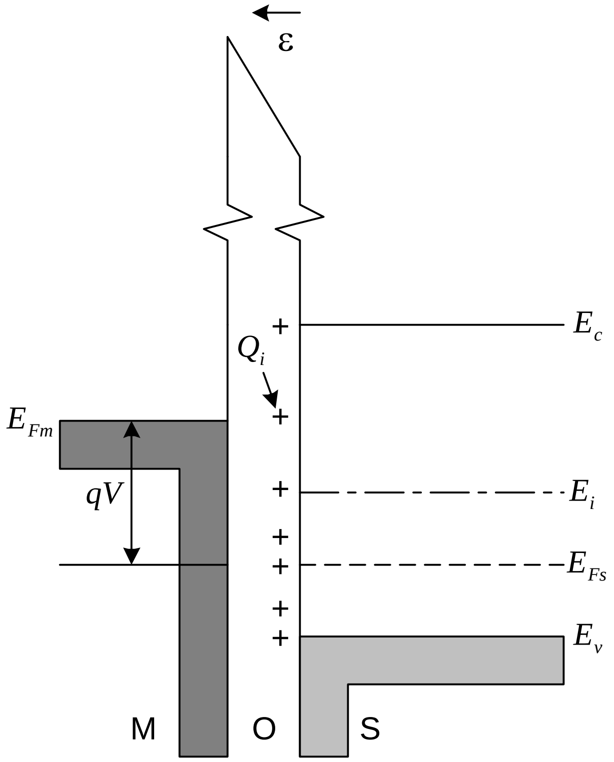


(b) Flat band
$V = V_{FB} = \Phi_{ms}$

Effects of Real Surfaces



Q_m	Mobile inoic charge
Q_{ot}	Oxide trapped charge
Q_f	Oxide fixed charge
Q_{it}	Interface trap charge



$$V_{FB} = \varphi_{ms} - \frac{Q_i}{C_i}$$

$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Real Surfaces

- Interface Charge:
  - Q_m (Mobile ionic) Sodium atoms move around under electric field
  - Q_{ot} (Oxide trapped) Imperfections in SiO_2 cause charge to be trapped
  - Q_f (Oxide fixed) Ionic silicon left over from oxidation process.
  - Q_{it} (Interface trap) Charge due to abrupt interface of SiO_2 and Si.

Threshold Voltage (Al Gate)

$$\mathrm{V_T} = \varphi_{\mathrm{ms}} - \frac{\mathrm{Q_i}}{\mathrm{C_i}} - \frac{\mathrm{Q_d}}{\mathrm{C_i}} + 2\varphi_{\mathrm{F}}(NMOS) \qquad \varphi_{\mathrm{F}} = .0259\ln\left(\frac{N_a}{n_i}\right)(NMOS)$$

$$\mathrm{V_T} = \varphi_{\mathrm{ms}} - \frac{\mathrm{Q_i}}{\mathrm{C_i}} - \frac{\mathrm{Q_d}}{\mathrm{C_i}} - 2\varphi_{\mathrm{F}}(PMOS) \qquad \varphi_F = .0259\ln\left(\frac{N_d}{n_i}\right)(PMOS)$$

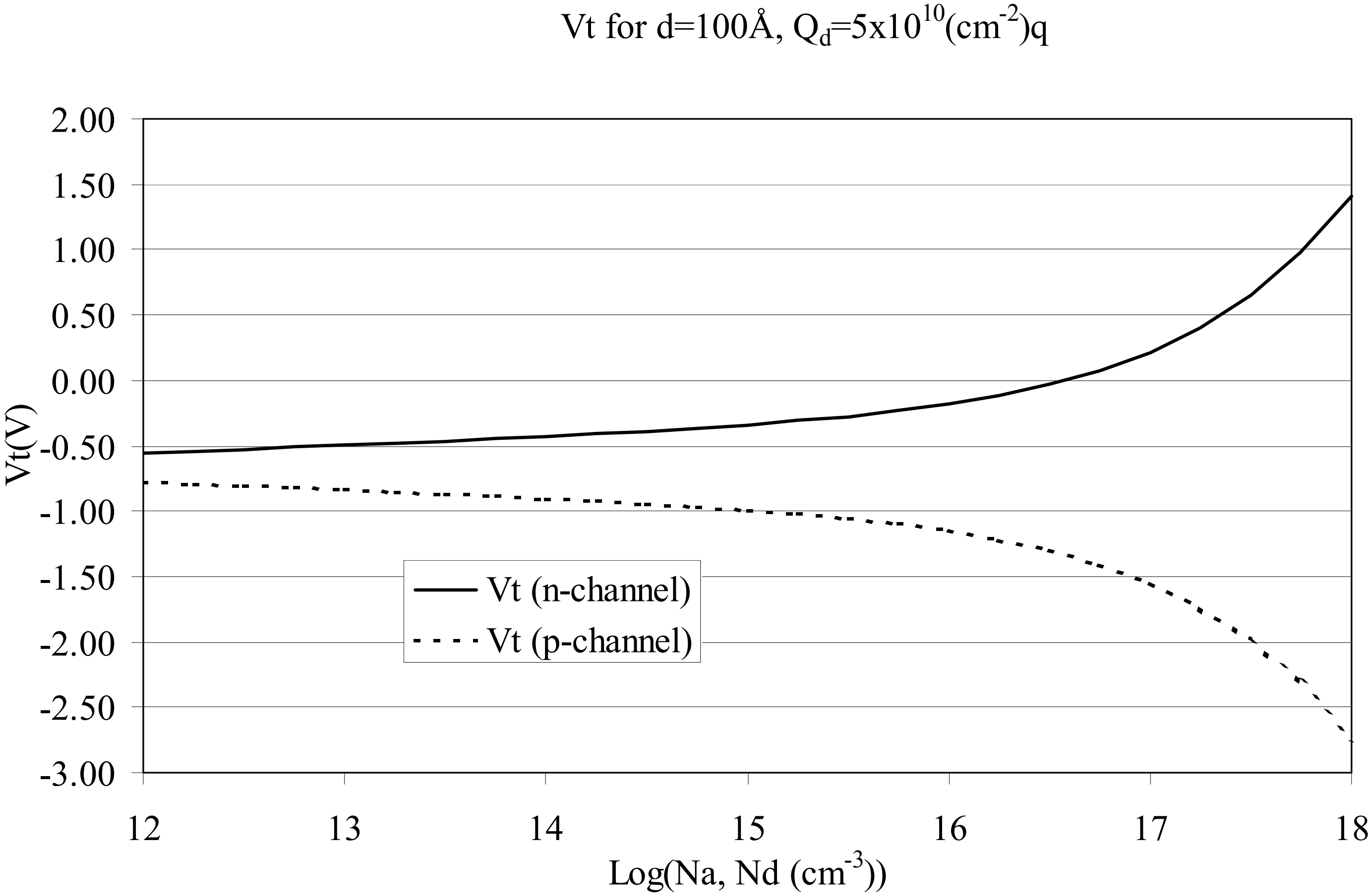
φ_{ms}Get from chart (both n and p channel)

$$\mathrm{C_i} = \frac{(3.9)(8.885\times10^{-14}\ \mathrm{F/cm})}{d(cm)} \text{ (both n and p channel)}$$

$\mathrm{Q_i}$ = Given to you by process engineer.

$$\mathrm{Q_d}(nmos) = -2(\varepsilon_s q N_a \varphi_F)^{\frac{1}{2}},\ \mathrm{Q_d}(pmos) = 2(\varepsilon_s q N_d \varphi_F)^{\frac{1}{2}},$$

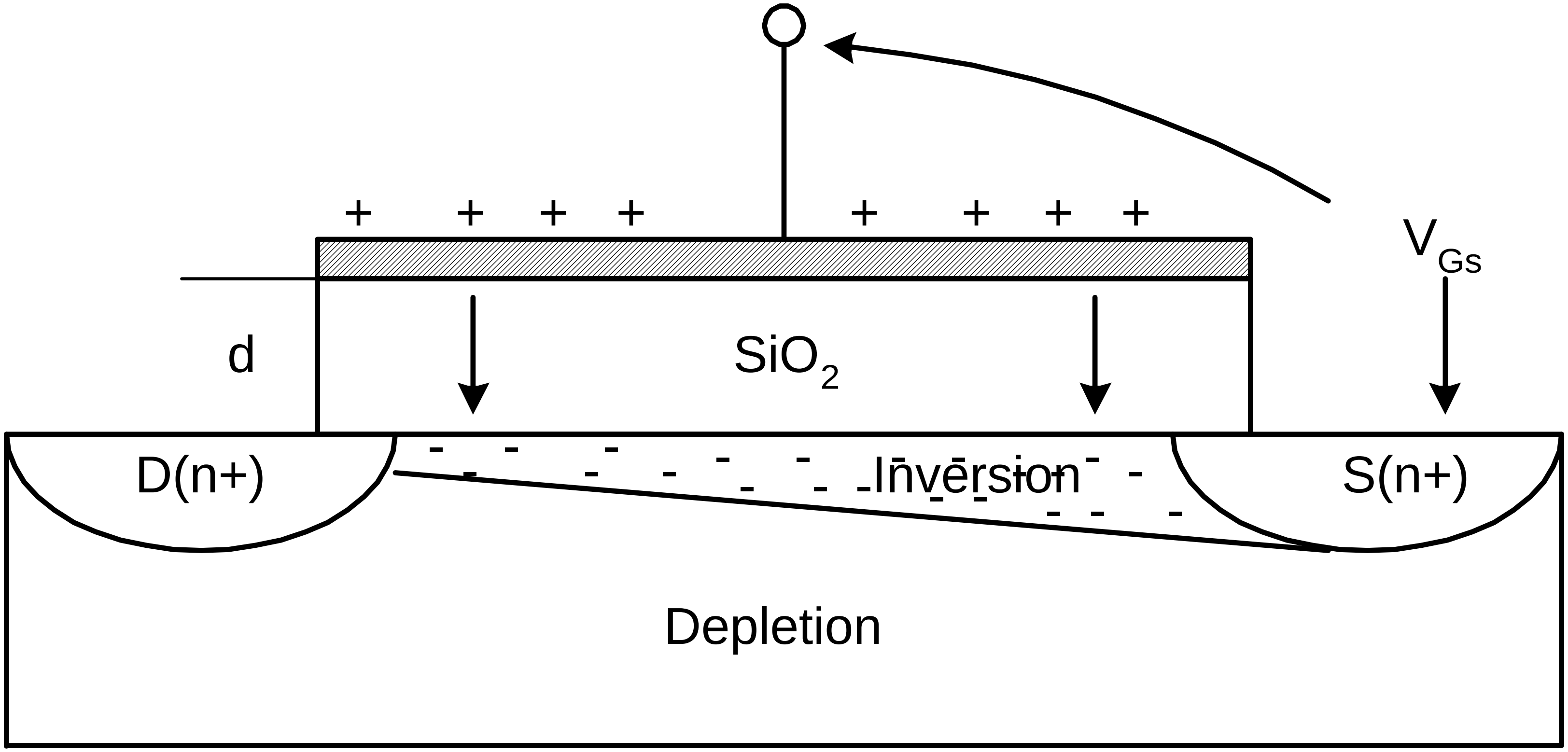
Threshold Voltage



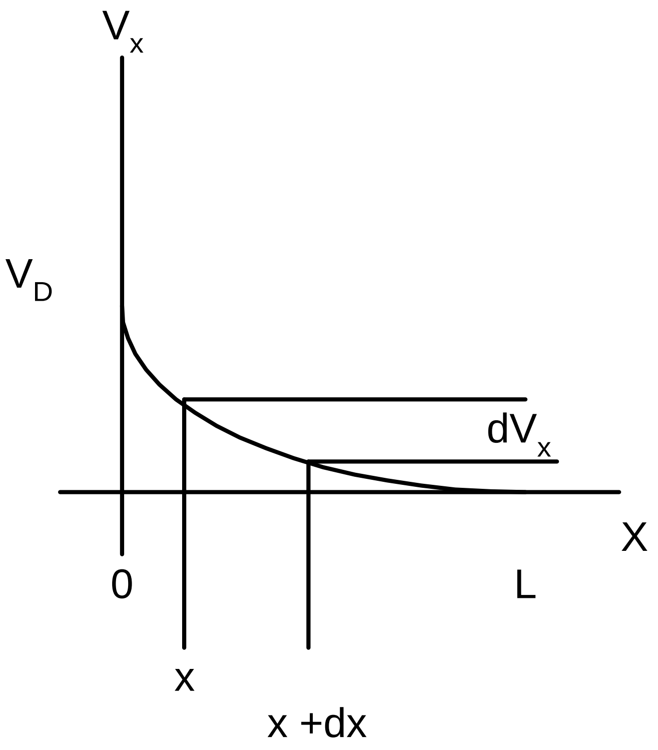
Examples

- Solve Example 6-1 except Na=1×10^{17}cm^{-3}
- Solve Example 6-2 except use a 50Å SiO_2 layer.

The MOS Field-Effect Transistor



The MOS Field-Effect Transistor



The MOS Field-Effect Transistor

Linear Region :

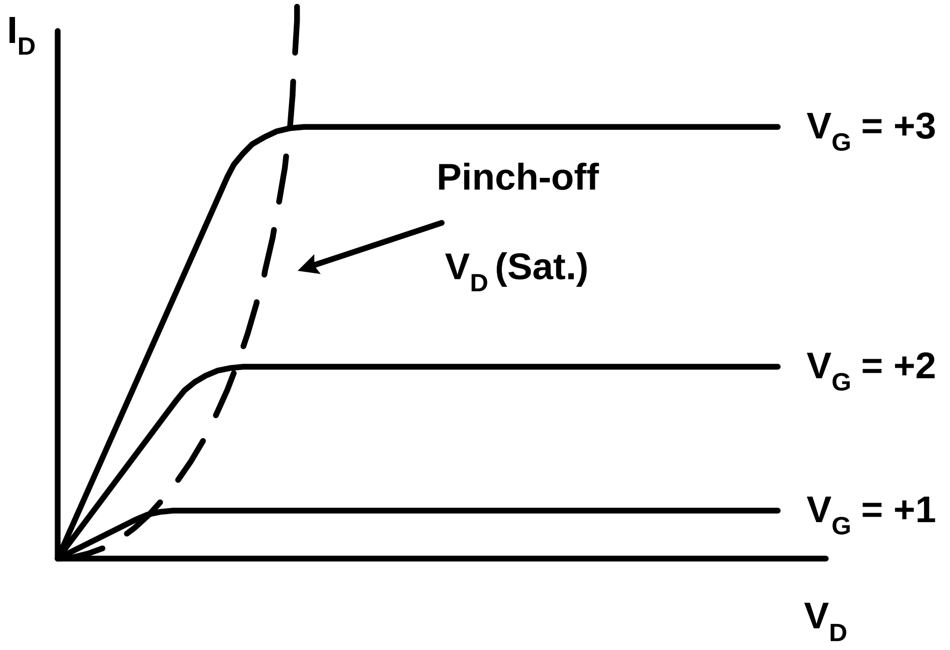
$$g_m = \frac{Z}{L}\mu_n C_i V_D$$

$$I_D = \frac{Z}{L}\mu_n C_i\left[\left(V_G - V_T\right)V_D - \frac{1}{2}V_D{}^2\right]$$

Saturation Region $(V_{DSAT} = V_G - V_T)$:

$$g_{m(sat)} = \frac{Z}{L}\mu_n C_i V_{DSAT}$$

$$I_{D(sat)} = \frac{Z}{L}\mu_n C_i V_{DSAT}{}^2$$



Control of Threshold Voltage

- Silicon gate technology
  - Φ_{ms} is reduce by using poly-silicon as the gate
    - Poly-silicon must be heavily doped
    - Φ_{ms} is now just the difference in Fermi levels of the two silicon regions.
    - Poly-silicon is also more process friendly (It can withstand higher temperatures than Al)

Control of Threshold Voltage

- Control of C_i
  - – We would like a small V_T under the gate but elsewhere we would like a large V_T to prevent channels from forming between transistors.
  - – Smaller C_i, leads to a smaller threshold.

Control of Threshold Voltage

- Ion Implantation
  - B ions can be implanted in a two dimensional sheet just below the oxide layer. These ions are negatively charged and can be used to offset Q_d. Dose typically 10 seconds.

$$V_{T(New)} = V_{T(Old)} + \frac{qF_B}{C_i}$$

Control of Threshold Voltage

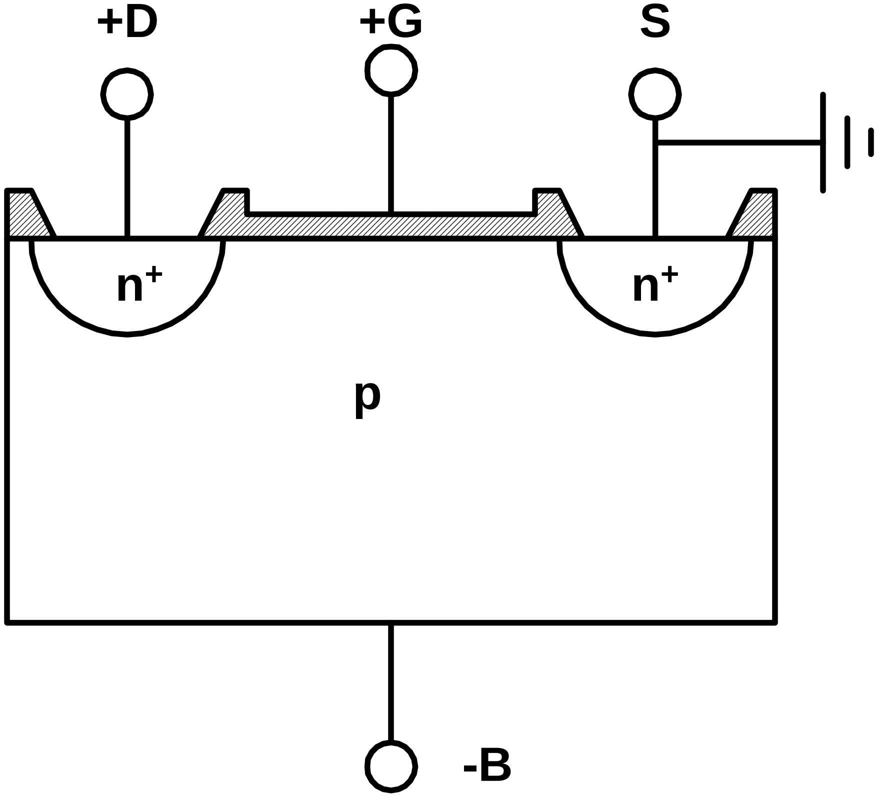
- Control Qi
  - Grow the SiO_2 layer on {100} oriented wafers
    - Less dangling bonds
    - Slower growth rate leads to higher quality layer
    - HCl in oxygen reduces sodium in SiO_2

Substrate Bias Effect

- We add a contact to the body (Normally the source and body are ties together at ground)

$$\Delta V_T = \frac{\sqrt{2\varepsilon_s q N_a}}{C_i}\left[(-V_B)^{\frac{1}{2}}\right](NMOS)$$

$$\Delta V_T = -\frac{\sqrt{2\varepsilon_s q N_d}}{C_i}\left[(V_B)^{\frac{1}{2}}\right](PMOS)$$

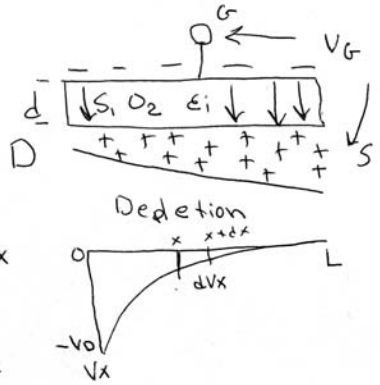


What is “Pinch off”

- For a given V_G, you have a maximum amount of current you can flow through the channel (regardless of V_D).
- When VD=VG-VT the channel is flowing as much current as it can so we call it pinched off (even though current continues to flow).

P-channel

$$Q_P = C_i\left(-V_g + V_T - V_x\right)$$



$$I_D\,dx = \bar{\mu}_p Z\, Q_{p(x)}\, dV_x$$

$$\int_0^L I_d\,dx = \bar{\mu}_p Z C_i \int_{-V_D}^{0} \left(-V_g + V_T - V_x\right) dV_x$$

$$\int_0^L I_d x = \mu_p Z C_i \Big[-V_g V_x + V_T V_x - \frac{V_x^2}{2} \Big]_{-V_D}^{0}$$

$$I_d L = \mu_p Z C_i \left(0 - \left(-V_g V_x + V_T V_x - \frac{V_x^2}{2}\right)\right)$$ Let $V_x = -V_d$

$$I_d = -\frac{\mu_p Z C_i}{L}\left(+V_g V_D - V_T V_D - \frac{V_D^2}{2}\right)$$

$$I_D = -\mu_p \frac{Z}{L} C_i \left((V_g - V_T)V_D - \frac{V_D^2}{2}\right)$$

[redacted]

I_{DSAT} when $V_D \leq V_G - V_T$