EE128 Homework Set 4

If not specified the temperature for all problems is 300K and the substrate is Silicon, with an Oxide of $Si0_2$.

Question 1:

An n+-polysilicon-gate n-channel MOS transistor is made on a p-type Si substrate with $Na=5x10^{15}cm^{-3}$. The SiO2 thickness is 100 Å in the gate region, and the effective interface charge is $Qi=4x10^{10}qC/cm^2$. Assume 300K.

Calculate W_M, V_{FB}, and V_T.

Question 2:

An n-channel MOSFET with a 400Å gate oxide has a V_T that is supposed to be 1Volt after coming back from ion implantation. After measurement, it turns out that V_T =3Volts. What happened?

Question 3:

Plot ID vs. VD (Excel like program) for several values of VG for the following p-MOS transistor.

Gate:n+poly Si, Nd=$10^{16}cm^{-3}$, Qi=$5x10^{10}qC/cm^2$, tox=$.01x10^{-4}$cm, $\mu p=200cm^2/V\text{-}s$, and Z=10L. Assume ID is constant after pinch off.

Question 4:

A typical figure of merit for high frequency operation is $f_c=g_m/2\pi C_G LZ$ (cut off frequency), where the gate capacitance is Ci over much of the voltage range. Express f_c above pinch-off in terms of material parameters and device dimensions, and calculate fc for the MOSFET in problem 3, with L=1μm.

Question 5:

A given MOSFET has n+(Nd=$10^{20}$$cm^{-3}$) S/D contacts separated by 1mm (L=1x10^{-4}cm). The substrate doping is Na=$10^{16}$$cm^{-3}$. Assume that the source and body are grounded. At what VD will the two depletion widths of the two diodes meet?

Question 6:

An n+-polysilicon-gate line is passing over a field oxide region. What thickness of oxide do you need to have a V_T=>10V, if the n-channel parasitic MOS transistor is made on a p-type Si substrate with Na=5x$10^{15}$$cm^{-3}$, and the effective interface charge is Qi=4x$10^{10}$$qC/cm^2$.

Question 7:

The figure below shows the measured CV data of a MIS capacitor on p-type <100> silicon substrate with an aluminum gate (ϕ_{ms}=-.6ev-$U_T$xln(NA/ni)) (The Insulator is $Si0_2$.) Extract d, (tox) NA, VT, and fixed oxide charge. (Room temperature conditions apply.) Hint, you do not have to scale the measured data by the area.

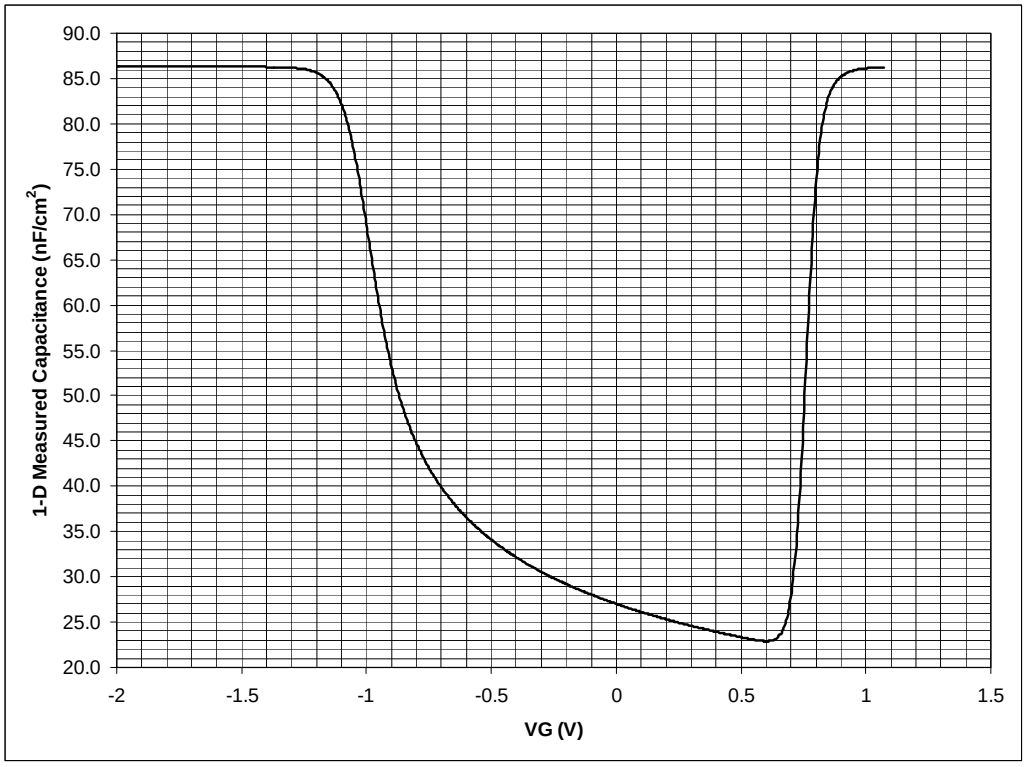

Figure 1: Measured 1-D CV plot of MIS capacitor.

Question 8:

Estimate VT from the following graph (V_{DS}=V_{GS}):