

EE128 Homework Set 3

Question 1:

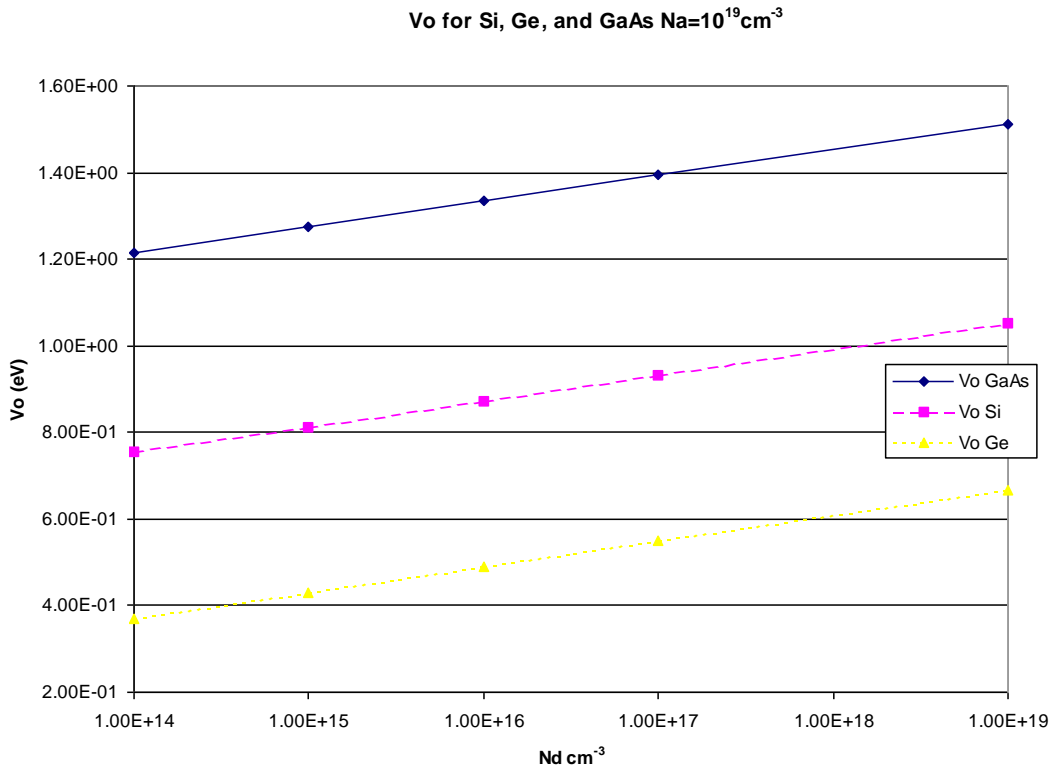
An abrupt Si p-n junction has the following properties at 300K:

p side	n side
$N_a=10^{17}\text{cm}^{-3}$	$N_d=10^{15}\text{cm}^{-3}$
$\tau_n=.1\times 10^{-6}\text{s}$	$\tau_p=10\times 10^{-6}\text{s}$
$\mu_p=400\text{cm}^2/\text{Vs}$	$\mu_n=1200\text{cm}^2/\text{Vs}$
$\mu_n=650\text{cm}^2/\text{Vs}$	$\mu_p=400\text{cm}^2/\text{Vs}$
$A=2\times 10^{-4}\text{cm}^2$	$A=2\times 10^{-4}\text{cm}^2$

- Calculate the Fermi level positions at 300K in the n and p regions.
- Draw the equilibrium band diagram for the junction and determine the contact potential V_0 from the diagram.
- Calculate V_0 according to the equation $V_0=kT/q\ln(N_aN_d/n_i^2)$. Compare V_0 to the value determined from your diagram.

Question 2:

On one set of axis, plot V_o versus N_d for three p-n junctions made of GaAs ($n_i=2 \times 10^6 \text{ cm}^{-3}$), Si ($n_i=1.5 \times 10^{10} \text{ cm}^{-3}$) and Ge ($n_i=2.5 \times 10^{13} \text{ cm}^{-3}$), at 300K where $N_a=10^{18} \text{ cm}^{-3}$. Use a log axis for N_d from 10^{14} - 10^{19} cm^{-3} . Shown below is a sample plot.



Question 3:

a) For the diode of question 1, calculate I for -8 volts, 0 volts (TE), and .5 volts.

Question 4:

- For the diode of question 1, calculate x_n and x_p for -8V, 0V(TE), and .5V.
- Calculate the depletion capacitance for the diode in question 1 for -8V, 0V(TE), and .5V.
- For the diode of question 1, calculate the diffusion capacitance for 1 for -8V, 0V(TE), and .5V.

Question 5:

- For the diode in question 1, find the breakdown voltage.
- What is the breakdown mechanism?
- Why?

Question 6:

Using the data from Figure 1, extract the built in voltage and the substrate doping concentration N_A .

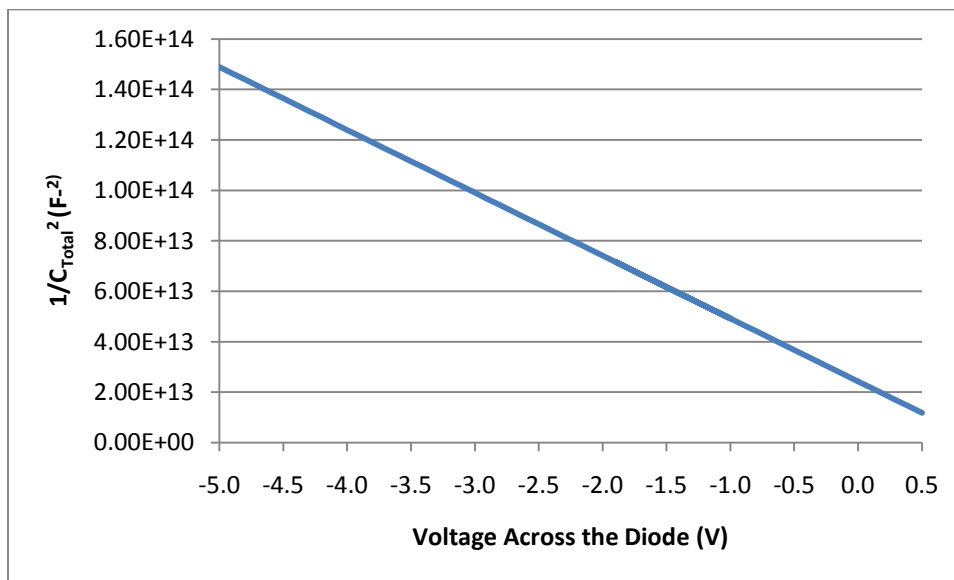


Figure 1: Data from a n+/p diode measured at 300K, with an Area of 1cm^2 .

Question 7:

Using the data from Figure 2, extract the built I_{gen} and the ideality factor.

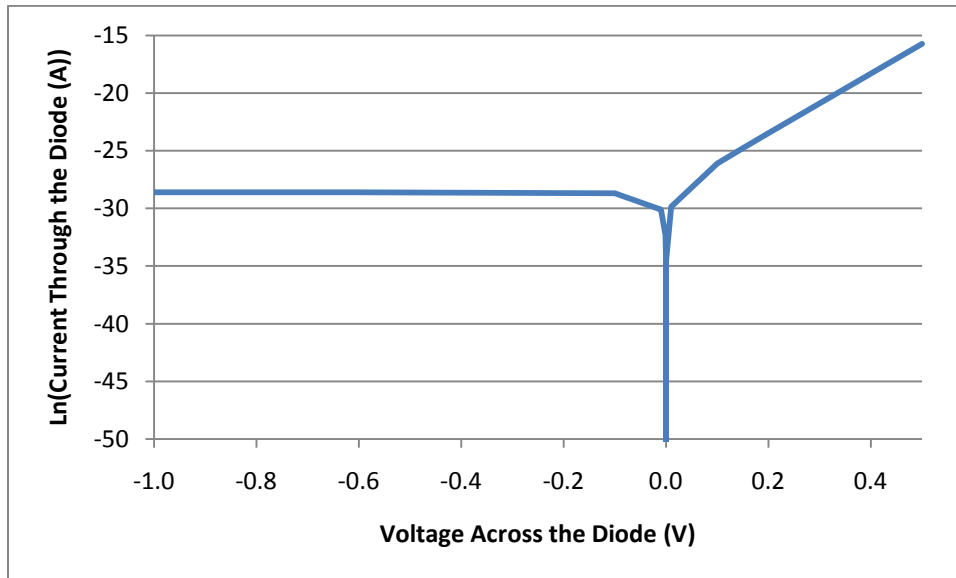


Figure 2: Data from an n+/p diode measured at 300K with an Area of 1cm^2 .

Question 8:

You are in charge of verifying that the break down voltage of your power rectifier diodes (n+/p , silicon, 300K) is greater than 100V. You notice that on the latest batch of wafers the breakdown voltages range from 10 to 15V. What do you think the problem is? What do you think the solution is?