Tutorial

1

SAN JOSE STATE UNIVERSITY

Electrical Engineering Department

Silvaco Tutorial

IC DESIGN GROUP SAN JOSE STATE UNIVERSITY

Athena/ Atlas Tutorial

David W. Parent
Assistant Professor
Electrical Engineering, SJSU
One Washington Square
San Jose, CA 95192-0084
Phone 408.924.3963 • Fax 408.924.2925

Table of Contents

LIST OF FIGURES:

Acknowledgements:

This tutorial is based on the NCSU design kit. For more information, see http://www.ece.ncsu.edu/cadence/CDK.html. This tutorial also follows the design flow used by WPI at http://vlsi.wpi.edu/cadence/.

Chapter
1

Chapter 1: Getting Started with Athena

Athena is a 2-D process simulator. The software can model diffusion, oxidation, implant, etch and deposition processes sue in microelectronic circuit fabrication. This tutorial will show you how to get started creating a process deck from scratch and demonstrate how grid density affects accuracy and speed performance of your simulations.

This chapter will introduce you to the Athena process modeling software by walking you through the fabrication of a Diode by B diffusion into an n-type substrate. It will also cove extracing sheet resistance and junction depths. Examples of how different meshes give different simulation times and accuracies.

Starting the software:

Log in to one of our UNIX stations or remote access the servers by using secure shell to eecadXX..engr.sjsu.edu. (Where XX is a number from 1 to 40)

Start a terminal and enter in the commands as shown in Figure 1.

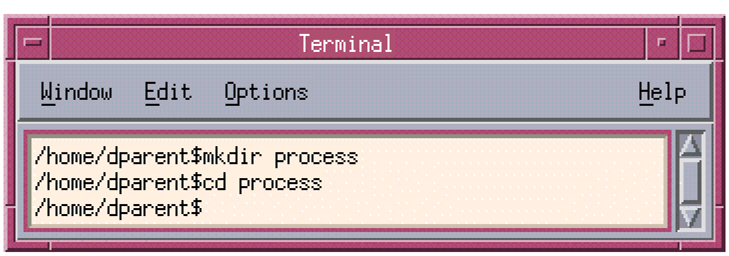

Figure 1: Creating a directory

Start the software by typing deckbuild –an & as shown in Figure 2.

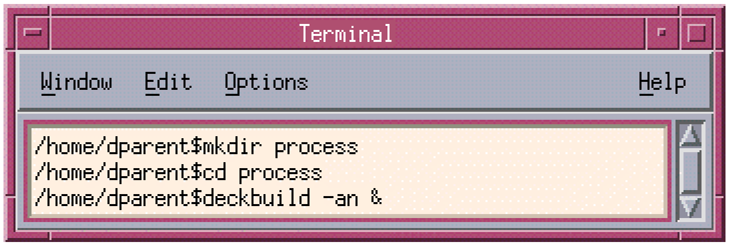

Figure 2: Starting Software

Deckbuild should appear like in Figure 3. This is where you will write the code that will control your simulations. It is an interpreter, not a complier.

We need to define a 2-D space for our simulation. In this case it will be a 10-micron by 10-micron box. **Defining a mesh can be difficult and rarely do I do one from scratch. What I normally do is find a run from the example files and modify it one line at a time until I get the structure I need.**

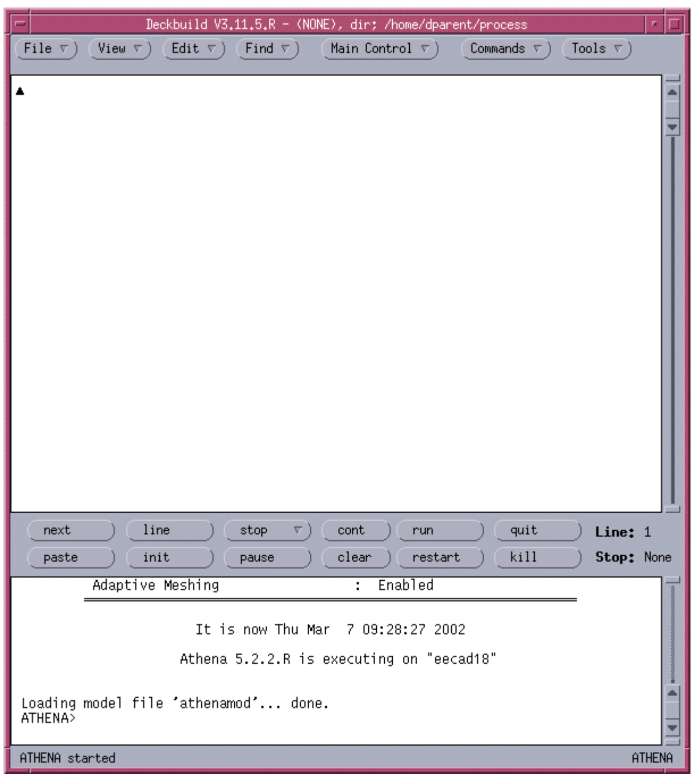

Figure 3: Deckbuild

Right Click on the commands tab in the top of the Deckbuild tool bar. A selection window should appear as in Figure 4. Right click on Mesh define and a pop up like Figure 5should appear.

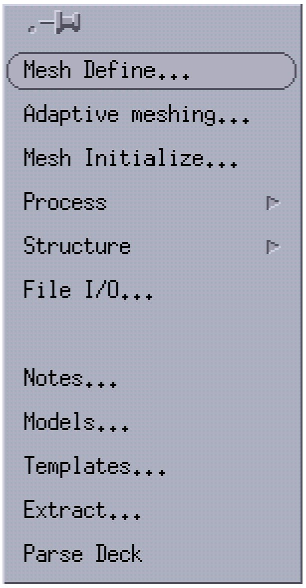

Figure 4: Setting up a 2-D Mesh

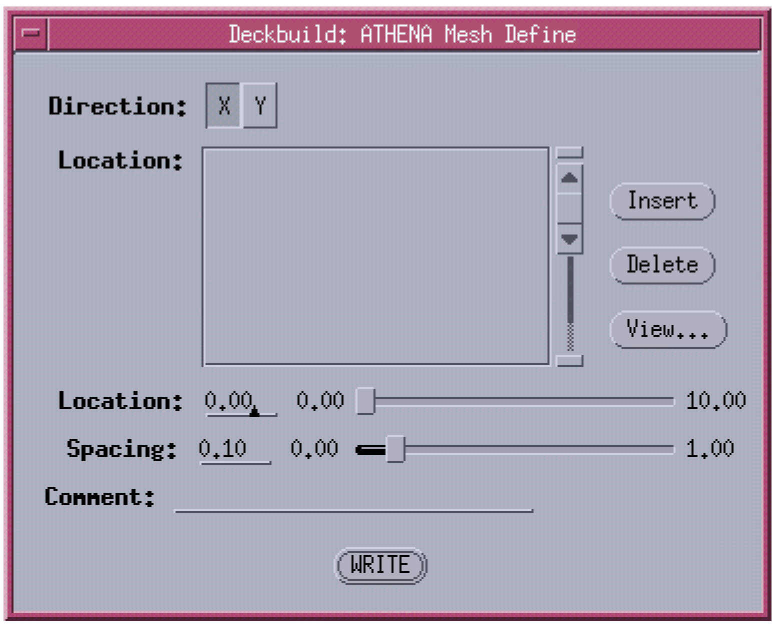

Figure 5: Setting left limit.

Click insert to put in the point already selected. You pop up should look like Figure 6.

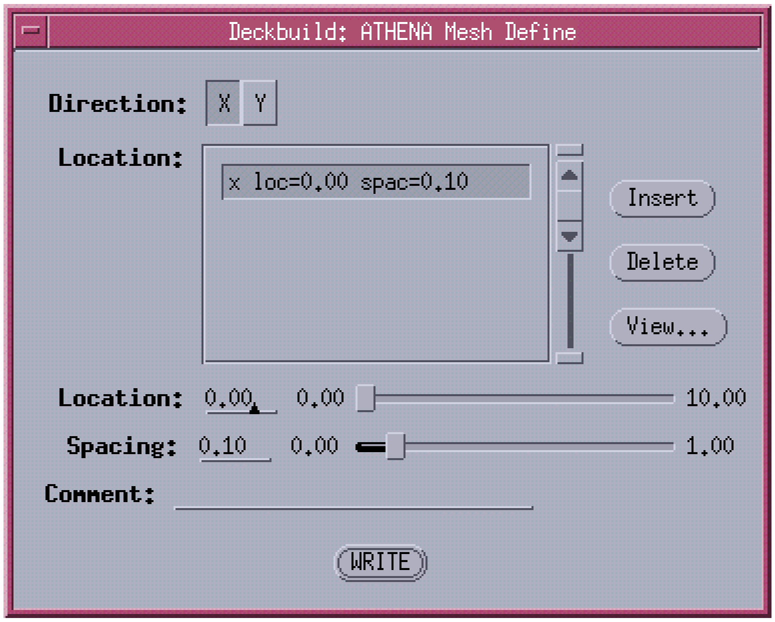

Figure 6: Setting Right Limit.

Enter in a location at 10 microns and click insert like in Figure 7.

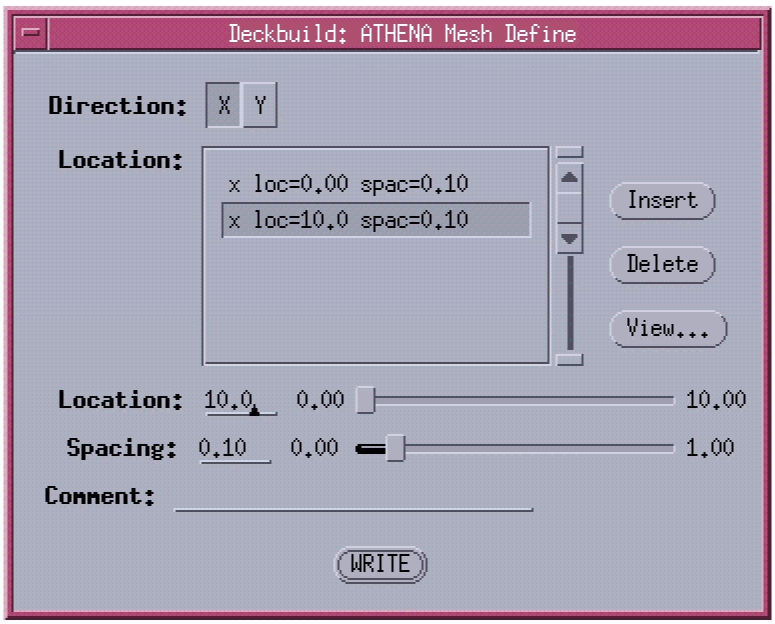

Figure 7: Completed X limits

Repeat the same procedure for the y mesh as in Figure 8, Figure 9, Figure 10.

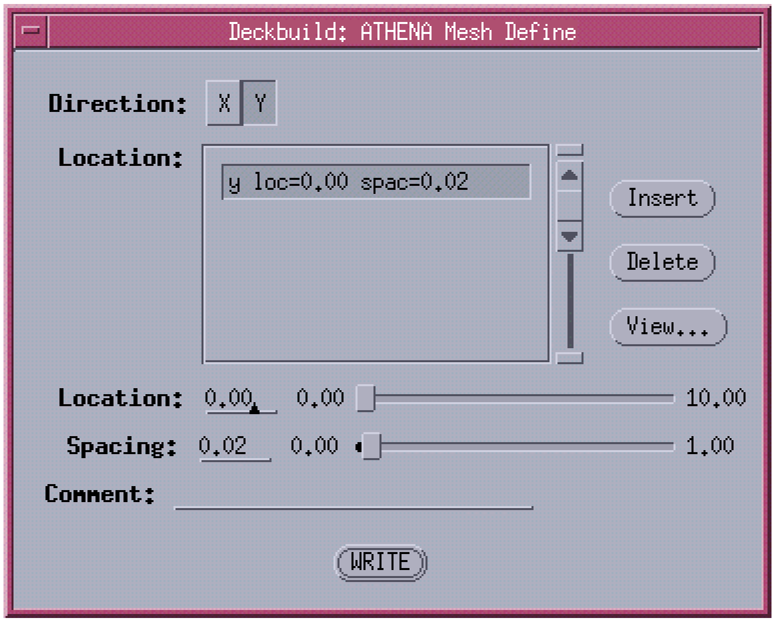

Figure 8: Setting top limit.

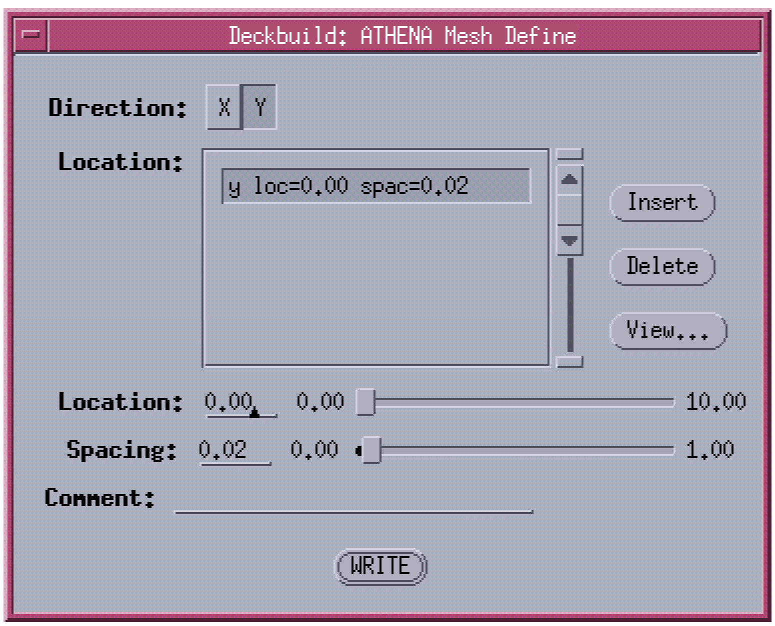

Figure 9: Setting lower limit.

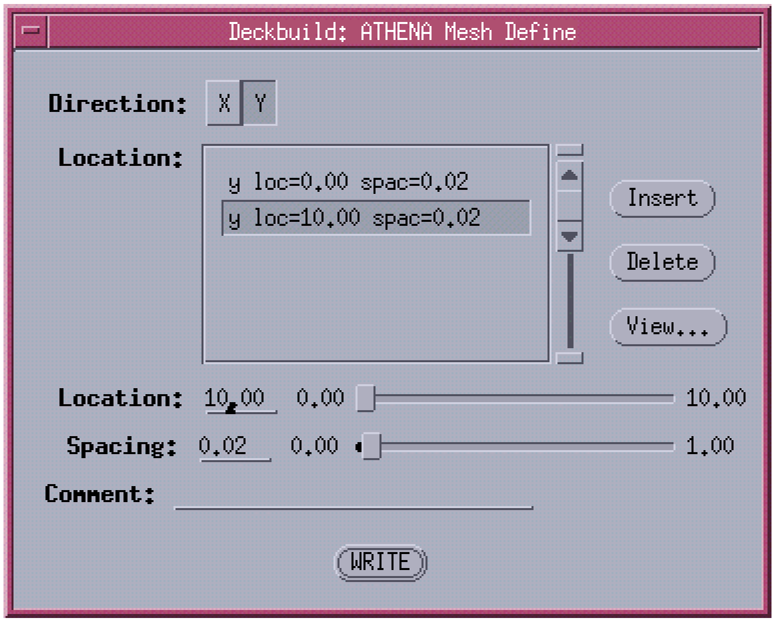

Figure 10: Completed Y limits.

Click the write button in the pop up of Figure 10. You run deck should look like Figure 11.

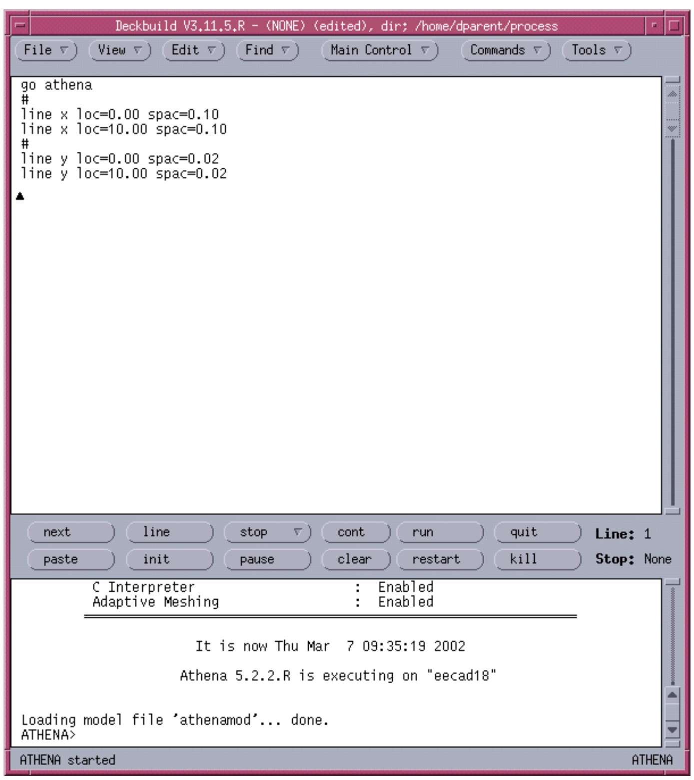

Figure 11: Completed mesh statements in run deck.

Now we need to initialize the 2-D mesh to a semiconductor type and doping. In this case, [100] silicon with a resistively of 10 ohms per square.

Right click on the commands pop up and select mesh define. A pop up like Figure 12 should appear. Fill it out like Figure 12.

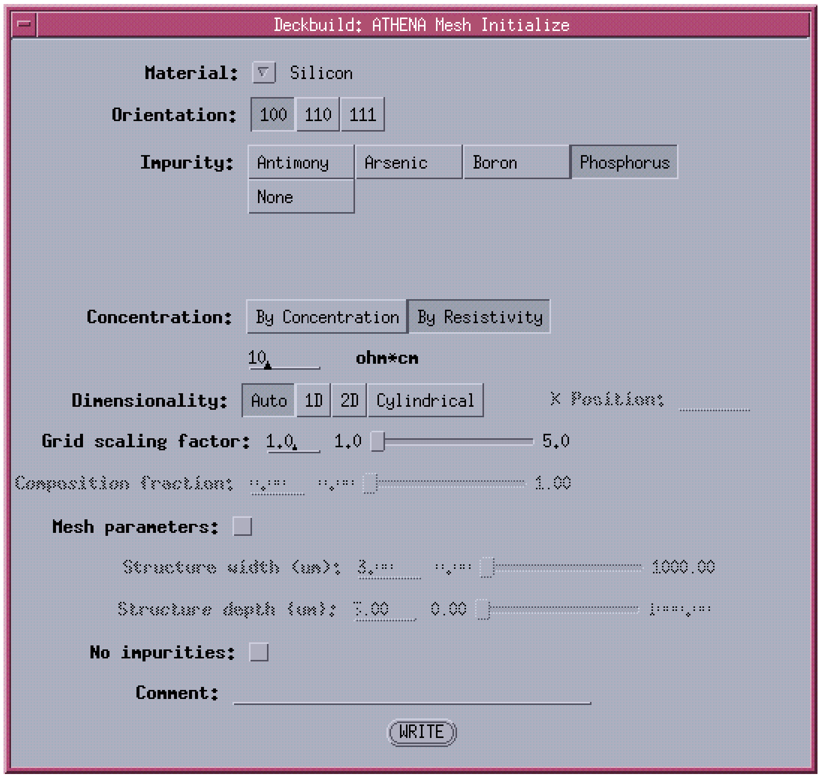

Figure 12: Initializing Mesh

Click write and you should see your run deck modified as in Figure 13.

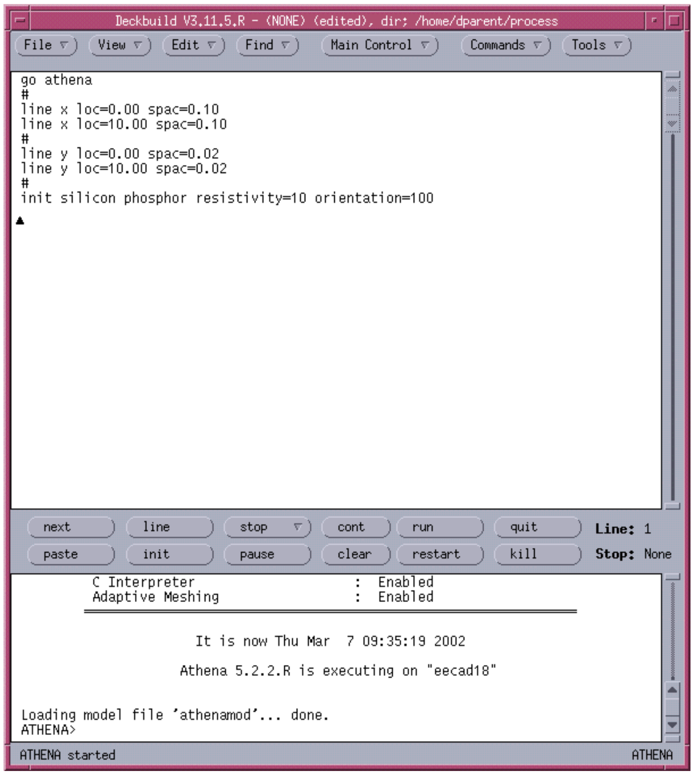

Figure 13: Initialized run deck.

Now save your run deck by right clicking on File... Save, fill out the pop like Figure 14.

You run deck should look like Figure 15.

Click on run. You should get an error that says you exceeded the maximum number of points. Even if the simulator could handle this number of points, it would take too long to do any simulations.

Change the y spacing to .2 (Figure 16), and run the deck again. It should run with out any errors (Figure 17).

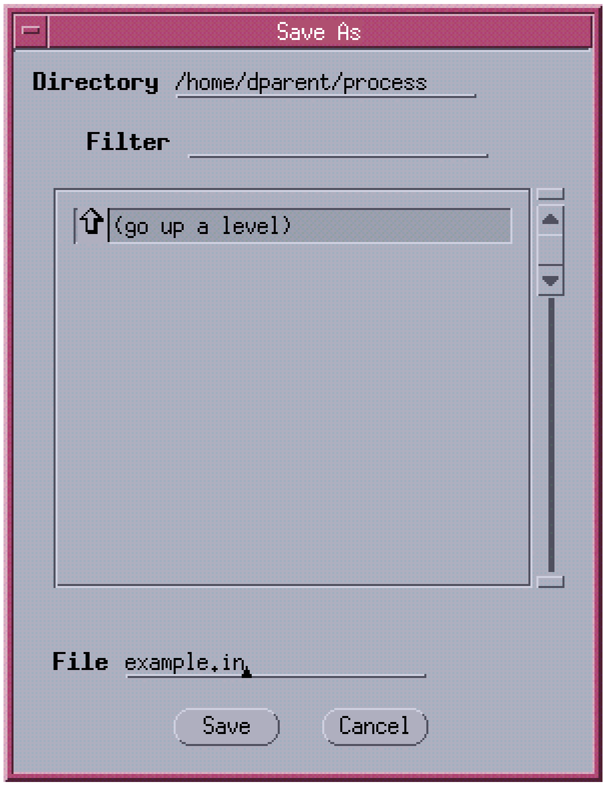

Figure 14: Saving a file.

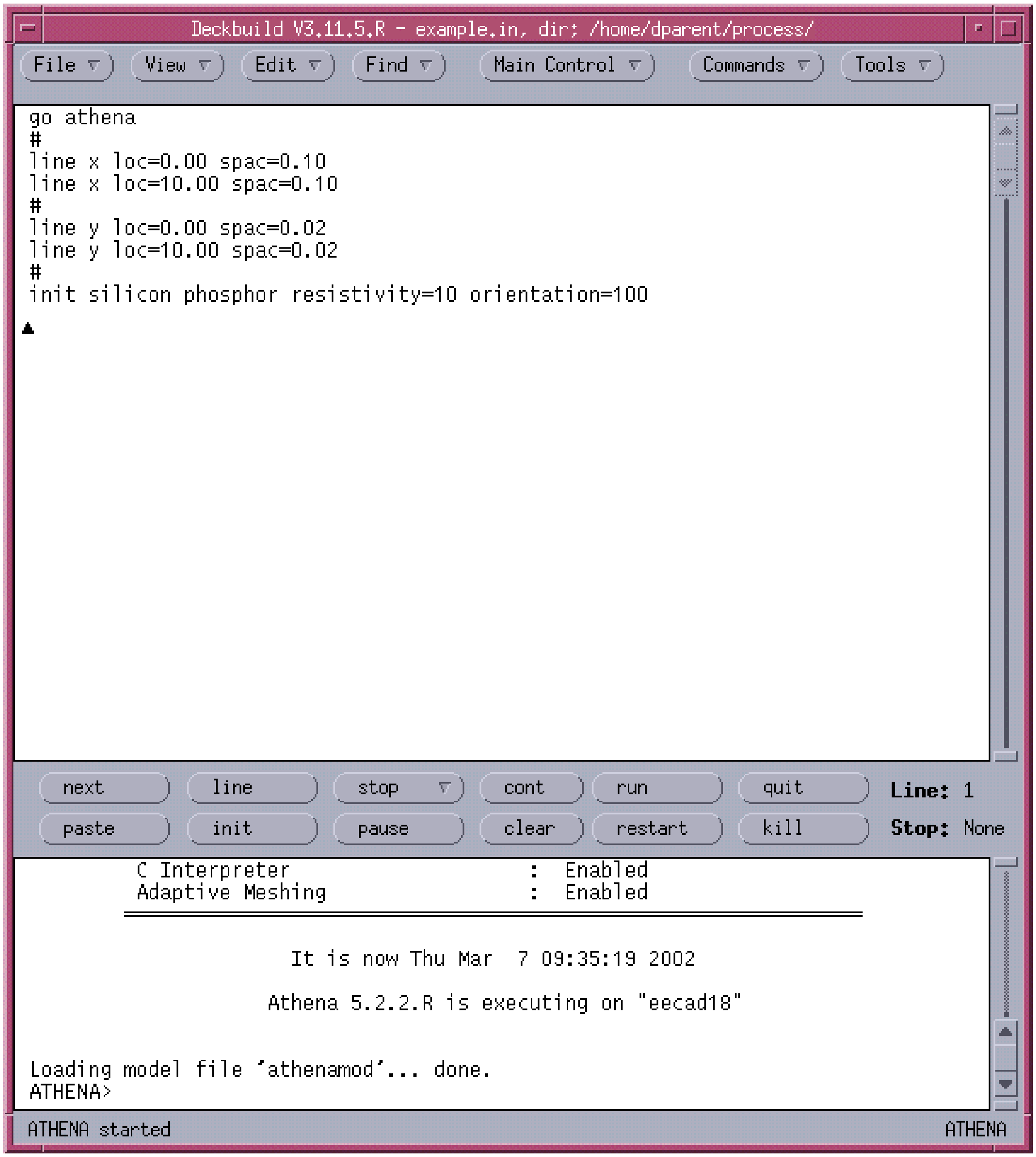

Figure 15: Initialized run deck.

```
go athena
#
line x loc=0.00 spac=0.10
line x loc=10 spac=0.10
#
line y loc=0.00 spac=0.2
line y loc=10 spac=0.2
#
init silicon phosphor resistivity=10 orientation=100
```

Figure 16: Change y spacing to .2.

```
ATHENA>
ATHENA> #
ATHENA> line x loc=0.00 spac=0.10
ATHENA> line x loc=10 spac=0.10
ATHENA> #
ATHENA> line y loc=0.00 spac=0.2
ATHENA> line y loc=10 spac=0.2
ATHENA> #
ATHENA> init silicon phosphor resistivity=10 orientation=100
ATHENA> struct outfile=.history02.str
ATHENA>
```

Figure 17: Output of initialized Run Deck.

To extract the sheet resistance of the layer go to Commands... Extract and a pop-up like Figure 18 should appear.

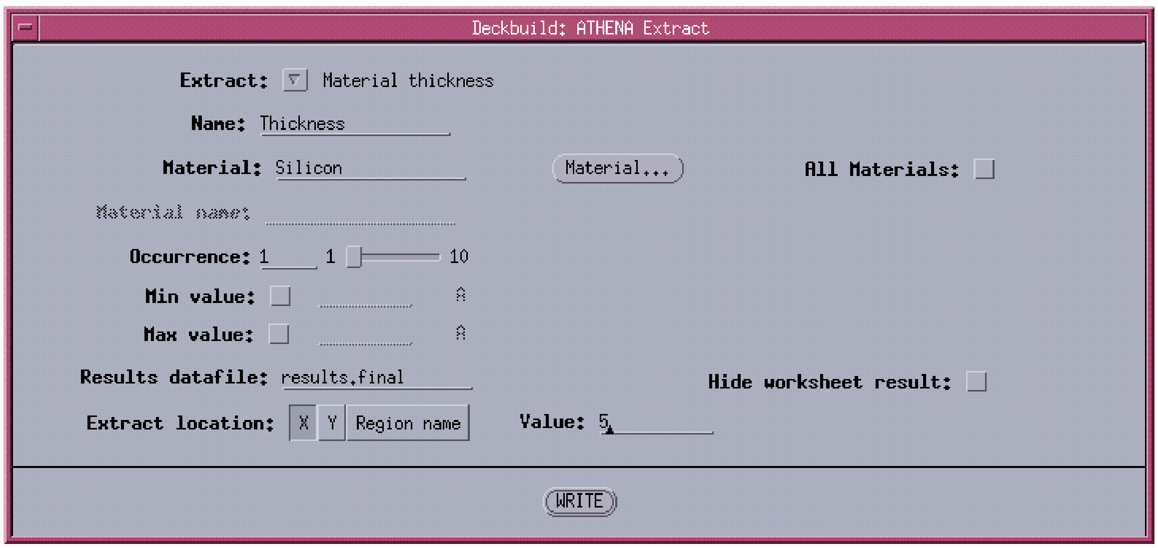

Figure 18: Extract Pop-up.

Fill out the pop-up according to Figure 19 and then click write your run deck should look like Figure 20 .

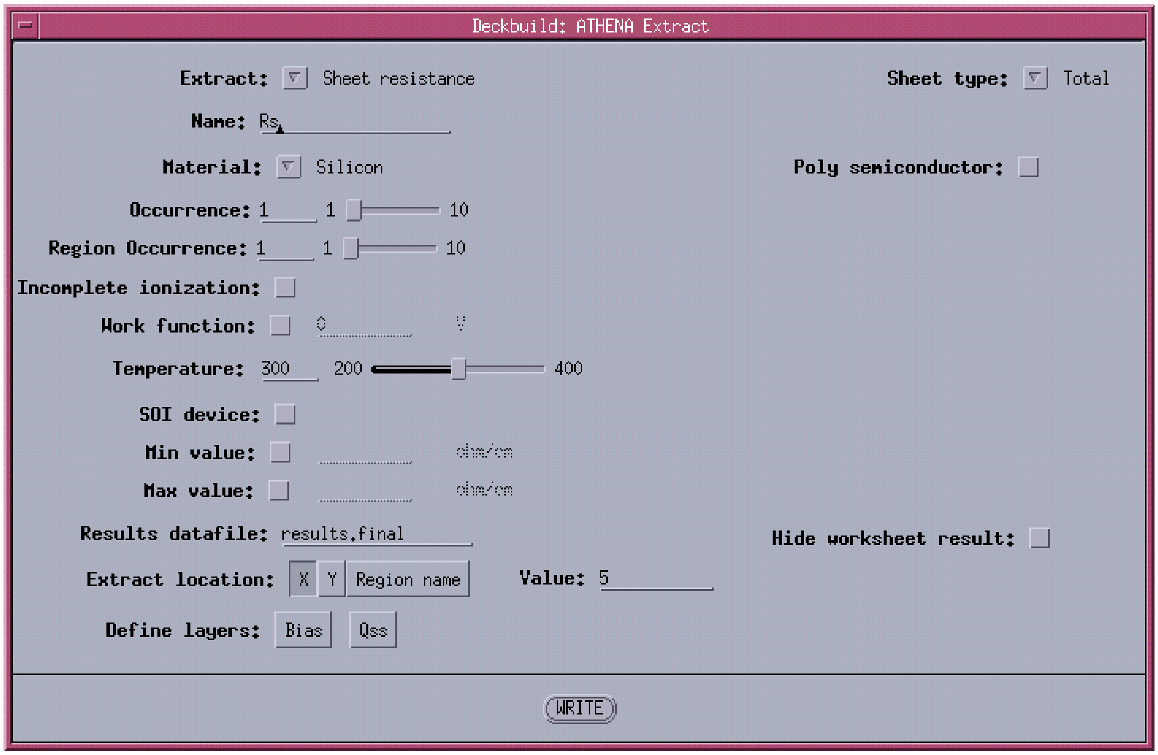

Figure 19: Extract Rs.

```
go athena
#
line x loc=0.00 spac=0.10
line x loc=10 spac=0.10
#
line y loc=0.00 spac=0.2
line y loc=10 spac=0.2
#
init silicon phosphor resistivity=10 orientation=100
#
extract name="Rs" sheet.res material="Silicon" mat.occno=1 x.val=5 \
        region.occno=1
```

Figure 20: Run deck for extracting Sheet Resistance at X position 5um.

Run the deck your output should look like Figure 21.

```
ATHENA> struct outfile=.history03.str
ATHENA> #
ATHENA> struct outfile=/tmp/deckbIAAPCaOnP
ATHENA>
EXTRACT> init inf="/tmp/deckbIAAPCaOnP"
EXTRACT> extract name="Rs" sheet.res material="Silicon" mat.occno=1 x.val=5
region.occno=1
Rs=10497.4 ohm/square  X.val=5
EXTRACT> quit
```

Figure 21: Extraction Output.

Note theoretically the sheet resistance should the resitivity of the layer divided by the thickness, for this case the sheet resistance should be according to hand calculations 10000 ohms even, not 10497 ohms. In reality the four-point probe can only measure sheet resistances up to 30 ohms/square.

Creating a diode by diffusion:

To tell Athena to create a P+/n diode by diffusion go to Commands... Process.... Diffuse and a pop-up like Figure 22 should appear. Fill out the pop-up according to Figure 23 and click write. Repeat the same procedure for Figure 24 and Figure 25 Your completed run deck should look like Figure 26.

To extract the sheet resistance and junction depth of the diffused layer go to Commands.. Extract and fill out the pop-ups as in Figure 27 and Figure 28. Your run deck should look like Figure 29.

Run the deck, the output should look like Figure 30.

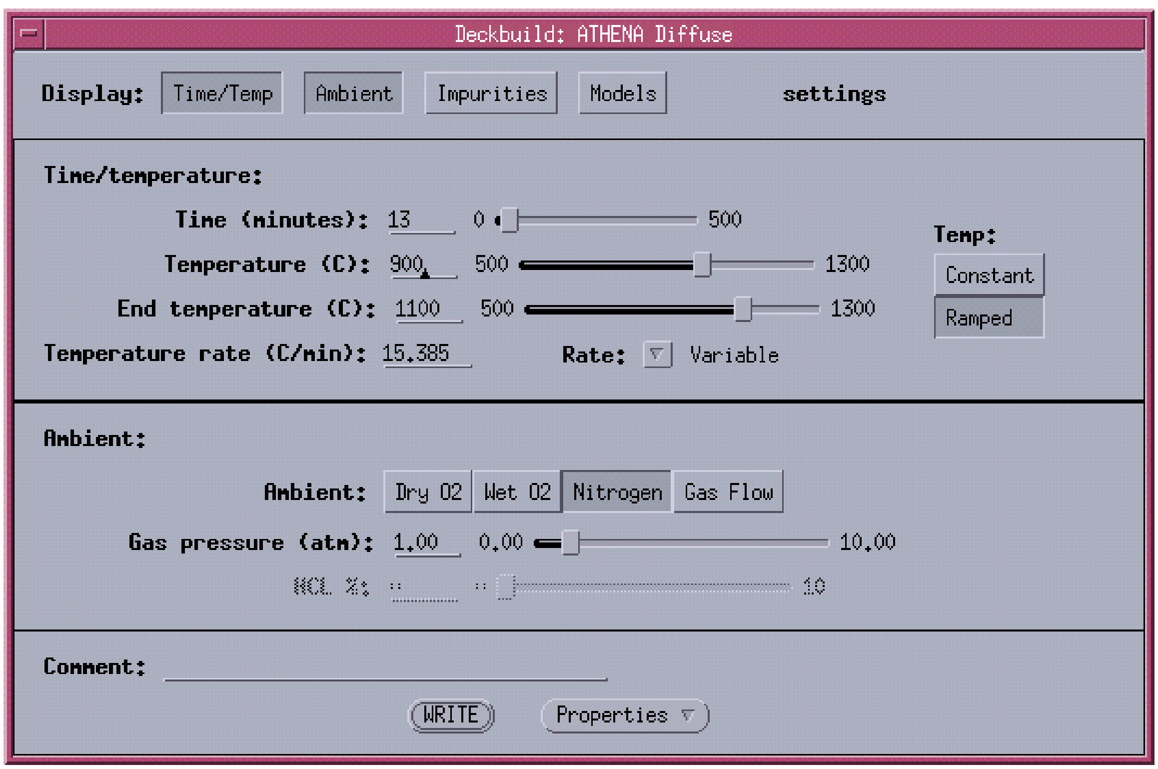

Figure 22: Diffusion Pop-up.

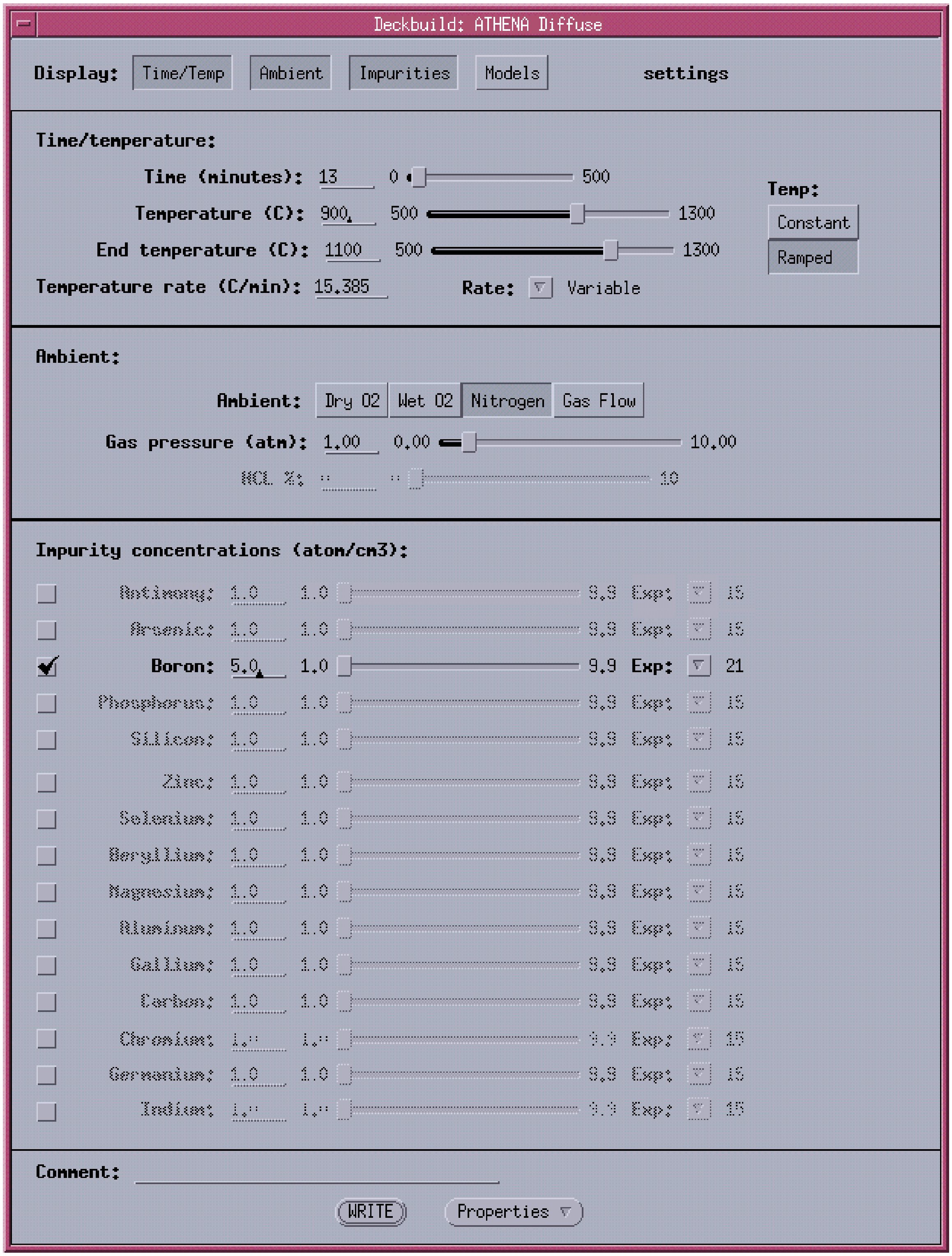

Figure 23: Ramp Diffusion in Nitrogen.

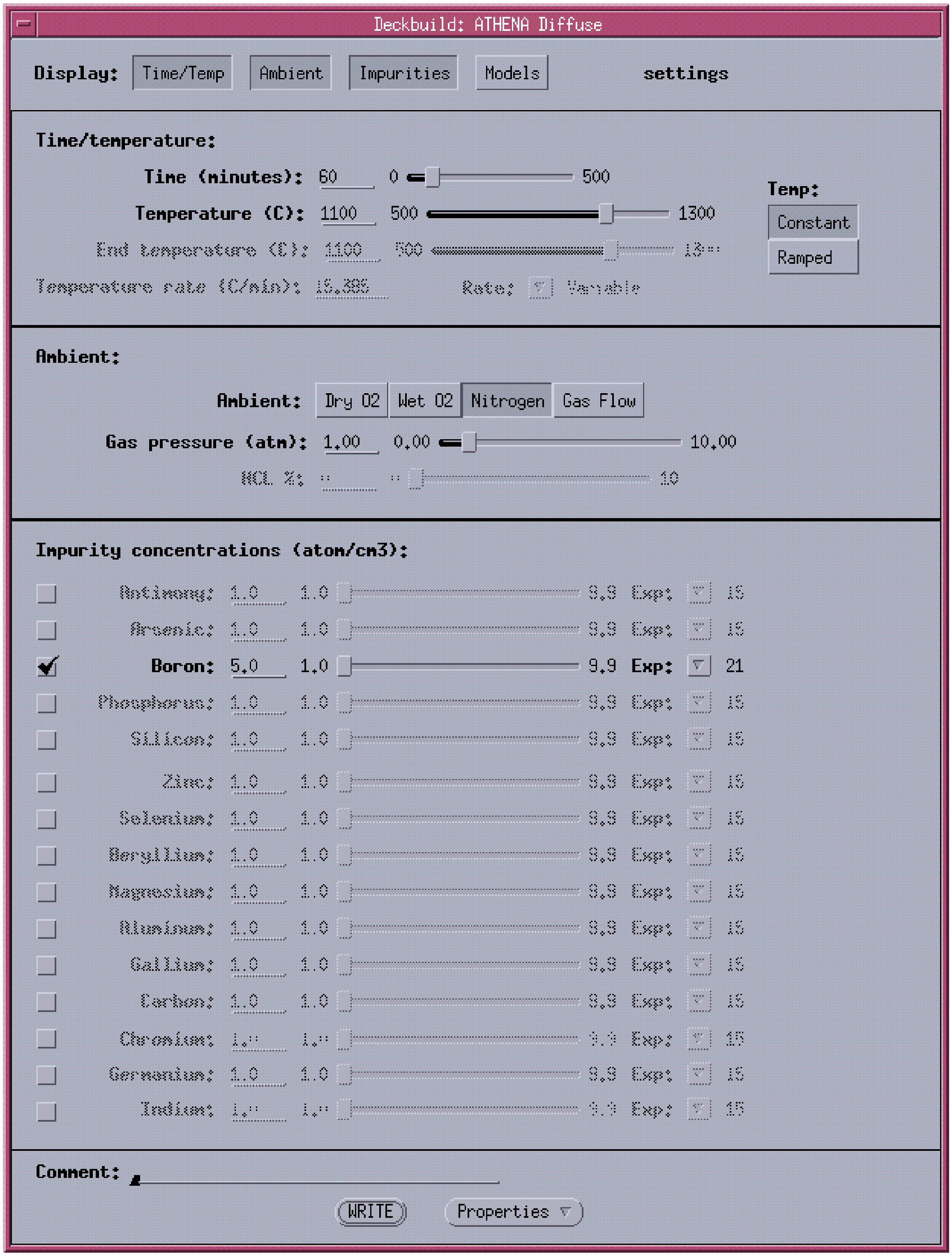

Figure 24: 60 minute B Diffusion.

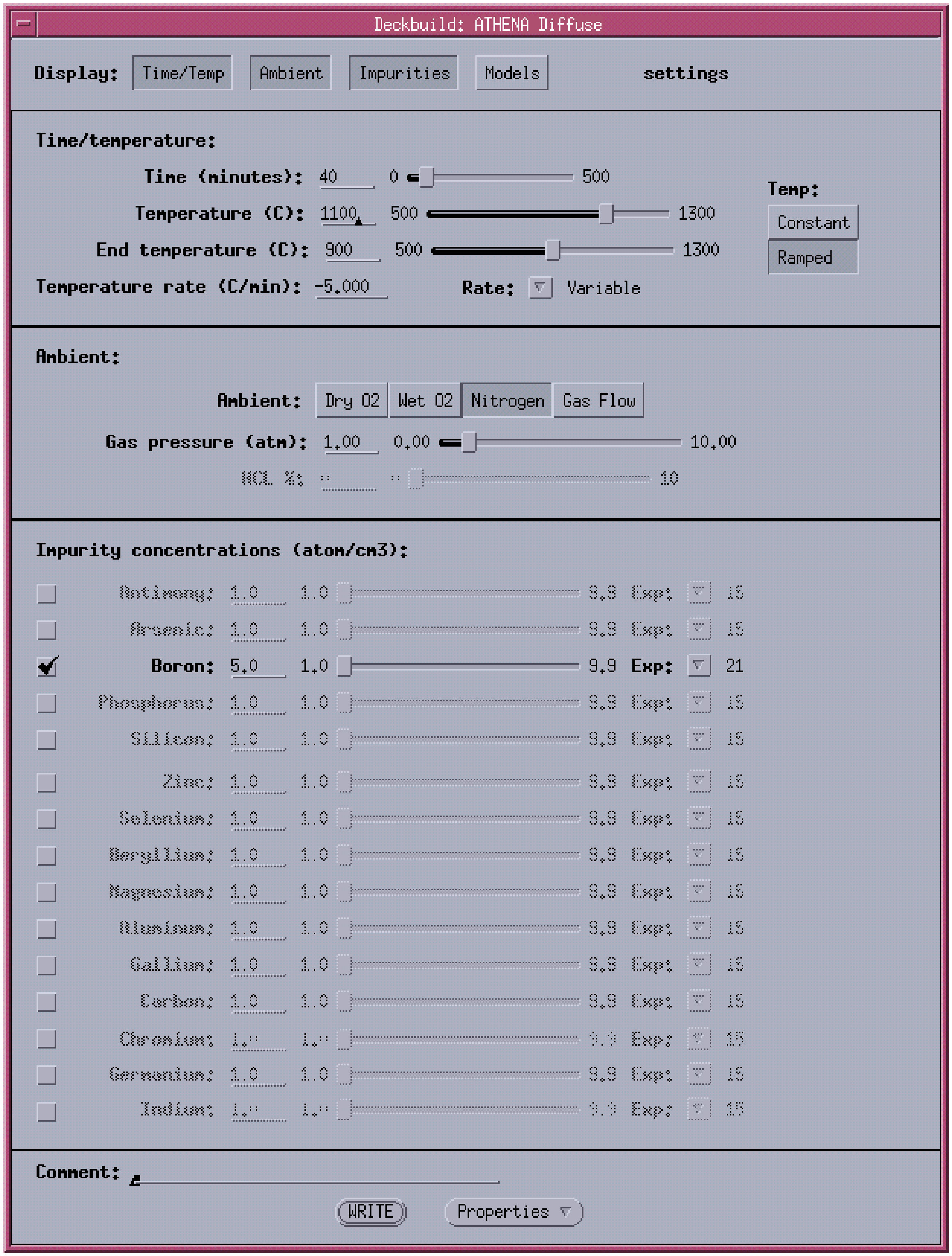

Figure 25: Ramp down Diffusion.

```
go athena
#
line x loc=0.00 spac=0.10
line x loc=10 spac=0.10
#
line y loc=0.00 spac=0.2
line y loc=10 spac=0.2
#
init silicon phosphor resistivity=10 orientation=100
#
#
extract name="Rs" sheet.res material="Silicon" mat.occno=1 x.val=5 \
        region.occno=1
#
diffus time=13 temp=900 t.final=1100 nitro press=1.00 c.boron=5e21
#
diffus time=60 temp=1100 nitro press=1.00 c.boron=5e21
#
diffus time=40 temp=1100 t.final=900 nitro press=1.00 c.boron=5e21
```

Figure 26: Run deck for a B diffusion with Ramp.

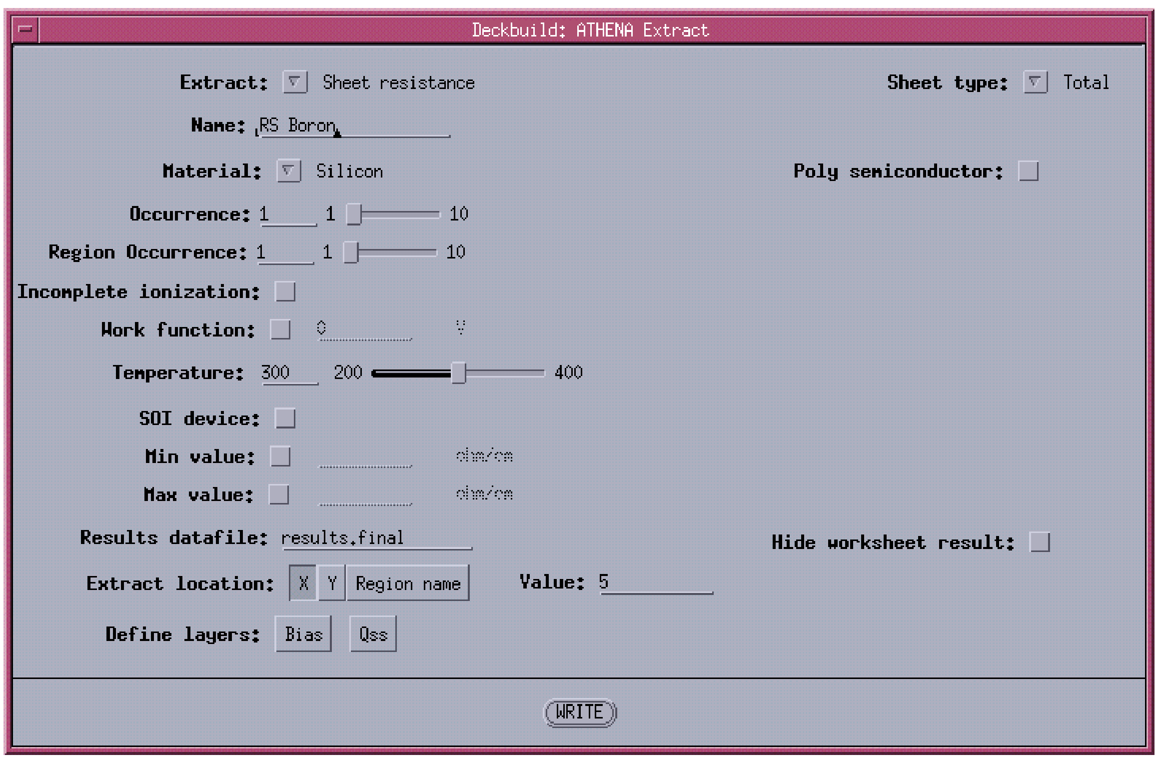

Figure 27: Extract Sheet Resistance.

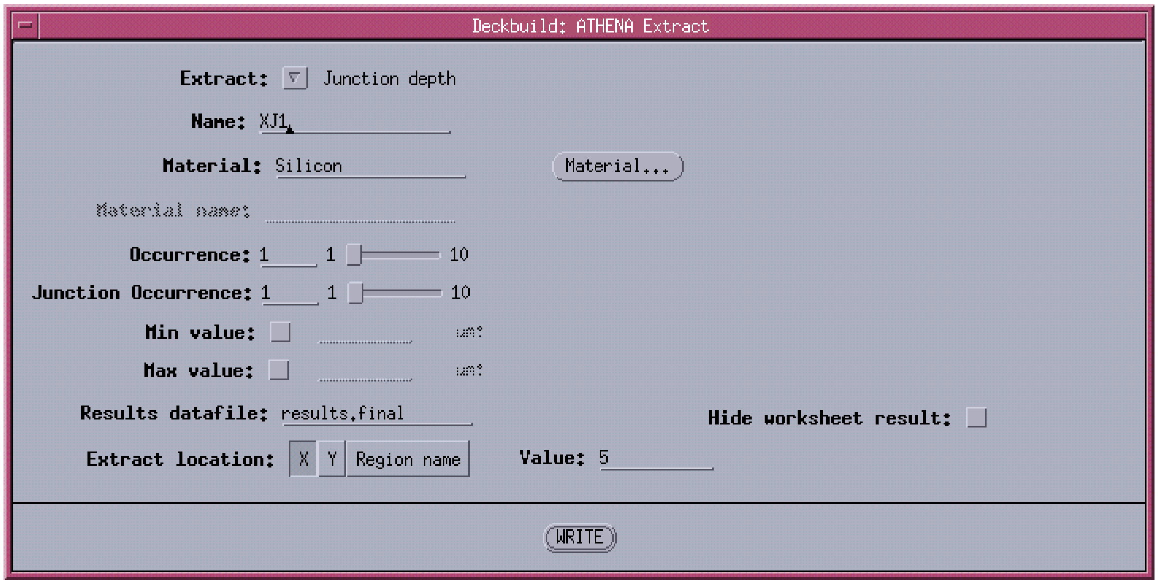

Figure 28: Extract Junction Depth.

```
go athena
#
line x loc=0.00 spac=0.10
line x loc=10 spac=0.10
#
line y loc=0.00 spac=0.2
line y loc=10 spac=0.2
#
init silicon phosphor resistivity=10 orientation=100
#
#
extract name="Rs" sheet.res material="Silicon" mat.occno=1 x.val=5 \
        region.occno=1
#
diffus time=13 temp=900 t.final=1100 nitro press=1.00 c.boron=5e21
#
diffus time=60 temp=1100 nitro press=1.00 c.boron=5e21
#
diffus time=40 temp=1100 t.final=900 nitro press=1.00 c.boron=5e21
#
extract name="RS Boron" sheet.res material="Silicon" mat.occno=1 x.val=5 \
        region.occno=1
#
extract name="XJ1" xj material="Silicon" mat.occno=1 x.val=5 junc.occno=1
```

Figure 29: Run deck for Diffused Diode.

```
EXTRACT> init inf="/tmp/deckbLAASCaOnP"
EXTRACT> extract name="RS Boron" sheet.res material="Silicon" mat.occno=1
x.val=5  region.occno=1
RS Boron=4.88553 ohm/square  X.val=5
EXTRACT> #
EXTRACT> extract name="XJ1" xj material="Silicon" mat.occno=1 x.val=5
junc.occno=1
XJ1=3.17939 um from top of first Silicon layer  X.val=5
EXTRACT> quit
```

Figure 30: Output of Diffusion run deck.

Experimenting with the mesh:

We can use fewer points on the mesh, but this will sacrifice accuracy to see this effect change the y spacing to 2, and then run the deck. It should look like Figure 31. Notice that the junction depths and sheet resistance values are difference by a large amount! Since we would like to use the minimum amount of grid points try refining the mesh until we get close to the valuesd obtained at a y spacing of .2

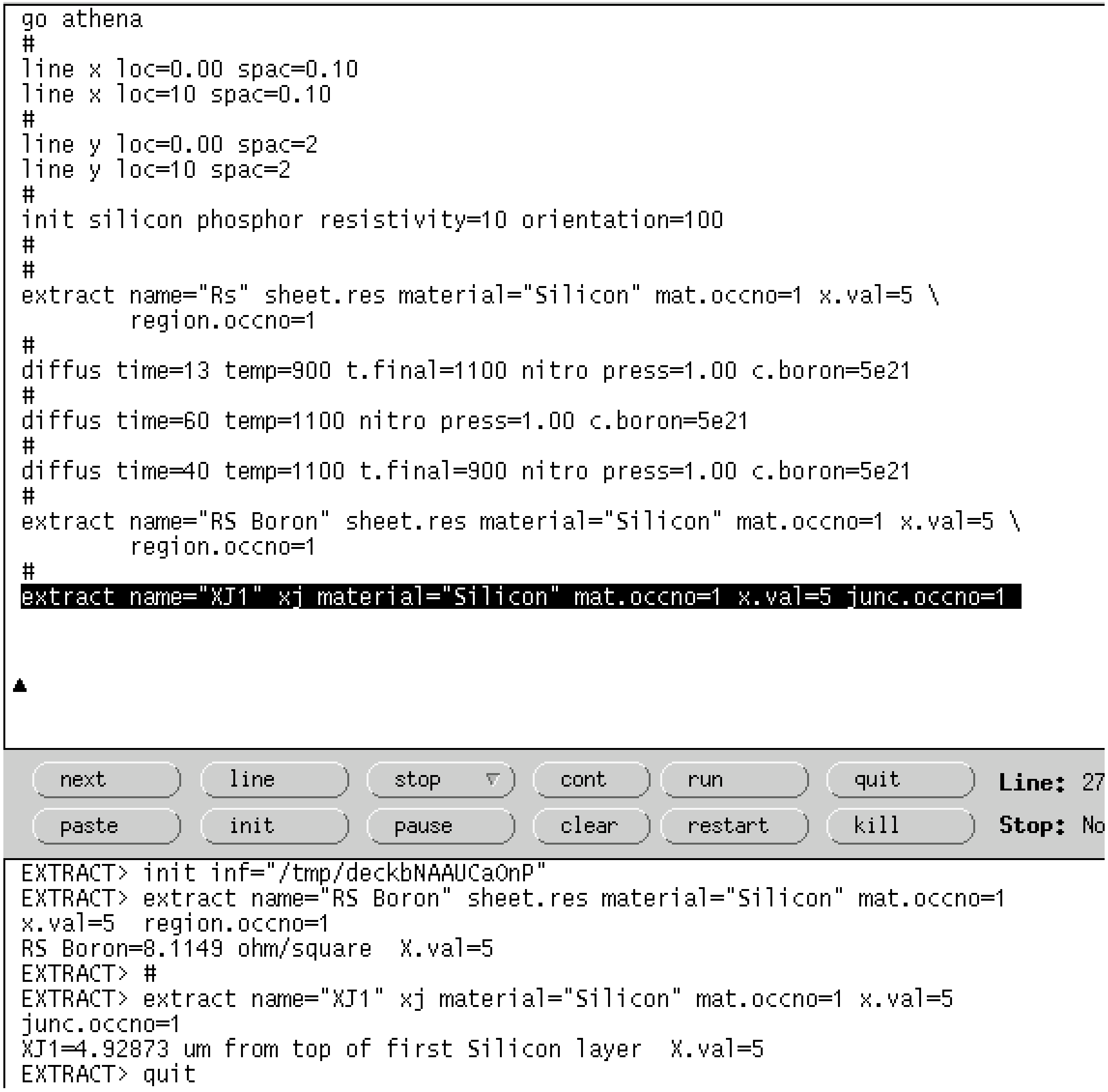

Figure 31: Relaxed mesh.

Changing the spacing according to Table 1. Table 1 shows the error between successive runs of the RS and XJ of the diffused layer. You probably did not notice any change in the simulation time as the mesh was refined because this is still a 1-D simulation. We can see that a mesh spacing of .25 or even .5 is acceptable.

Table 1: Refining Mesh.

Y Spacing (mm)	Rs w/❑	XJ(mm)	Rs Rel Error	Xj Rel Error
0.2	4.88	3.127		
2	8.11	4.9	-66.18852459	-56.69971218
1	5.477	3.77	-12.23360656	-20.56283978
0.5	5.01	3.33	-2.663934426	-6.491845219
0.25	4.89	3.12	-0.204918033	0.223856732
0.125	4.89	3.18	-0.204918033	-1.694915254

Plotting the Impurity Curve:

To plot the impurity profile you just calculated, make sure that no text in the run deck is highlighted. Click on Tools.. Plot and should appear.

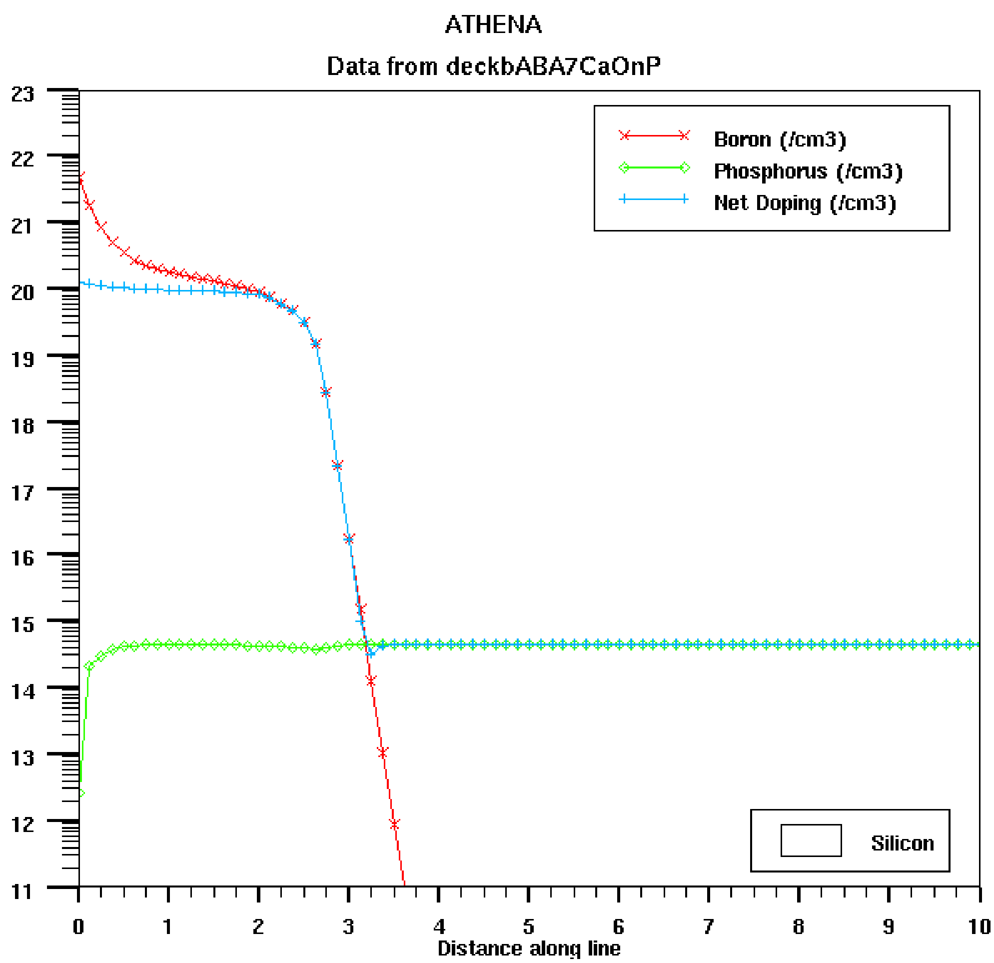

Figure 32: Impurity profile.

Viewing the extraction results:

You can view all the extraction results by going to the terminal that your run directory is in and typing more r* in the terminal. You should see a figure close to that of Figure 33.

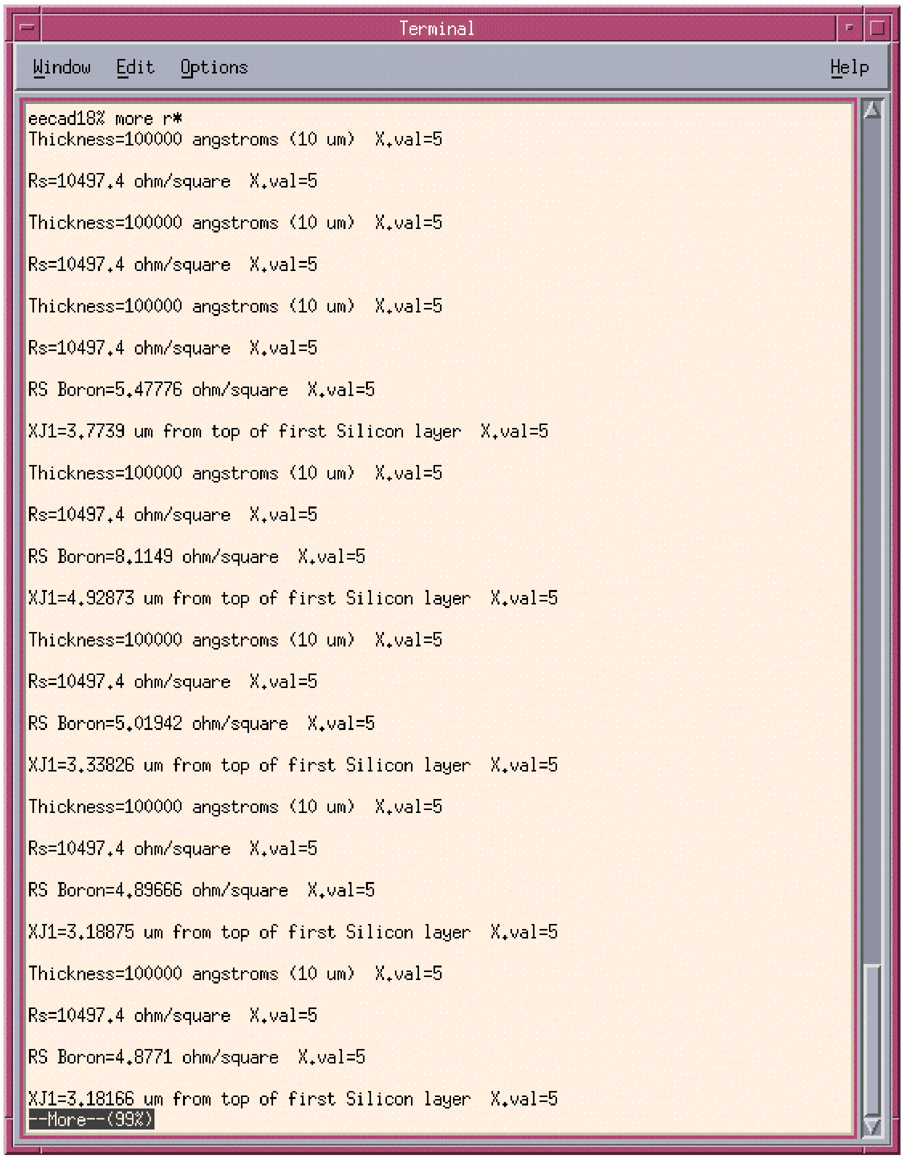

Figure 33: Results File.

Running the Atlas Electrical Simulation:

Once you have created a device you can simulate its electrical and optical properties in Atlas. Writing an Atlas Deck is extremely hard so the best method is to find an existing simulation for the examples file and then modify it to the device you want to study.

We will use an NMOS example. To load this in, first save your diffusion run deck and then go to Main control Examples (Figure 34).

Index

1 MOS1 : MOS Application Examples

2 MOS2 : Advanced MOS Application Examples

3 BJT : Bipolar Application Examples

4 DIODE : Diode Application Examples

5 SOI : Application Examples

6 EPROM : Application Examples

7 LATCHUP : CMOS Latchup Application Examples

8 ESD : ESD Application Examples

9 POWER : Power Device Application Examples

10 ISOLATION : ISOLATION Applications Examples

11 MESFET : Application Examples

12 HBT : HBT Application Examples

13 HEMT : HEMT Application Examples

14 FastATLAS : FastBlaze MESFET and HEMT Application Examples

15 QUANTUM : Device Simulation with Quantum Mechanics

Figure 34: List of Example Files.

Then click on MOS 1 Examples and then NMOS ID/VGS Threshold Voltage Extraction until the exmaples window looks like Figure 35.

1 MOS1 : MOS Application Examples

1.1 mos1ex01.in : NMOS : Id/Vgs and Threshold Voltage Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating an Id/Vgs curve and extracting threshold voltage and other SPICE parameters. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=0.1V
- parameter extraction for Vt, linear gain (beta) and mobility rolloff (theta)

Figure 35: MOS Example.

Clcik on load example and the sample run deck should appear in Deck build (Figure 36).

```
go athena

#
line x loc=0.0 spac=0.1
line x loc=0.2 spac=0.006
line x loc=0.4 spac=0.006
line x loc=0.6 spac=0.01
#
line y loc=0.0 spac=0.002
line y loc=0.2 spac=0.005
line y loc=0.5 spac=0.05
line y loc=0.8 spac=0.15
#
init orientation=100 c.phos=1e14 space.mul=2

#pwell formation including masking off of the nwell
#
diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
#
etch oxide thick=0.02
#
#P-well Implant
#
implant boron dose=8e12 energy=100 pears

#
diffus temp=950 time=100 weto2 hcl=3
#
#N-well implant not shown -
```

Figure 36: Sample MOS Run Deck.

Read through the run deck and you will see all the basic steps for fabricating a .5 micron NMOS transistor with a lightly doped drain. Click run. Notice that after the etch poly left command that the simulation slows down considerably. That is because now the simulation is truly 2-D. After about three minutes a 2-D cross Section is plotted (Figure 37).

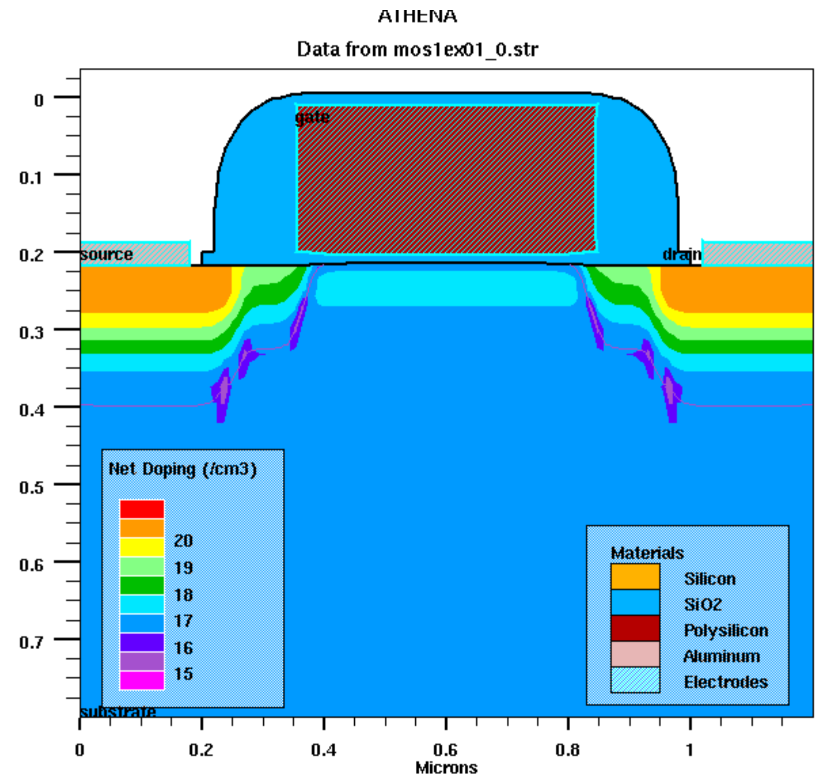

Figure 37: 2-D cross Section of An NMOS.

add how to view mesh junction depth with discussion

Manipulating the View in Tonyplot

The output of Figure 37 shows a contour plot of the doping. The orange areas are mpre highly doped than the blue areas. The junction can be seen by the purple line, but can be hard to see with this view.

To view the manipulate Tonyplot go to the Tony Plot window and left click on plot. A pop-up like Figure 38, should appear.

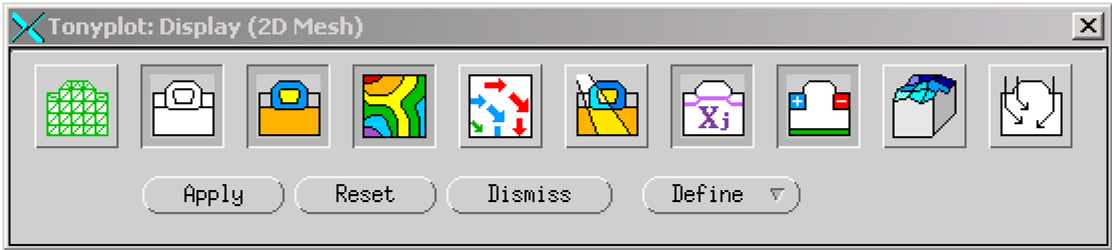

Figure 38.: Plot Window

Unselect Xj and Contour buttons as in Figure 39 and click apply. Your figure should look like Figure 40.

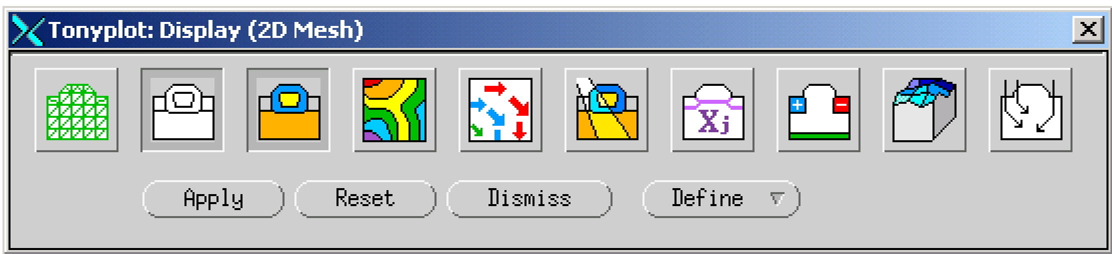

Figure 39: Delecting Xj and Doping Contour.

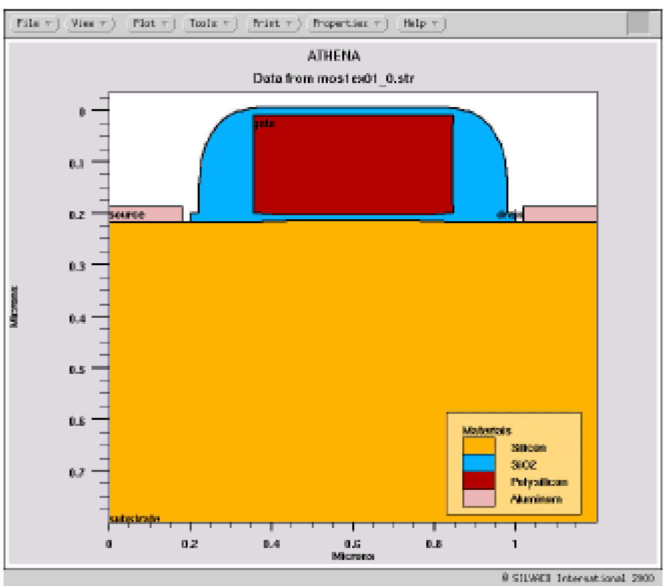

Figure 40: Results of deselecting Doping Contour and Xj

Select mesh and Xj as in Figure 41 and click on apply. Your figure should look like Figure 42. Notice how the mesh is finer in the gate oxide region and the junction near the channel.

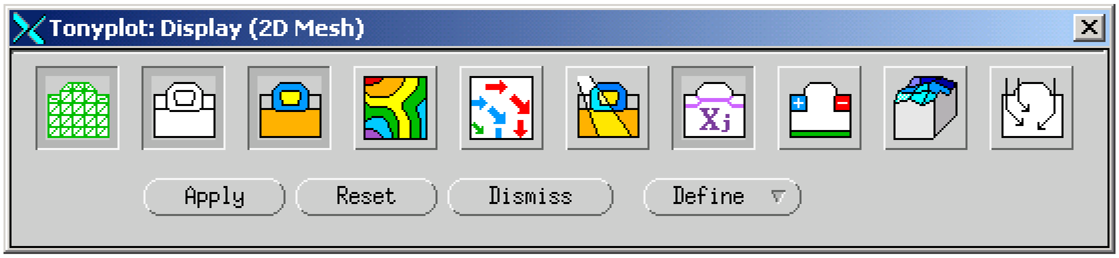

Figure 41: Selecting Mesh and Xj.

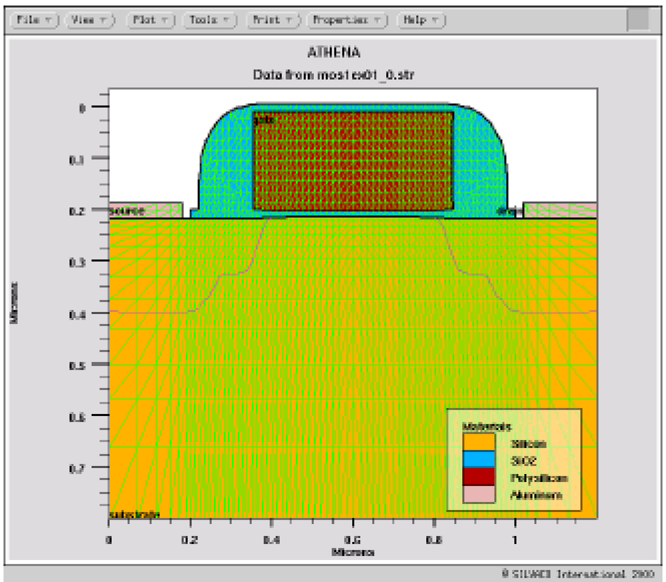

Figure 42: Viewing Mesh and Xj.

To view a doping profile in the middle of the channel go to Tools ... Cutline in Tonyplot. A pop-up like Figure 43 should appear.

Draw a vertical line done the middle of the MOSFET and you should see the results in Figure 44

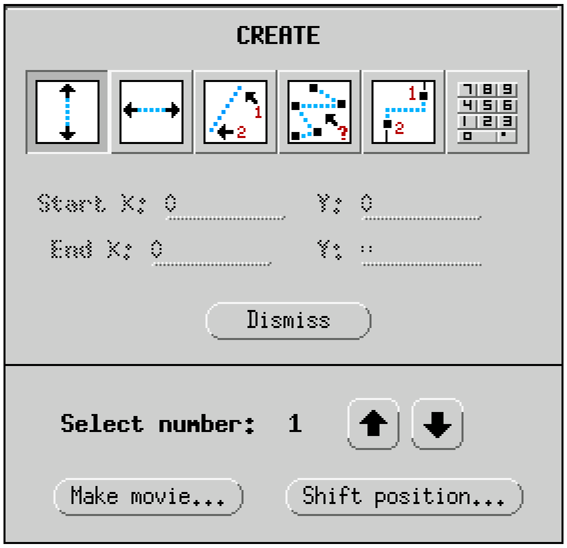

Figure 43: Creating a Cutline to View Doping Profile.

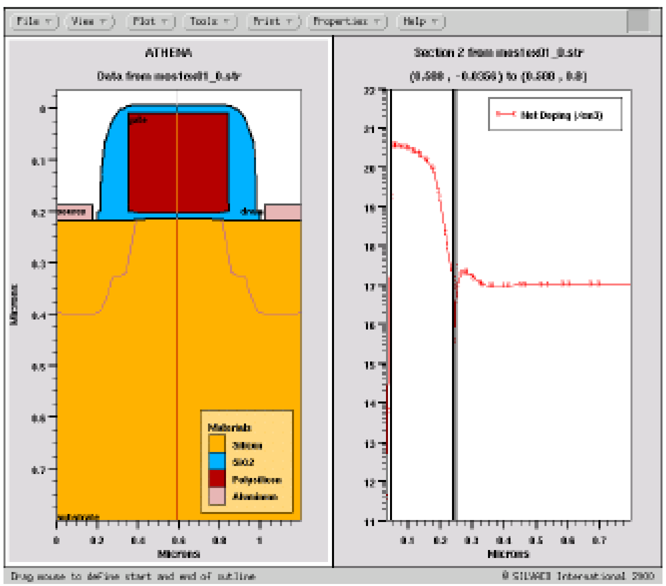

Figure 44: Output of Cutline.

To see the Phosphorous and Boron doping concentrations click on the doping profile window until a white line surrounds it. Then go to Plot Display in Tonyplot and a pop-up like Figure 45 should appear. Select Boron and Phosphorous and click on apply. You should see the results as in Figure 46

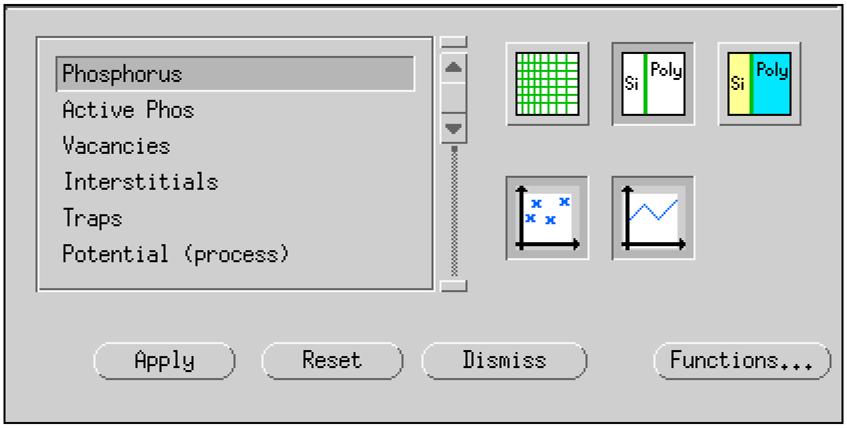

Figure 45: Selecting to View Boron and Phosphorus Doping Concentration.

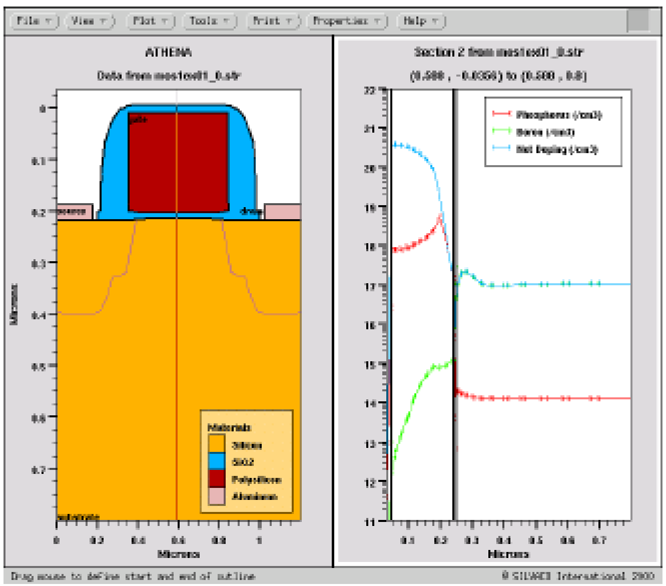

Figure 46: Viewing Boron and Phosphorous Doping Concentration.

Go to Tools... Ruler and draw a box around the poly silicon gate to measure the as drawn gate length of the MOSFET.

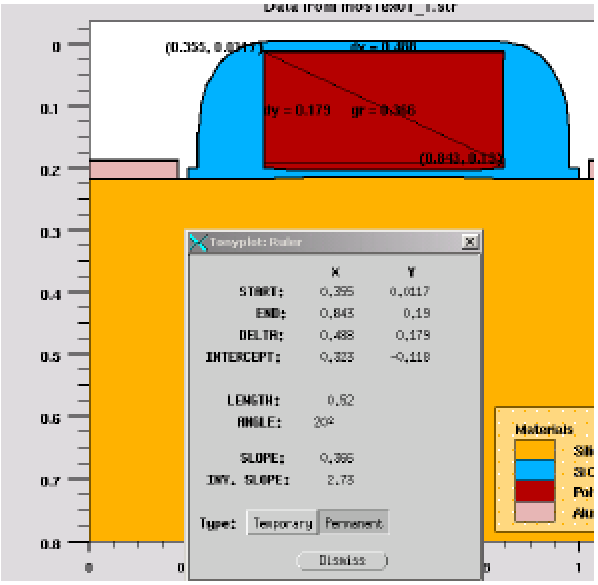

Figure 47: Using the ruler to measure the as drawn Gate Length.

To measure the effective channel length under zero bias Use the cutline tool to draw a horizontal line across the channel as close to the gate oxide as possible. Draw a ruler from where the junctions are (Figure 48) and you should get a channel length of about .4mircons.

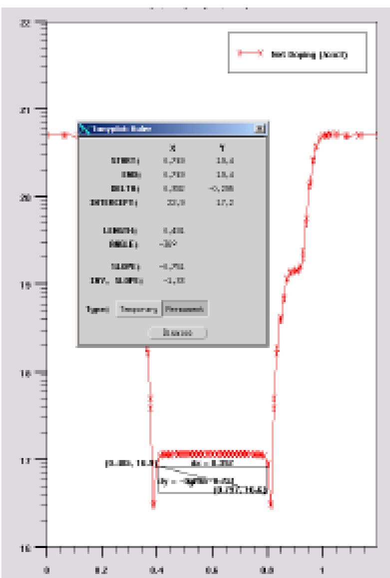

Figure 48: Effective Channel length.

View the electrical simulation results:

After a few more minutes plot of VG tied to VD vs ID is plotted (Figure 50). The VT, KN and theta are all extracted from the curve in the run deck window (Figure 49).

```
nvt=0.507118
EXTRACT> extract name="nbeta"
slope(maxslope(curve(abs(v."gate"),abs(i."drain"))))  *
(1.0/abs(ave(v."drain")))
nbeta=0.00025345
EXTRACT> extract name="ntheta" ((max(abs(v."drain")) *
$"nbeta")/max(abs(i."drain")))  - (1.0 / (max(abs(v."gate")) - ($"nvt")))
ntheta=0.133788
EXTRACT> quit
```

Figure 49: Extracted NMOS parameters.

The Atlas Report states that it only used 2 minutes of real time (Figure 52). Reduce the spacing by as in (Figure 53) and re-run the simulation. The simulation time shoots up, but the accuracy remains the same. Re plot the grid and you will that the mesh is finer.

Sometimes you want to read a specific point of the graph. This can be done by going to Tools... HP4145. You can move the cursor to each data point (Figure 51). You can also draw line to extract the x intercept of a MOSFET curve in the saturation regime (Lambda).

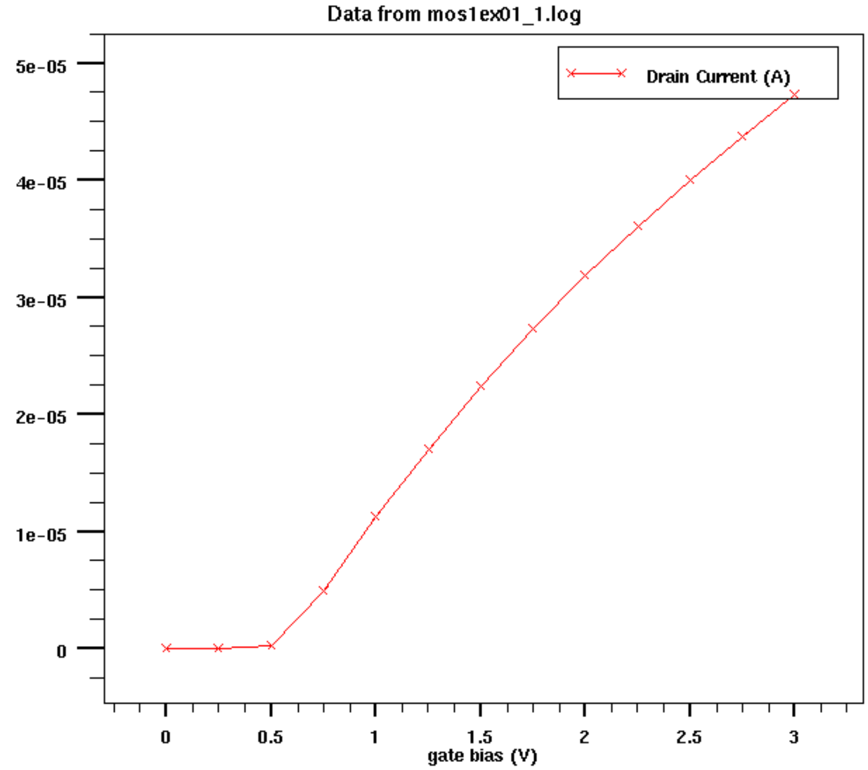

Figure 50: VG, vs. ID (VD=.1V).

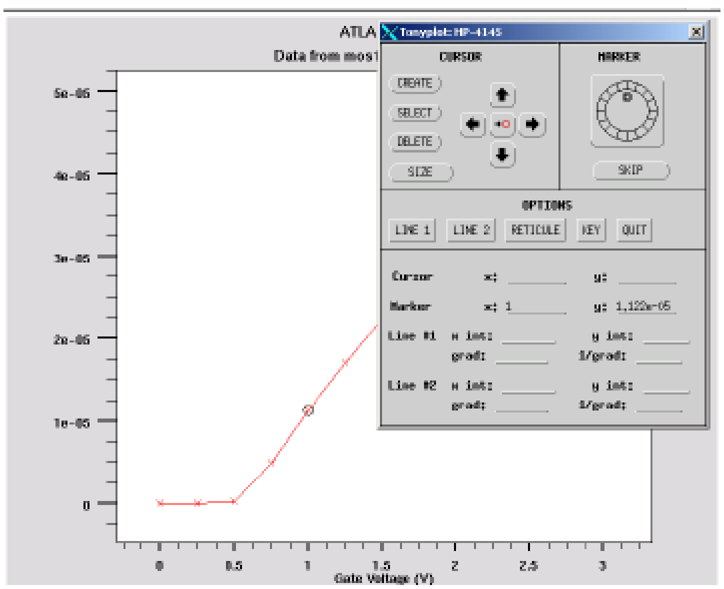

Figure 51: Using the HP4145 function to view individual points.

```
ATLAS version 5.2.1.R finished at Thu Feb  5 22:19:04 2004

real      2:03.5
user      1:46.0
sys          0.5

*** END ***
```

Figure 52: Time used.

```
#
line x loc=0.0 spac=0.09
line x loc=0.2 spac=0.005
line x loc=0.4 spac=0.005
line x loc=0.6 spac=0.009
#
line y loc=0.0 spac=0.001
line y loc=0.2 spac=0.004
line y loc=0.5 spac=0.04
line y loc=0.8 spac=0.05
#
```

Figure 53: Refined mesh.

Exercises:

Adapt the NMOS example file to have a threshold voltage of .25Volts.

Adapt the NMOS example file to produce a channel length of 1 micron.

Make sure to save each run deck under a different name. I will need to see the run deck and the plots.

Chapter

2

Chapter 2: Cross Sections of Process Flow

This Chapter will go over:

1. Setting up your account
    a. Design Entry through schematic capture
    b. Create INV schematic capture
    c. Create INV symbol
    d. Create INV Test bench
2. Simulation using CDS's Spectre (Bsim3 model simulator, different underlying algorthyms than spice or hspice)

Initial Substrate

The initial substrate is (100) Si doped with phosphorus to $4x10^{14}cm^{-3}$ as can be seen in Figure 54. Since the doping is the same every where on the wafer, we can get by with a 1-D representation of the process.

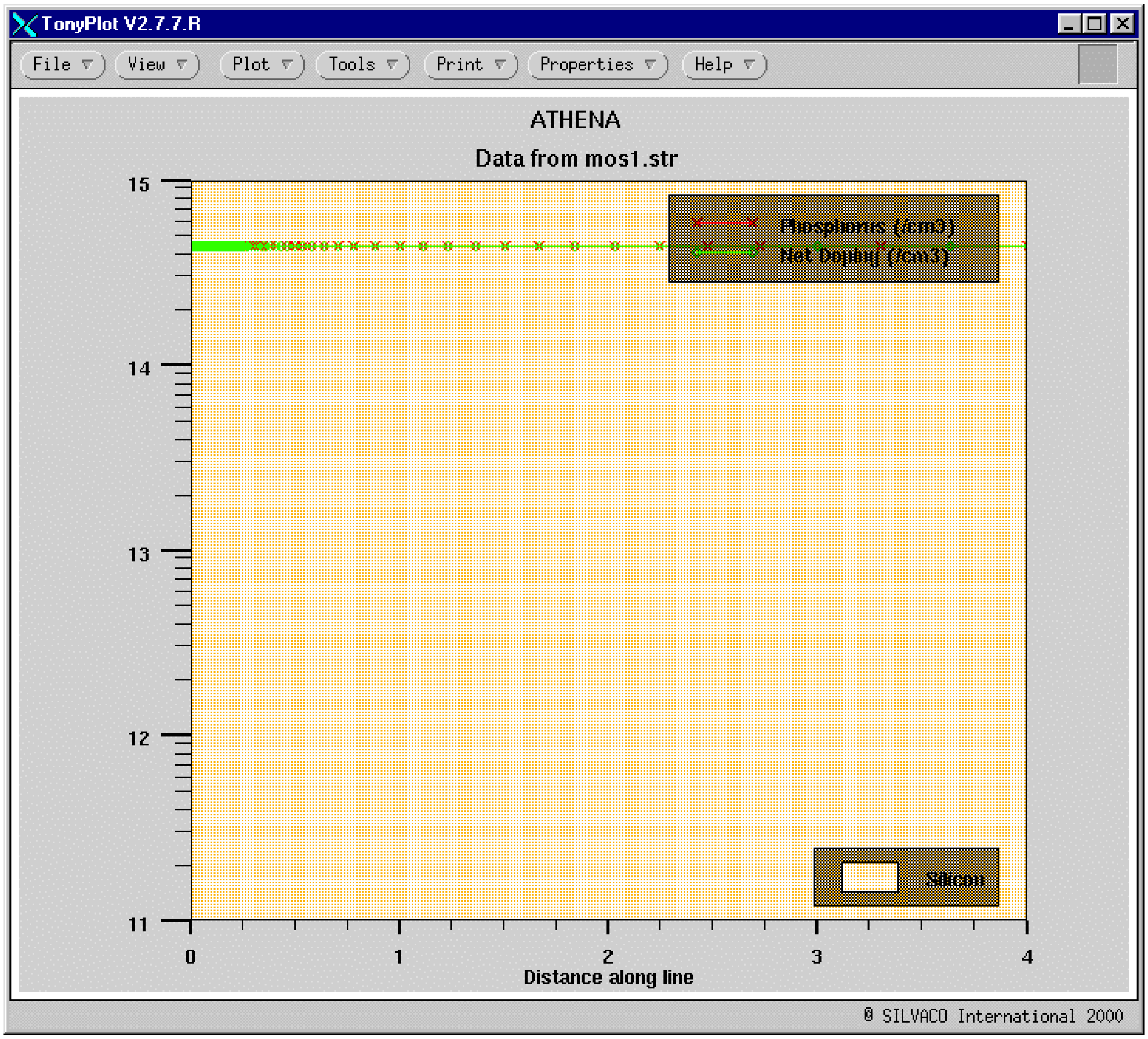

Figure 54: Initail Substrate.

Screening Oxide:

An Initail screening oxide is grown at 1100oC (dry O2) for 30 minutes to protect the wafer during travel around the lab, and to the Implant-Center. It also acts to randomize the ion-beam used to dope the wafer. Dopant pile-up can be seen at the interface of the oxide in Figure 55.

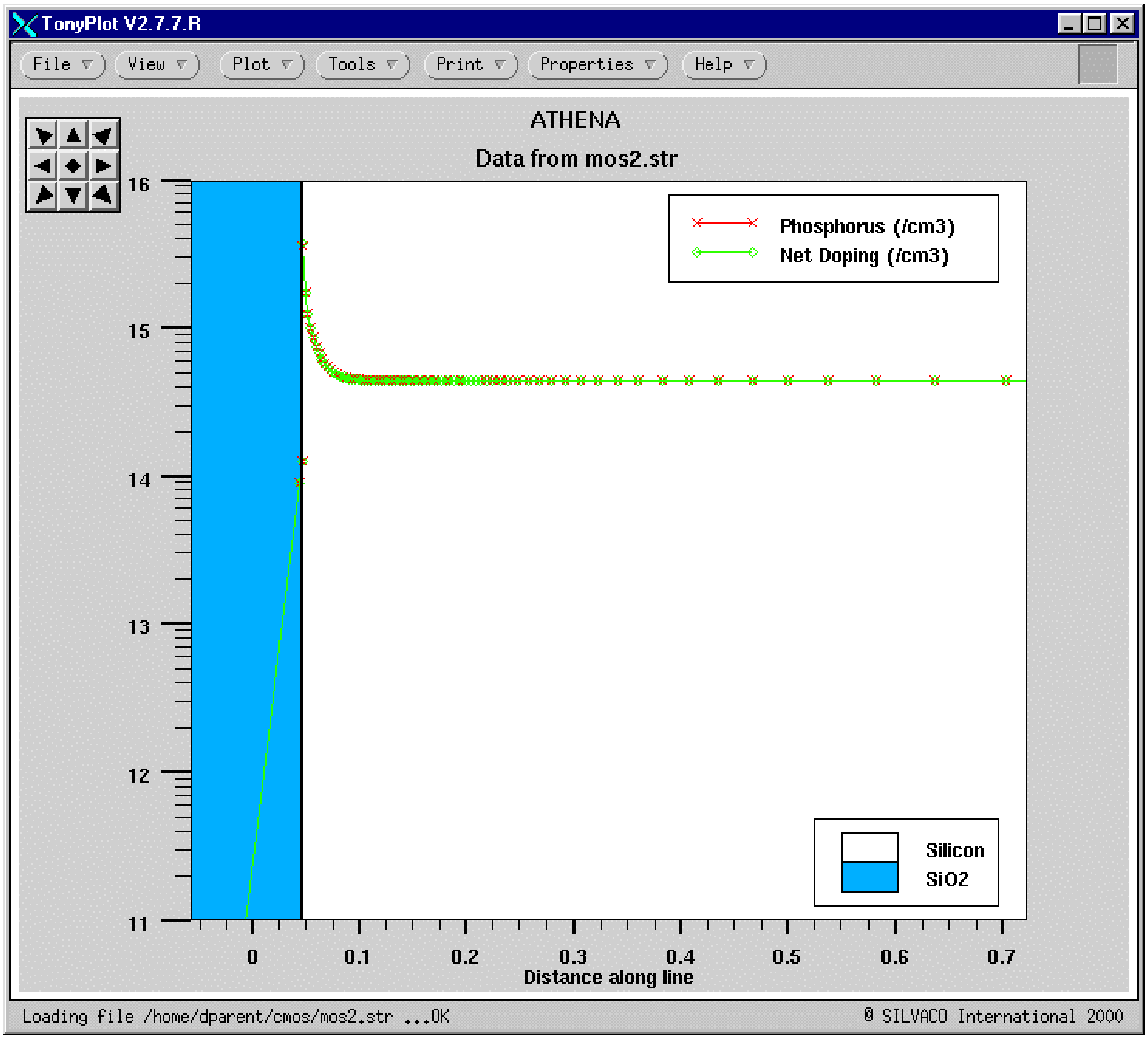

Figure 55: Screening Oxide.

NWELL Implant:

The substrate is too lowly doped to have a useful PMOS threshold voltage we implant (DOSE=1e11, ENERGY=140keV SP=P, Tilt=7, rot=0) All across the wafer to bring up the doping level.

PWELL Implant:

The substrate is n-type, we have to selectively (selectively means PL operation with MASK1) implant a PWELL (Implant DOSE=3e13 Energy=100keV Species=b11, tilt=7, rotation=0) to bring the p-type doping up to the required level. In Figure 56, we can see the doping distribution of the P and the B.

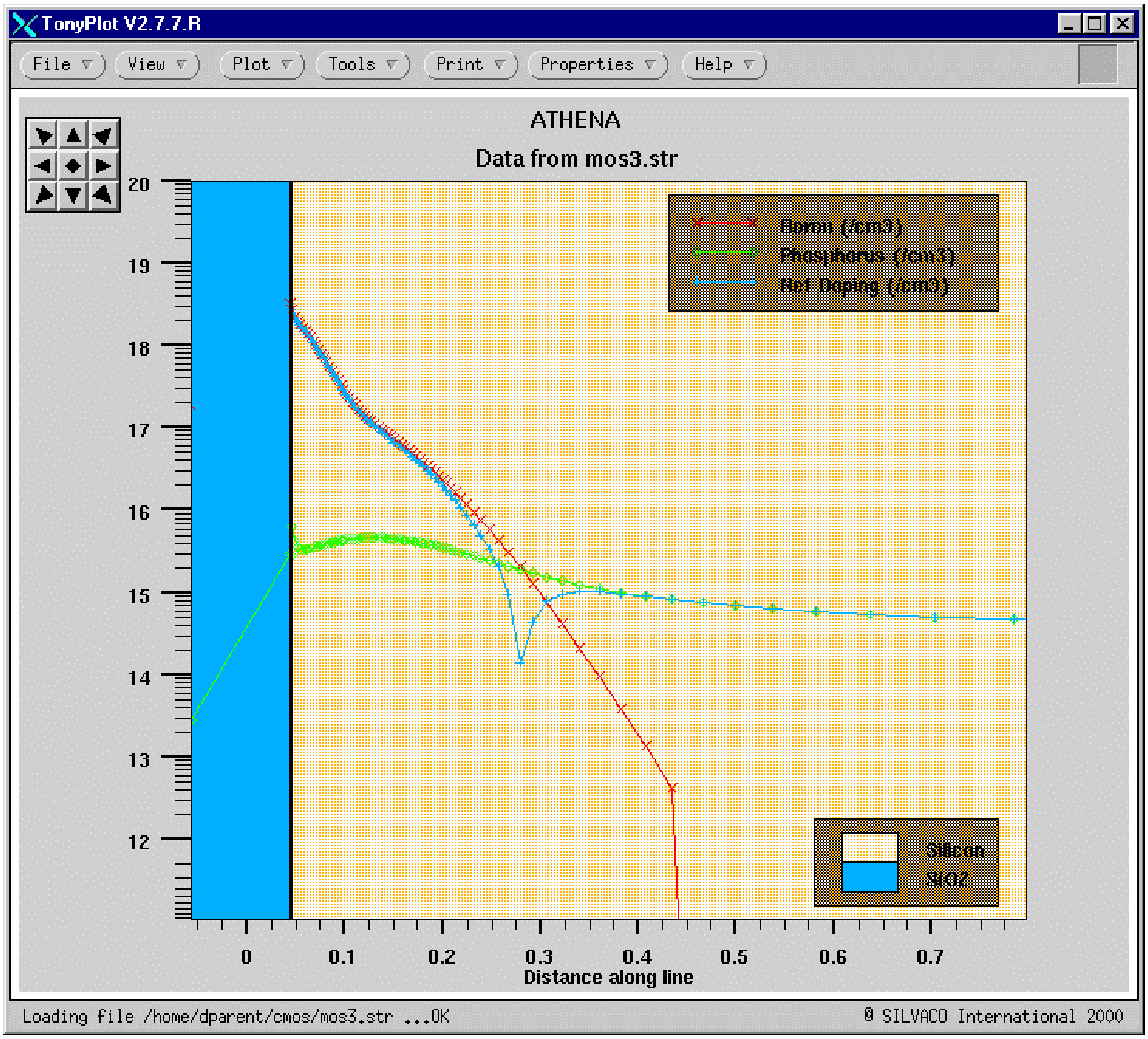

Figure 56: NWELL and PWELL Implants.

Field Oxide Growth:

The next step is to grow a field oxide over the entire wafer. The oxide will be thicker over the n-substrate than the PWELL because the screening oxide was not etched away from the n-substrate regions. This oxide is grown at 1100oC for 30 minutes in steam. The dopant redistribution can be seen in Figure 57.

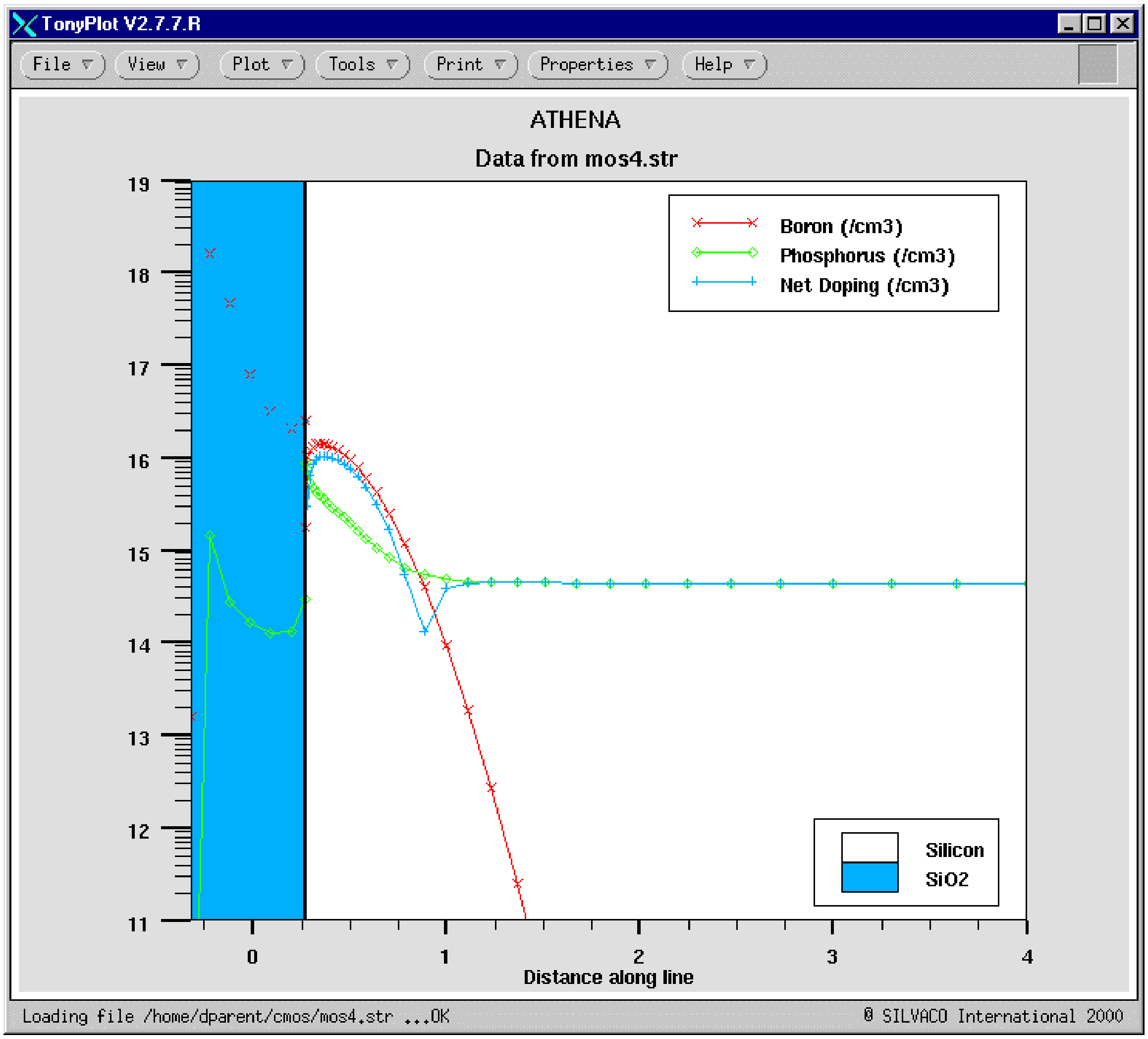

Figure 57: Field Oxide Growth.

Well Drive:

After the Field oxide is grown, we need to drive in the dopants so that the dopant concentration near the surface is correct and that the junction is deep enough to prevent latch-up. his is done at 1150oC for three hours in nitrogen. In Figure 58, We can see that the junction depth has moved out to 2.2 microns.

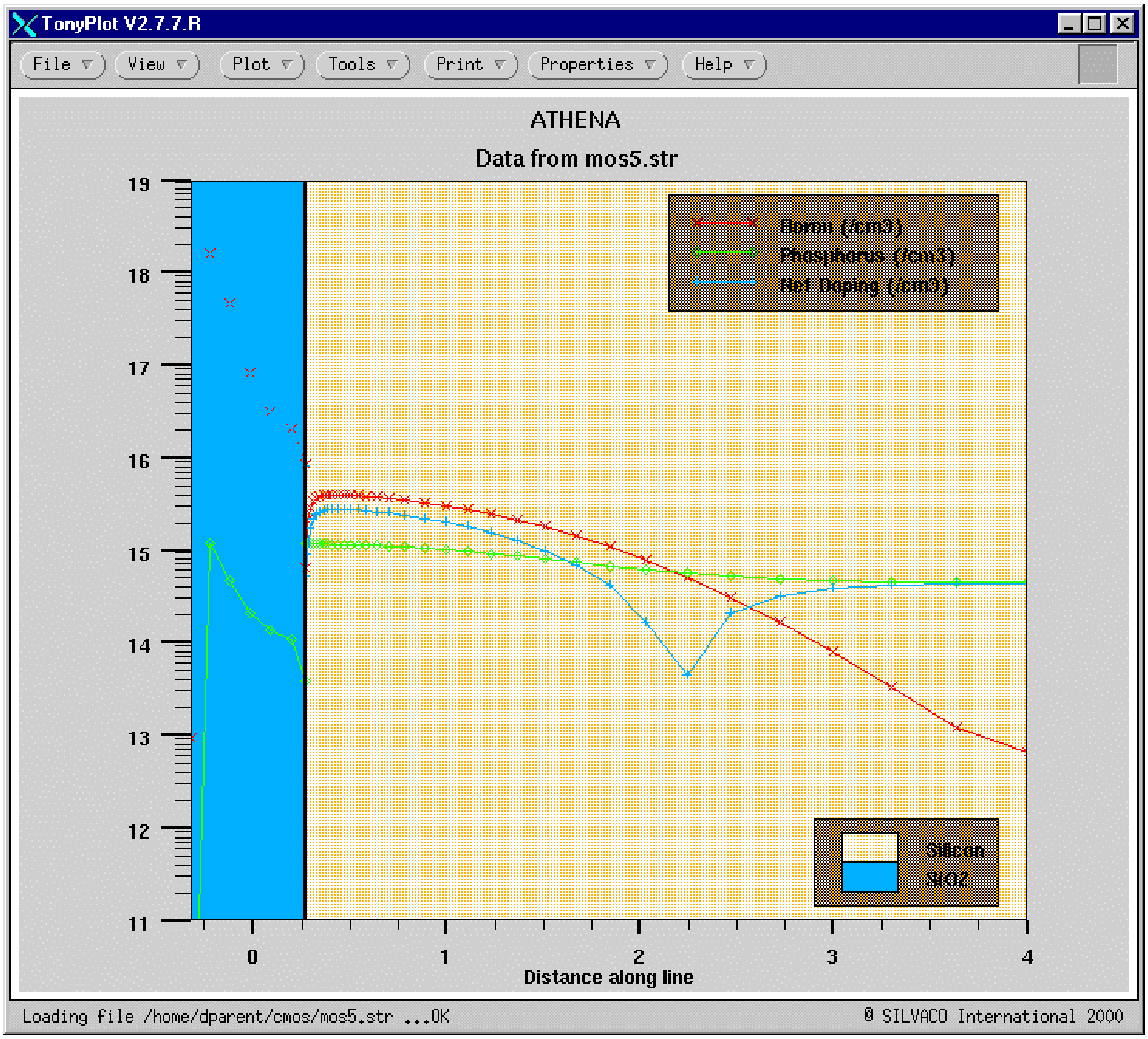

Figure 58: PWELL after Well Drive.

Appendix

A

Appendix A: Grabbing an image for documentation

You will want to save some of your outputs and designs an image that can be imported into a word-processing program. This instruction will show you how to grab an image and save it to a floppy disk for importing into a document or just plain printing.

Start CDS (for example) tools and open up the figure or plot you want to save an image of. For example, use the inverter layout as in Figure 59.

You will need to add some text to identify the image as your own. In the layout tool you create a label, in the schematic tool you add notes. In the layout goto Creat.. label. Fill out the pop-up like Figure 60. Except change the info to your name!

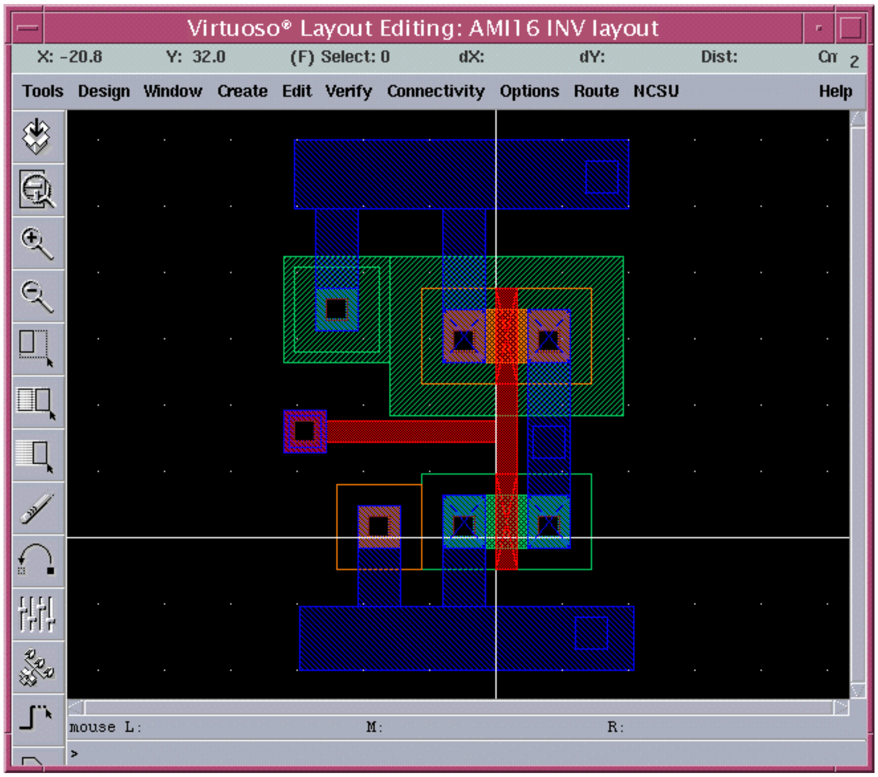

Figure 59: Grabbing the image of your inverter layout.

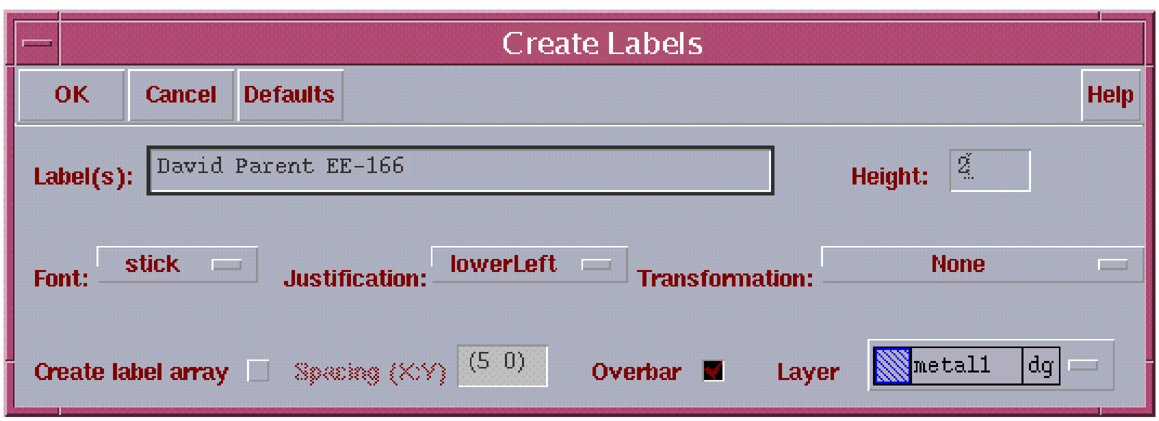

Figure 60: Creating a label.

The software thinks each work is a separate object so click down with the left mouse button to place each word you want displayed, like in Figure 61.

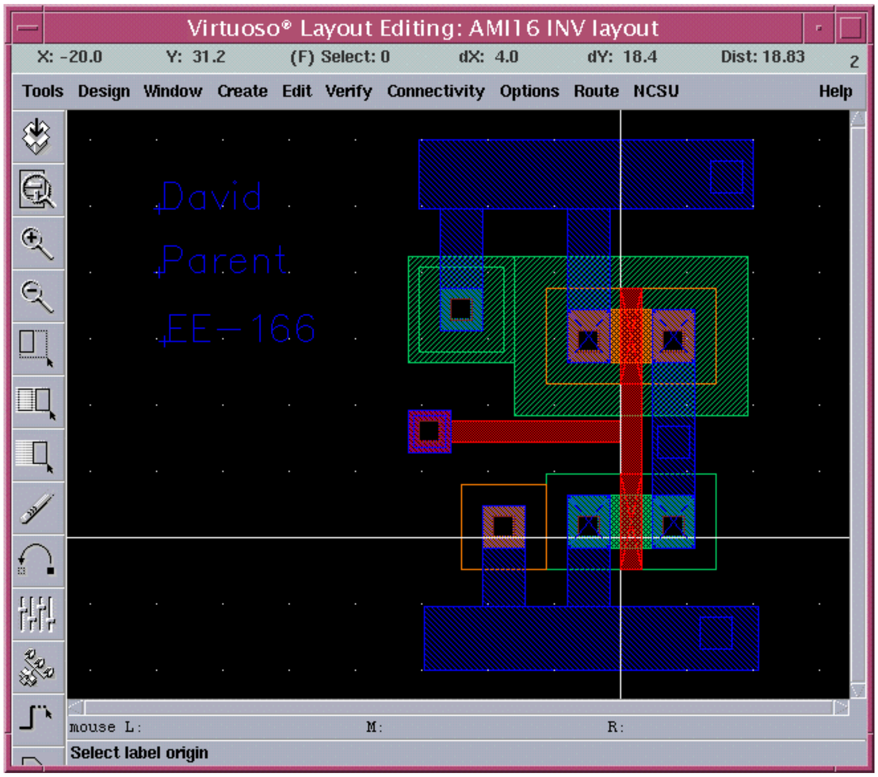

Figure 61: Inverter with text.

You will need to start the image grabber software which comes with the Sun OS.

Right click any where on the screen that is not an application. You should see a pop-up like Figure 62. Highlight Applications and come down to Snapshot like in Figure 63. Left click on Snapshot to start the program. Pop-ups like Figure 64 and Figure 65 should appear on screen.

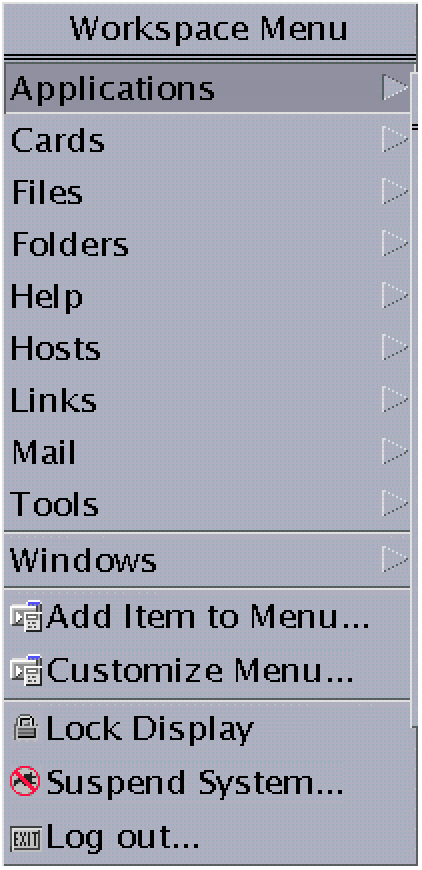

Figure 62: Starting Sun's Snapshot.

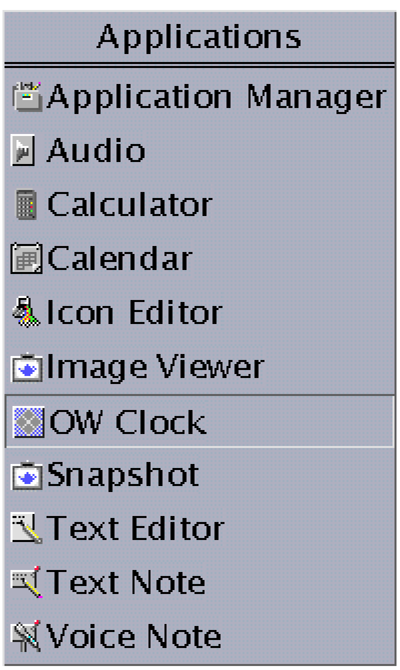

Figure 63: Starting Snapshot continued.

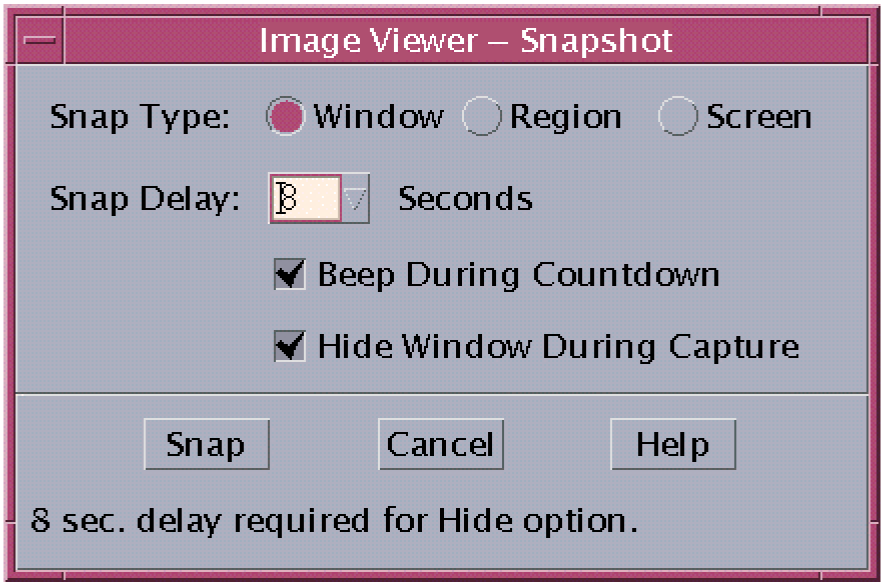

Figure 64: Setting up Snapshot Features.

Fill out the pop-up according to Figure 64.

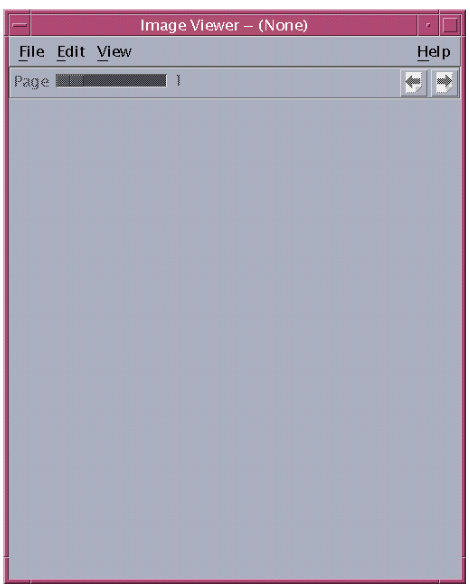

Figure 65: Snap Shot File Manager.

Left click on Snap, and then left click on the inverter image before the beeping ends. After some time the Snapshot file manager should display an image like Figure 66.

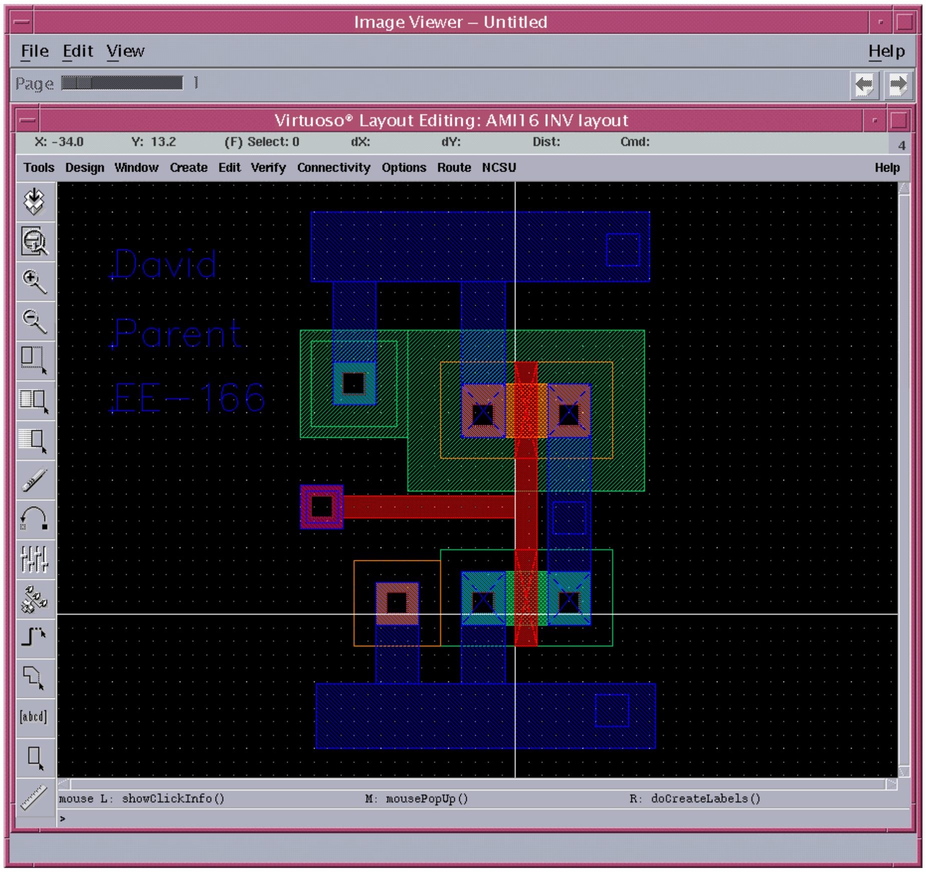

Figure 66: The image of the inverter.

In the Snapshot file manager goto File... Save as. A pop-up like Figure 67 should appear.

Make sure you select TIFF as the image format. Enter in the name of the image file you want to save. Make sure you enter in the .tiff extension like in Figure 67.

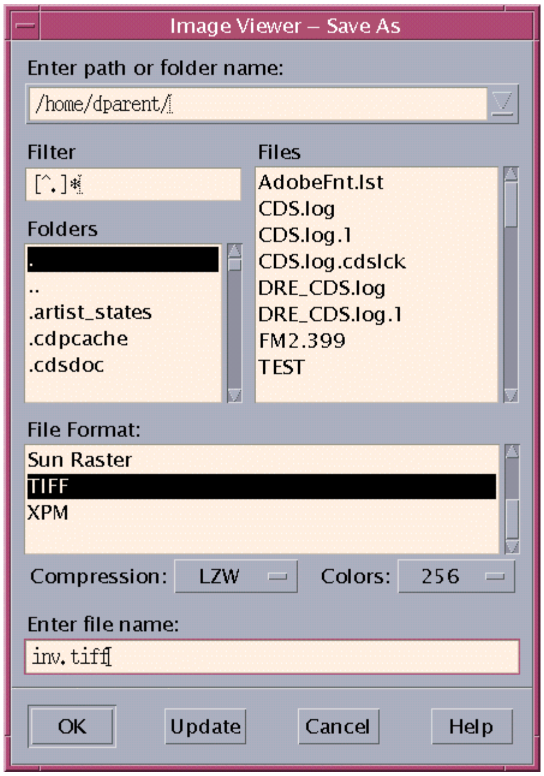

Figure 67: Saving the image.

Start the file manager by right clicking anywhere on the screen that is not an application. You should see a pop-up like in Figure 62. Goto Files... File Manager to start the file manager. You should get a pop-up like Figure 68

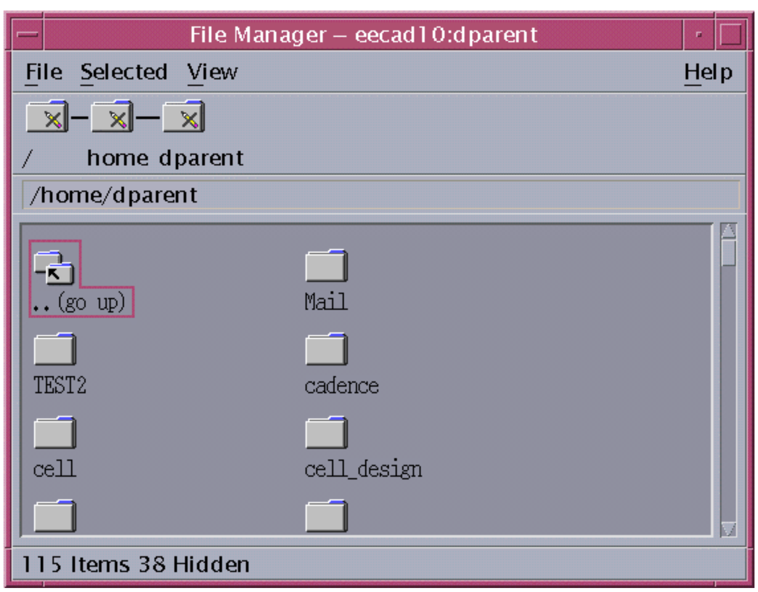

Figure 68: Starting the file manager.

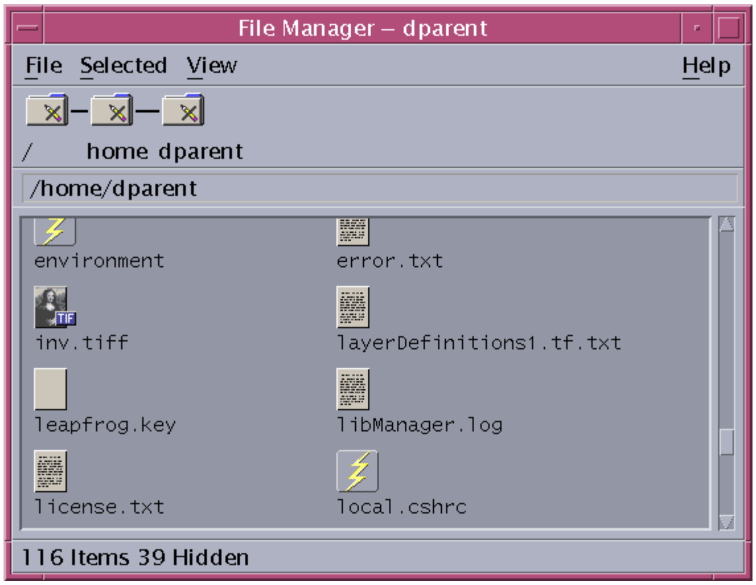

Figure 69: File manager showing TIFF file.

Scroll down until you see your inv.tiff image like in Figure 69.

In the file magager window goto file... open floppy like in Figure 70.

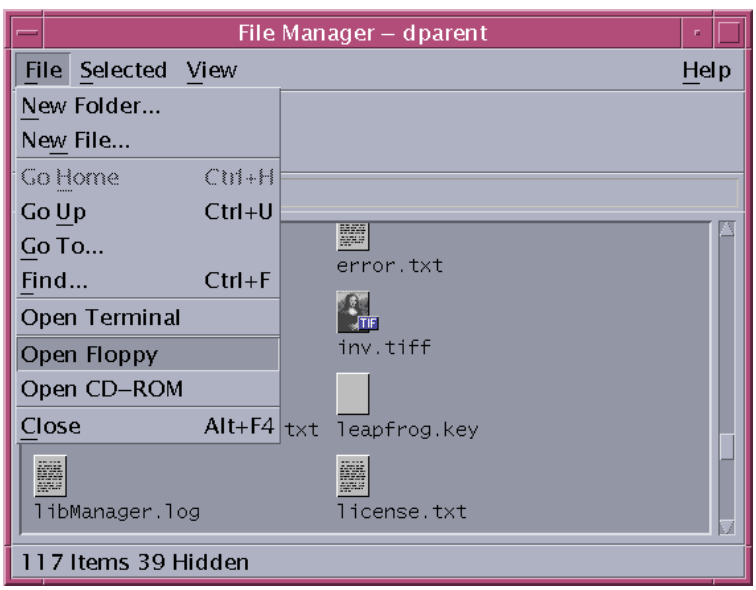

Figure 70: Opening up the floppy drive.

Draw a rectangle around the figures you wan to copy and drag an drop them into the floppy window like in Figure 71. Note: Figure 71 is showing more files than you will have if you follow this tutorial.

Now you can print the TIFF image or import it into Power Point or Word, for a professional looking document. You could even start writing Cadence Tutorials yourself!

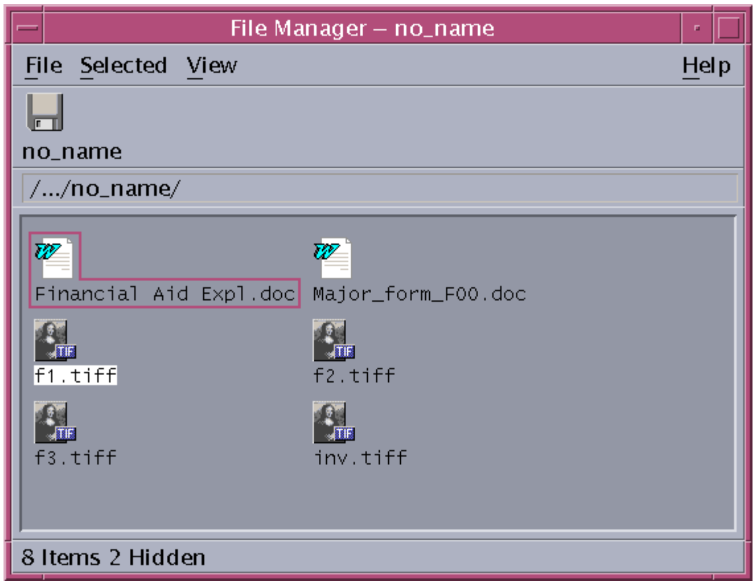

Figure 71: The floppy drive with the inverter images.