

SAN JOSE STATE UNIVERSITY
College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING

EE270– 01

Advanced Logic Design

Spring 2007

This Green Sheet contains information about various aspects of EE 270 course. Please read it carefully and retain and refer to it for answers to all your questions regarding course **schedule**, **grading**, and **policies** throughout the term.

Course Information

Instructor: Dr. Modarres

Class Hours: MW 18:00 – 19:15, Room Sci. 253.

Office Hours: MW 19:15 – 19:45, Room Sci. 253/Eng. 351.

Course Description

Advanced topics in logic design include discussion of combinational and sequential logic, synchronous and asynchronous design, and testability. Topics from contemporary computer systems will be used extensively, in parallel to the theory, as practical application of logic design. Concepts will be generalized during the course of instruction, and reinforced by independent reading assignments. Detailed homework assignments and analysis and design problems will be used to help the learning process.

Who Should Take This Course

Students who already have a background in logic design and are seeking to enhance their knowledge in advanced topics in computer and digital design.

Prerequisites

- A course in logic design and/or computer organization.
- Knowledge of C/C++ languages and Verilog HDL language.

References

Contemporary Logic Design by Randy H. Katz and Gaetano Borriello, 2005.

Digital Logic Circuit Analysis and Design by V. Nelson and H, 1995.

Digital Principles and Design by D. Givone, 2003.

Asynchronous Circuit Design by Chris J. Myers, 2001.

“Verilog HDL,” by S. Palnitkar, SunSoft Press. An introductory guide to Verilog HDL.

Course Policies

This course employs **strict no-exception policies**. That is, such policies cannot be changed to accommodate any student's personal, professional, academic, or financial needs, irrespective of the reasoning. It is therefore important to read the course policies carefully and to make sure that they fit student's particular academic, professional, financial, and personal situation.

Course Topics

Lectures will cover the following set of topics, as time permits. Reading assignments will be selected from the related material, assigned or handed out. Detailed schedule of readings and assignments will be communicated to the students throughout the semester. Presented material will be adjusted to better fit students' background and needs.

- Combinational logic and its simplification
- Synchronous sequential design
- Asynchronous sequential design
- Design for testability
- Special topics and application examples in digital system design
- Specification of logic and description languages.

Grading

Following weightings are used for various performance measures towards student's overall grade:

- 35% for midterm exam.
- 45% for a comprehensive final exam.
- 20% for homeworks and design problems.

More on Course Policies

Following policies are developed to be fair to and to treat all students in this course in exactly the same manner, as well as to remove any ambiguity on course policies.

- Students who are absent from class are responsible for obtaining related course material, assignments, and schedule updates. Lectures will not be repeated for those who are absent from class.
- Homeworks will be collected for partial and rough grading. **Homeworks** are due **only in class** and **only in hard copy form**. Late homeworks receive partial credit, 25% less per class session, without any exception. No late homework will be accepted after solutions are distributed or discussed.
- Homeworks should be neat and readable. Typed homeworks receive up to an additional 10% of the grade as extra credit.

- All material covered in class *and* assigned readings will be tested on. Exams are closed book with use of a single summary information sheet allowed. Use of non-programmed calculator is permitted in exam sessions.
- Students are expected to answer exam questions on their own and independently. No hint is provided and no help is given during the test to either guide the students thru the solution or provide any opinion on correctness of a solution. No formula will be provided to students who have forgotten to learn or write proper information on their information sheet.
- Students are responsible for clarity and comprehensiveness of their solutions; points may be lost if a solution is not totally clear or is illegible. Credit is given for correct application of formulae and concepts leading to correct result.
- Grades are quantized for each problem or sub-problem, in homeworks and exams. Full grade will be given to correct approach and correct answer. No credit is given for mere writing of formulae when they have not been applied correctly.
- **No re-grading** of homework or exam will be accommodated after the paper is returned to the student. Student may appeal only if an obvious mistake in grading is observed.
- **No make-up** test or homework will be given under any circumstance. If a student misses a homework or a test due to an emergency, the related grade may be distributed over the rest of student's grades upon presentation of proof of the emergency; otherwise a grade of zero is assigned for that particular performance factor. Any timing conflict with student's academic, personal, or professional matter is not considered an emergency.
- **No grade of I** will be given for poor performance or schedule conflict with student's personal, professional, or academic matters. Grade of I can be assigned if the student misses the final exam due to a (medical) emergency with solid proof, in which case the student should take the test in the following term, possibly with a different instructor and probably based on a different set of covered material.
- **No late drop** will be signed in the second half of the term without proof of an unexpected and irresolvable situation.
- **Grading is very strict** in this course. Your **final grade is determined only by your performance in this course** using previously specified weightings. In particular, your possible disqualification from school or financial aid or any other personal or professional matter has **no impact**, whatsoever, on your final grade.
- Final grades cannot be posted or communicated through e-mail. Please contact Records' Office for your final grade.

Class Etiquette

Please observe the following:

- Attend the class on time and plan on staying for the duration of the class.
- Plan on turning your cell phone off in class, or place it on mute.
- Refrain from speaking to your classmates in class.
- Refrain from consuming food in classroom.

EE Honor Code

Cheating in any form or shape will not be tolerated and may lead to a grade of F for the course and reporting to the department. Please refer to EE honor code for further information.

Honesty and Respect for Others and Public Property

EE HONOR CODE

Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor.”*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student’s second offense in any course will result in a department recommendation of suspension from the University.*