SAN JOSE STATE UNIVERSITY

Electrical Engineering Department

Semester: Fall 2007
Course: EE 256, ***Programmable DSP Architecture and Applications***
Class meetings:

Instructor:
Office:
Phone:
Office hours:

Course Description

Implementations of DSP algorithms using programmable DSP architectures. Internal DSP architectural requirements for a DSP device, system level hardware/ software design, and applications of DSP architectures.

Text

Singh, A. and Srinivasan, S., Thomson, 2004.

References

1. Higgins, R.J. "Digital Signal Processing in VLSI", Prentice-Hall, 1990.

2. Strum, R., and Kirk, D., "First Principles of Discrete Systems and Digital Signal Processing", Addison Wesley, 1988.

3. Bateman, A. and Yates, W. "Digital Signal Processing Design", Computer Science Press, 1989.

4. Texas Instrument "Digital Signal Processing Applications with the TMS320 Family", Prentice-Hall, 1988.

5. Texas Instruments "TMS320C5X User's Guide", 1990.

6. El-Sharkawy, M. ,"Real Time Digital Signal Processing with Motorola's DSP56000 Family", Prentice-Hall, 1990.

7. Embree, P.M. and Kimble, B. ,"C Language Algorithms for Digital Signal Processing", Prentice-Hall, 1991.

8. Texas Instruments, "Linear Circuits: Data Conversion, DSP Analog Interface, and Video Interface", 1992.

9. Chassaing, R. and Horning, D. W. , “Digital Signal Processing with the TMS320C25”, Wiley, New York, 1990.

10. Chassaing, R. and Horning, D. W. , “Digital Signal Processing with C and the TMS320C30”, Wiley,
11. New York, 1992.

12. Lapsley, P. etal , “DSP Processor Fundamentals: Architectures and Features”, IEEE Press, 1997.

13. Math Works, "The Student Edition of MATLAB with DSP Toolbox", Prentice-Hall, 1992 or later.

Laboratory References

14. Code Composer Studio User's Guide (SPRU328B, 1599 KB - Updated: 03/28/2000)

15. DSP Glossary (SPRU258A - Updated: 09/01/1997)

16. PCI2040 EVM Implementation Guide (SCPU004, 142 KB - Updated: 10/22/1999)

17. TMS320 DSP Algorithm Standard API Reference (SPRU360B, 301 KB - Updated: 10/30/2000)

18. TMS320 DSP Algorithm Standard Developer's Guide (SPRU424A, 143 KB - Updated: 08/06/2001)

19. TMS320 DSP Algorithm Standard Rules and Guidelines (SPRU352D, 390 KB - Updated: 01/31/2001)

20. TMS320 DSP/BIOS User's Guide (SPRU423, 1807 KB - Updated: 06/30/2000)

21. TMS320C5000 DSP/BIOS Application Programming Interface (API) Ref Guide (SPRU404C, 2199 KB - Updated: 05/31/2001)

22. TMS320C548/549 Bootloader & ROM Code Examples Techn. Reference (SPRU288A, 305 KB - Updated: 05/03/2000)

23. TMS320C54x Assembly Language Tools User's Guide (SPRU102E, 1235 KB - Updated: 04/30/2001)

24. TMS320C54x C Source Debugger User's Guide (SPRU099D - Updated: 07/31/1998)

25. TMS320C54x Chip Support Library API Reference Guide (SPRU420, 1229 KB - Updated: 05/30/2000)

26. TMS320C54x Code Composer Studio Tutorial (SPRU327C, 1045 KB - Updated: 03/31/2000)

27. TMS320C54x DSKplus Adapter Kit (SLAU030, 581 KB - Updated: 05/11/1999)

28. TMS320C54x DSKplus DSP Starter Kit User's Guide (SPRU191 - Updated: 04/01/1996)

29. TMS320C54x DSP Applications Guide Reference Set Volume 4 (SPRU173 - Updated: 10/01/1996)

30. TMS320C54x DSP CPU Reference Guide (SPRU131G, 2156 KB - Updated: 03/31/2000)

31. TMS320C54x DSP Enhanced Peripherals Ref Set, Vol 5 (SPRU302, 1277 KB - Updated: 05/30/1999)

32. TMS320C54x DSP Functional Overview (Addendum to 'C54x Data Sheets) (SPRU307A, 201 KB - Updated: 05/31/2000)

33. TMS320C54x DSP Library User's Guide (SPRU518, 277 KB - Updated: 03/31/2001)

34. TMS320C54x DSP Mnemonic Instruction Set Reference Set Volume 2 (SPRU172C, 1096 KB - Updated: 01/31/2001)

35. TMS320C54x DSP Programmer's Guide (SPRU538, 231 KB - Updated: 06/30/2001)

36. TMS320C54x DSP Reference Set Volume 3: Algebraic Instruction (SPRU179C, 1115 KB - Updated: 01/31/2001)

37. TMS320C54x DSP/BIOS User's Guide (SPRU326C, 1238 KB - Updated: 03/31/2000)

38. TMS320C54x Evaluation Module Installation Guide (SPRU134 - Updated: 09/14/1995)

39. TMS320C54x Evaluation Module Technical Reference (SPRU135 - Updated: 10/01/1995)

40. TMS320C54x Optimizing C/C++ Compiler UG (SPRU103F, 751 KB - Updated: 04/30/2001)

Course Learning Objectives

	Course Learning Objective (CLO)	***Program Outcomes (POs)**
1.	Ability to analyze DSP algorithms and operations for a DSP processor implementations	1, 2
2.	Ability to use MATLAB for DSP analysis and design	1, 2, 3
3.	Ability to determine architecture and hardware to implement DSP operations and algorithms	1, 2
4.	Ability to analyze a programmable DSP device	1, 2
5.	Ability to understand software model for a DSP device	1, 2
6.	Ability to use DSP software development tools	3
7.	Ability to implement DSP algorithms for filters and controllers	1, 2, 3
8.	Ability to develop assembly code for a digital filter	1, 2, 3
9.	Ability to understand interfacing serial converters to a programmable DSP device	1, 2
10.	Ability to analyze synchronous serial interface	1, 2
11.	Ability to program a multi-channel buffered serial port	1, 2, 3
12.	Ability to implement a real-time DSP scheme	1, 2, 3
13.	Ability to evaluate computational accuracy in DSP implementations	1, 2
14.	Ability to understand quantization, truncation, rounding, overflow, and saturation errors in DSP implementations	1, 2
15.	Ability to implement FFT algorithms for spectrum analysis	1, 2, 3
16.	Ability to interface memory to a programmable DSP device	1, 2
17.	Ability to interface data converters to a programmable DSP device	1, 2

***Program Outcomes (POs)**

1) Students will be able to base analysis, problem solving and design on core advanced EE theory.
2) Students will be able to develop deeper understanding of an area of concentration in their graduate programs.
3) Students will be able to apply modern tools for computations, simulations, analysis, and design.
4) Students will be able to communicate engineering results effectively.

Grading

Homework/ Labs	20%
Midterm Exam	20%
Final Exam	30%
Lab Project	30%

Standard grading method will be used to assign letter grades. For instance an overall score of 90% will be assigned a letter grade of A-. Any adjustment to this scheme of grading, if necessary, will be described in the class.

Examinations

Midterm: **Class Announcement**
Final: **University Schedule**

EE 256 LECTURE TOPICS
FALL 2007

1. Introduction to Digital Signal Processing Operations (Chapter 2)
The Sampling Theorem and Digital Signal Sequences
Frequency Response and FIR/ IIR Filters
DFT and FFT
Computer Based Tools for DSP Analysis and Design
Homework/Lab*:* *Using MATLAB for DSP Analysis and Design*

2. Architectural Requirements of a DSP Device (Chapter 4)
Architectures and hardware to implement DSP operations and algorithms
Comparison of various DSP architectures in use
Homework

3. Programmable DSP Devices (Chapter 5)
Architectural Analysis of a DSP Device
The Instruction Set and the Addressing Modes
Writing Assembly Code for Applications
Homework

4. DSP Implementation Tools (Chapter 6)
DSP Software Development Tools: Compiler,
Assembler, Linker, Simulator, and Debugger
Homework/Lab*:* *Using TMS320C5000 Software Development Tools*

5. Software Implementations of DSP Algorithms (Chapter 7)
Assembly Code Implementations: FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controllers, Adaptive Filters, and Nonlinear Operations.
Homework/Lab*:* *Developing Assembly Code for a Digital Filter*

MIDTERM

6. Interfacing Serial Converters to a Programmable DSP Device (Chapter 10)
Synchronous Serial Interface between the DSP and an AIC
A Multi-channel Buffered Serial Port (McBSP)
The McBSP Programming
An Analog Interface Circuit (AIC)
Homework/ Lab Project*:* *Implementing and Demonstrating a Real-time DSP Scheme*

7. Computational Accuracy in DSP Implementations (Chapter 3)
The DSP System Model
Quantization, Truncation, Rounding, Overflow, and Saturation Errors in DSP Implementations
Homework

8. Software Implementations of FFT Algorithms (Chapter 8)
Spectrum Analysis
Homework/ Lab Project*:* *Implementing an FFT Algorithm for Spectrum Analysis*

9. Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices (Chapter 9)
Memory Interfacing, A/D and D/A Interfacing
Homework

FINAL