

San José State University
Electrical Engineering Department
EE287, CMOS ASIC Design, Fall 2009

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Office Hours: T&TH 3:30-5:30pm Other days by appointment
Class Days/Time: MW 9:00-10:15PM
Classroom: E 343

Prerequisites:

EE270. (Students should be able to perform Verilog designs before taking EE287)

Web Page

[Http://www.engr.sjsu.edu/mjones](http://www.engr.sjsu.edu/mjones)

Blackboard <http://sjsu6.blackboard.com>

Course Description

EE287 is an overview of CMOS ASIC concepts and design. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by a design project. Team work will be stressed.

Course Goals and Student Learning Objectives

- Prepare students to be productive members of an industrial ASIC design team
- Prepare students for graduate projects involving digital circuits using ASIC techniques and synthesis
- Provide an understanding of the ASIC life cycle
- Provide an opportunity developing teamwork skills
- Provide an environment where students learn to think critically
- Provide an environment where students learn to enjoy the learning and designing process
- Have students internalize the culture of the design engineer

Course Objectives (Outcomes):

To be productive members of an industrial ASIC design team, students should be able to:

- Practice and demonstrate critical thinking

- Understand requirements and translate them to a high level design language
 - (Verilog is a required prerequisite and not taught in EE287).
- Understand capabilities and limitations of CMOS logic and adjust designs to best use CMOS ASIC technologies.
- Demonstrate common ASIC team rules, and articulate the purposes for such rules.
- Demonstrate an ability to use industry synthesis tools to achieve desired project objectives.
- Demonstrate an understanding of module interfaces, pipe lining, design for test, test pattern generation, and BIST.
- Modify designs to achieve performance objectives.
- Perform an ASIC design from requirements to timing verification

Critical thinking has been described as:

A person who thinks critically can ask appropriate questions, gather relevant information, efficiently and creatively sort through this information, reason logically from this information, and come to reliable and trustworthy conclusions about the world that enable one to live and act successfully in it. ... critical thinking mimics the well-known method of scientific investigation: a question is identified, an hypothesis formulated, relevant data sought and gathered, the hypothesis is logically tested and evaluated ... [1]

Students who can think critically can:

- Determine what information is required to achieve an objective, find that information, and apply it
- Create designs from limited information
- design test benches that can prove that a design meet a specification
- identify design errors, and adjust a design to meet specifications

A course goal is students learn to enjoy the CMOS ASIC design team experience through a *hands on* approach.

Student Preparedness

Students are expected to have previously taken a course covering Verilog and digital logic design. A course on CMOS devices and circuit design is helpful, but not required. Students will be given a vague specification for the design project, and are expected to perform research and form clarifying questions to complete the project.

Outcome Assessment (Grading):

- Homework (20%): Homework will consist of a mix of analysis and design problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. In addition to homework, online assessments are included in the homework scores. Students are encouraged to work in groups after homework 2, but each student needs to try to solve the homework problems, before group meetings. Each student in a group must submit individual homework assignments on the eCampus system until formal groups are set up on the system. After that, the assignments will be presented to groups, and must be submitted as a group. When the group submission is made, only one submission is required for the entire group. Online assessments must be completed individually.
 - All homework shall be submitted individually on the eCampus system. (you can access the system at <http://sjsu6.blackboard.com>)
 - The eCampus document upload only works from a windows based machine. If you use another

- operating system, you can upload from the academic success center located in the Clark building
- You can scan paper documents at the academic success center
- Your user ID is your SJSU student number
- Your password will be given in class
- Please login and change your password
- Developing professional discipline such as on time homework submission is expected and required. Homework scores are modified according to the following schedule:
 - 100% Early or on time
 - 50% Late up to 1 week
 - 0% Late one week or more (Not accepted after 1 week late)
- 50% of the homework grade is a class project. This project is a design problem. The specifications are found on the web. Teams of 2-3 people are expected to work on the design problem. To discourage *borrowing* of other designs, the successful designs will be run through a recursive difference engine, and the score will be reduced by the similarity to other submitted designs. Both designs will be penalized.
- Students should have already taken a logic/Verilog design class (such as EE270/271). EE287 will not teach the Verilog design principles required for the project. The project will tie together a number of the ASIC principles taught in the class.
- Midterm (35%): Covers the first half of the semester. A study guide is available on the web site with typical questions. Several past midterms are also posted on the web. All EE287 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.
- Final Exam (45%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. All EE287 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.

Grading Scale

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.999%	varies for + and -
C+	78-79.99999%	No C or C- grades are given.
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available.

Honor Code

Students should know that the University's Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Adherence to the San Jose State Honor Code is required in EE287.

San Jose State University Electrical Engineering Department EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*

A student's second offense in any course will result in a Department recommendation of suspension from the University.

Homework Due Dates

Date	Which
31-Aug	ACC 1
02-Sept	HW 1
09-Sept	ACC 2
14-Sept	Choose Groups
16-Sept	HW 2
21-Sept	ACC 3
28-Sept	Fifo HW
30-Sept	ACC 4
07-Oct	HW 3
21-Oct	HW 4
26-Oct	Engine HW
28-Oct	HW 5
04-Nov	ACC 5
16-Nov	ACC 6
18-Nov	Proj Simulation
23-Nov	HW6
30-Nov	Proj Synthesis

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at <http://info.sjsu.edu/web-dbgen/narr/socfall/rec-298.html>. Information about late drop is available at <http://www.sjsu.edu/sac/advising/latedrops/policy/>. Students should be aware of the current deadlines and penalties for adding and dropping classes.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with

disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Course plan

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews. The items labeled ACC are eCampus assessments (online quizzes) each students should perform online.

Date	Topic	pdf readings
24-Aug	intro296.pdf, CMOSASIC2000.pdf, CMOS gate review	cmosgr.pdf
26-Aug	Delay in CMOS overview	cmosdelay.pdf
31-Aug	Cell types in 260	260c_pri_e.pdf
02-Sept	Latches and FFs	latches.pdf
07-Sept	No Class – Labor Day	
09-Sept	The clock cycle and paths	clkcycle.pdf
14-Sept	Working with latches	discussion
16-Sept	Fifos	
21-Sept	Fixing Long Paths and Races	examples, discussion
23-Sept	Working with timing	
28-Sept	A real library	260c_highpri_e.pdf
30-Sept	Delay models	260c_pri_e.pdf
05-Oct	Timing closure	
07-Oct	Clock distribution networks	
12-Oct	Midterm Review	Study Guide

14-Oct	Midterm	
19-Oct	Product debug requirements	
21-Oct	Project function discussion	
26-Oct	Multiple Clock domains	
28-Oct	I/O pads and packaging	260e_mac_e.pdf I/O pages, P16,17
02-Nov	Power and Ground pins	
04-Nov	Power estimation	
09-Nov	Floor plan and impacts	
11-Nov	No Class -- Veterans Day	
16-Nov	Manf and test. D algorithm	faults.pdf
18-Nov	Scan based testing	
23-Nov	Bist -- Concepts	
25-Nov	No Class -- Thanksgiving	
30-Nov	Bist -- Logic	
02-Dec	Bist -- Memory	
07-Dec	Review for Final	

Text Book

There is no text book for EE287. It is taught from notes, and lecture materials.