

San José State University
Electrical Engineering Department
EE275, Advanced Computer Architecture, Fall 2009

Instructor:	H. Modarres
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Office Hours:	MW 20:45-20:15
Class Days/Time:	MW 19:30-20:45
Classroom:	CL 226
Prerequisites:	EE 270 (Advanced Logic Design)

Web Page

<http://www.engr.sjsu.edu/electrical/>

Course Description

This is the first graduate course on computer architecture. Topics discussed include: instruction set architectures, instruction pipelining, instruction-level parallelism, memory hierarchy including cache and virtual memory, I/O and storage systems, and interconnection networks.

Course Goals and Student Learning Objectives

1. Understand the basic elements of a modern digital computer system.
2. Understand and analyze performance of a computer system.
3. Understand the concepts of instruction-level parallelism.
4. Understand the design and analysis of a pipelined processor.
5. Understanding fundamentals of memory hierarchy.
6. Learning techniques for optimization of a memory system.
7. Understand and analyze the performance of a storage system.
8. Design of a reliable storage system for high-speed processors.
9. Understanding fundamentals of computer interconnections.
10. Understanding various interconnection networks and computer clusters.

Required Texts/Readings

Textbook

J. Hennessy and D. Patterson, Computer Architecture, 4th Ed., Morgan Kaufmann, 2007.

Other Readings

1. D. Patterson and J. Hennessy, Computer Organization and Design, Morgan Kaufmann.
2. S. Palnitkar, *Verilog HDL*, SunSoft Press.

Other material

Handouts will be provided in class.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the class and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. [Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html](http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html). [Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/](http://www.sjsu.edu/sac/advising/latedrops/policy/). Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

Assignments	15%
Projects	15%
Midterm exam	30%
Final exam	40%
Total	100%

Notes:

- a. All exams are closed book and notes.
- b. Homework assignments will be given regularly and are due one week from the assigned date.

EE 275: Advanced Computer Architecture, Semester: Fall 2009, Course Schedule

Week	Date	Lecture Topics
1	Aug 24,26	Green sheet. Grading policy. Introduction to computer systems
2	Aug 31, Sep 2	Performance evaluation and performance equations
3	Sep 9	MIPS architecture
4	Sep 14,16	Instruction-level parallelism and dependence analysis
5	Sep 21,23	Pipelined processor design and speculation
6	Sep 28,30	Fundamentals of memory hierarchy
7	Oct 5,7	Cache architecture
8	Oct 12,14	Virtual memory design
9	Oct 19,21	Review session, mid-term exam
10	Oct 26,28	Optimization of memory systems
11	Nov 2, 4	Fundamentals of storage system design
12	Nov 9	Disk mechanics and performance equations
13	Nov 16,18	Redundancy and RAIDs
14	Nov 23,26	Interconnection networks
15	Nov 30, Dec 2	Network topologies and clusters
16	Dec 7	Review session
	Dec 16	Final exam: 19:45-22:00

University Policies

Academic integrity

Students should know that the University's [Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf). Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for [Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE Department honor code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University. A student’s second offense in any course will result in a Department recommendation of suspension from the University.