

San José State University
Charles W. Davidson College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING
EE271 - Advanced Digital System Design and Synthesis

Instructor: Prof. Thuy T. Le
Office Location: Engineering Building, room 369
Telephone: (408) 924-5708
Fax: (408) 924-3925
Email: Thuy.Le@sjsu.edu
Web Page: www.engr.sjsu.edu/tle/
Office Hours: Monday & Wednesday: 15:00 – 17:30
Class Days/Time: Monday & Wednesday, 18:00 – 19:15
Classroom: Engineering Building, room 345
Prerequisites: EE270 - Advanced Logic Design or equivalent experience. Background in integrated circuit design is helpful. Must have self-motivations in learning EDA tools and Verilog HDL

Faculty Web Page

Course information and materials such as course syllabus, tutorials, journal/proceeding papers, homework/lab assignments and solutions, office hours, special announcements, etc. will be posted on my web page at www.engr.sjsu.edu/tle/. Students are responsible for regularly checking the web page for the information.

Course Description

This course covers topics in the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of logic and system design, synthesis, and optimization for area, speed and power consumption. The course enables students to apply their knowledge for the design of advanced digital hardware systems with corresponding EDA tools. Verilog HDL will be used for simulation and synthesis of the homework assignments and final design project.

Student Learning Objectives

Upon successful completion of this course, students will be able to:

- LO1. Design and manually optimize complex combinational and sequential digital circuits
- LO2. Model combinational and sequential digital circuits by Verilog HDL
- LO3. Design and model digital circuits with Verilog HDL at behavioral, structural, and RTL levels

- LO4. Develop testbenches to simulate combinational and sequential circuits
- LO5. Perform functional and timing verifications of digital circuits
- LO6. Perform static and dynamic timing analysis with false paths and hazards
- LO7. Synthesis combinational and sequential circuits with trade-offs in timing, area, and power
- LO8. Improve timing performance of a digital circuit by using pipelining and superscalar techniques
- LO9. Design various advanced/high-speed digital arithmetic circuits including addition, subtraction, multiplication, and division of integer, fraction, unsigned, signed, and floating-point numbers in various number systems
- LO10. Estimate area and timing delay of various arithmetic circuits based on various implementation algorithms
- LO11. Estimate power distribution and power consumption of digital circuits

Required Texts, Readings, and EDA Tools

Textbooks

- EE271 Lecture Notes by Thuy T. Le
Each chapter will be posted on the class website two weeks before the start of the lecture, and will be deleted once the lecture discussion is started in class.
- “Computer Arithmetic” by David Goldberg, Xerox Palo Alto Research Center - Appendix A of Computer Architecture – A Quantitative Approach by John L. Hennessy & David A. Patterson - Morgan Kaufmann Publishers, Inc. (available on class website)

Additional Readings (optional)

- Any “Verilog Language” books/notes. Below are few on-line documents:
http://www.doulos.com/knowhow/verilog_designers_guide/
http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html
- Self-research of additional reading materials based on topics covered in lecture notes.

EDA Tools

- Synopsys VCS (required): Available on SJSU Cadence Lab
- Synopsys Design Compiler synthesis tool (required): Available on SJSU Cadence Lab
- Silos (optional): Available on class website
- Any other Verilog simulator such as ModelSim PE (optional): Can be downloaded at www.model.com/downloads/evaluations.asp

UNIX Accounts on Cadence Laboratory

- Rooms E289 and E291 are Cadence laboratories installed with Cadence and Synopsys software tools. Each registered SJSU student should automatically have a UNIX account. If you do not know your login name and password (or having problems with the account), you can find out at <https://unix.engr.sjsu.edu/wiki/doku.php>
- For Unix tutorial materials and other documents related to Cadence laboratory, please consult Prof. Parent’s website at <http://www.engr.sjsu.edu/dparent/>

Classroom Protocol

EE271 students understand that professional attitude is necessary to maintain a comfortable academic environment in the classroom. For examples:

- Students will put their cell phones in quiet/vibration mode during the lecture.
- Students understand that drinking water, juices, etc. during the lecture is acceptable but NOT eating.
- Students will not skip the lecture and then ask the instructor to summarize the lecture later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.
- Students will come to the class on time and leave the class at the end of the lecture.
- Students will consult the course syllabus for class policies and requirements before requesting the instructor for any special considerations and/or exceptions
- To minimize possible tension during the exams, students are requested to follow the exam rules closely.
- Students will work on the project and report by their own and will not share the work with other students
- Students understand that long-term learning is their responsibility and will always keep it up.

If you need to communicate with me, please try to see me in person during the office hours. If you must send me an email, please clearly specify your full-name, course, section, etc. I will not respond to email that I do not know the author or emails that have no manners.

Dropping and Adding Policies and Procedures

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at <http://info.sjsu.edu/web-dbgen/narr/soc-fall/>. Information about late drop is available at <http://www.sjsu.edu/sac/policies/latedrops/policy/>. Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

Lectures

The course will follow the selected subjects as listed on the course description. Additional theory and examples will be given and discussed in class as much as time permits. Please note that lecture materials are NOT solely based on the required text and so students are responsible for following up the lecture in order to prepare themselves for the exams.

- Students are responsible for the reading the text, handouts, lecture presentations, etc.
- Students are responsible for following up and keeping track of the in-class lecture materials.
- Students are responsible for finding and reading additional books, papers, examples, etc. in order to gain more understanding of the materials discussed in the lectures.
- Students are responsible for self-learning and using of CAD tools for assigned homework problems, lab exercises, projects, and for lecture discussions.

Exams and Final Design Project

There will be one midterm exam, a comprehensive final exam, and an individual final design project with report. The dates of the midterm and final exams are listed as below. Since make-up exams will NOT be allowed, please make sure that you are able to attend all exams at the indicated scheduled dates and times (from the beginning of the semester) in order to register for the course.

- Midterm exam: Wednesday October 14, 18:00 – 19:15
- Final exam: Monday December 14, 17:15 - 19:30
- Final project report due: Thursday December 17, 2009, before 11:00AM
- All exams are closed-book exams.
 - One sheet (double-side) of hand-written notes is allowed for the midterm exam and two sheets of hand-written notes are allowed for the final exam.
 - Summary (printed) of Verilog keywords will be provided.
 - Some complex information will be provided if needed.
 - Only basic calculators are allowed.
- There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for making-up exams).
- Exam solutions will be discussed in class after the exam dates. Written solutions will NOT be distributed.

Homework Assignments and Lab Exercises

Eight to ten homework assignments and/or lab exercises will be given periodically and will mostly be due in one week from the assigned date. Homework/lab solutions will be made available after the due date.

- NO late submission will be accepted (absolutely!).
- There is no make-up homework/lab

To get credit for your homework/lab assignments, submissions must be neat, clean, and must be done professionally and seriously. Your official name (not nickname), course #, and homework # must be visibly shown on each assignment.

Grading Policy

The overall course grades (letter-grades) will be assigned based on the overall class distribution or grading standard, whichever that is better. If grading standard is used, overall score above 90% will be distributed for A and A+, 80% to 89% will be distributed for B, B+, A-, 70% to 79% will be distributed for C, C+, B-, and 60% to 69% will be distributed for D, D+, C-. If overall class distribution is used for determining grade, overall scores above class average will be distributed for B, B+, A-, A, A+ and overall scores below class average will be distributed among B-, C+, C, etc. The weights of work assignments are listed as below:

Homework assignments and lab exercises:	10%
A closed-book midterm exam:	20%
A closed-book comprehensive final exam:	45%
An individual final design project and project report:	25%

University Policies

Academic integrity

Students should know that the University's [Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf). Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for [Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please see me as soon as possible during my office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE Honor Code - Honesty and Respect for Others and Public Property

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student's second offense in any course will result in a Department recommendation of suspension from the University.

Course Schedule (tentative – will be updated regularly)

Week	Date	Topics
1	08/24/2009	Course syllabus – Class policies
	08/26/2009	Lecture Note #1: Introduction to Advanced Digital System and Logic Design
2	08/31/2009	Appendix 1 – Review of Combinational Logic
	09/02/2009	
3	09/07/2009	Labor Day – Campus Closed
	09/09/2009	Appendix 2 – Review of Sequential Circuits
4	09/14/2009	Appendix 2 (continue)
	09/16/2009	Lecture Note #2: Verilog HDL Models and Synthesis
5	09/21/2009	Lecture Note #2 (continue)
	09/23/2009	
6	09/28/2009	Lecture Note #2 (continue)
	09/30/2009	
7	10/05/2009	Lecture Note #3: Timing and Power Analysis
	10/07/2009	
8	10/12/2009	Lecture Note #3 (continue)
	10/14/2009	Midterm Exam: Wednesday October 14, 18:00 – 19:15
9	10/19/2009	Lecture Note #4: Synthesis and Optimizations
	10/21/2009	
10	10/26/2009	Lecture Note #5: Digital Arithmetic
	10/28/2009	
11	11/02/2009	Lecture Note #5 (continue)
	11/04/2009	
12	11/09/2009	Lecture Note #6: The Design of Addition and Subtraction Circuits
	11/11/2009	<i>Veteran's Day – Campus Closed</i>
13	11/16/2009	Lecture Note #6 (continue)
	11/18/2009	
14	11/23/2009	Lecture Note #6 (continue)
	11/25/2009	<i>Thanksgiving holiday – Campus closed</i>
15	11/30/2009	Lecture Note #7: The Design of Multiplication and Division Circuits

Week	Date	Topics
	12/02/2009	
16	12/07/2009	Lecture Note #7 (continue)
17	12/14/2009	Final Exam: Monday December 14, 17:15 - 19:30, ENGR345
	12/17/2009	Final Project Report: Thursday December 17, before 11:00AM