

San José State University
Department of Electrical Engineering
EE 229, Advanced Topics in Microelectronics, Section 01,
Fall, 2009

Instructor:	Saurabh Tiwary
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Office Hours:	Saturday 11:45 to 12:45
Class Days/Time:	S 9:00-11:45
Classroom:	ENG 232
Prerequisites:	EE 221

Course Description

The course focuses on different issues relating to designing practical analog / mixed-signal circuits. Topics that would be covered include: Analog VLSI, Mixed-Signal Circuit Design, Oscillators, Noise Analysis, Circuit Simulation Considerations, Phase Lock Loop Circuits, PLL metrics, Modeling Mixed Signal Circuits, ADC and DAC Converters, ADC Metrics, Sigma-Delta ADCs, Bandwidth and Accuracy in Sigma-Delta Converters, Decimation, and Statistical Design Considerations.

Course Goals and Student Learning Objectives

This course provides an introduction to design techniques and practical considerations while designing analog and mixed-signal (AMS) circuits in modern VLSI processes. The course begins with a review of transistors, parasitics and related models. It is followed by a review of circuit simulation techniques that are critical in evaluating the quality of a design. Techniques for design and analysis of oscillators are covered next. We then look at a phase locked loop circuit, both from a system as well as a circuits perspective. This is followed by an overview of circuit modeling aspects. In the latter half of the course, we look at the design of ADC and DAC blocks, again from both, a system and circuits perspective. Finally, we discuss statistical variations and the techniques to model and quantify their impact. The course concludes with an overview of the latest advances in AMS design.

GE/SJSU Studies Learning Outcomes (LO), if applicable

Upon successful completion of this course, students will be able to:

LO1 Demonstrate an understanding of the fundamentals of analog/mixed-signal design, including its principles, analysis and design.

LO2 Demonstrate the ability to apply the practice of Engineering in real-world problems.

Course Content Learning Outcomes

Upon successful completion of this course, students will be able to:

LO3 **Analyze** oscillator designs. (e)

LO4 **Identify, formulate and solve** common circuit simulation problems like DC, AC, transient and PSS analysis (n,o)

LO5 **Describe** the functioning of a phase locked loop (PLL). (e)

LO6 **Demonstrate** trade-offs in the design of PLLs. (k)

LO7 **Demonstrate** a functioning design of a PLL at the schematic level while working in a group. (d,k)

LO8 **Describe** different circuit modeling concepts relating to improving simulation speed. (k)

LO9 **Analyze** ADC and DAC designs. (e)

L10 **Describe** statistical design issues and different solutions to handle the problem. (m)

LO11 **Describe** modern advances in analog design and CAD (j)

LO12 **Interpret and report** on research papers in the form of powerpoint presentations (g)

ABET outcomes

The letters in parentheses in the course learning objectives refer to ABET criterion 3 outcomes satisfied by the course. These are listed below as a reference:

- (a) An ability to apply knowledge of mathematics, science, and engineering
- (b) An ability to design and conduct experiments, as well as to analyze and interpret data
- (c) An ability to design a system, component, or process to meet desired needs
- (d) An ability to function on multi-disciplinary teams
- (e) An ability to identify, formulate, and solve engineering problems
- (f) An understanding of professional and ethical responsibility
- (g) An ability to communicate effectively
- (h) The broad education necessary to understand the impact of engineering solutions in a global and societal context
- (i) A recognition of the need for, and an ability to engage in life-long learning
- (j) A knowledge of contemporary issues
- (k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice
- (l) Specialization in one or more technical specialties that meet the needs of companies
- (m) Knowledge of probability and statistics, including applications to electrical engineering

- (n) Knowledge of advanced mathematics, including differential and integral equations, linear algebra, complex variables, and discrete mathematics
- (o) Basic sciences, computer science, and engineering sciences necessary to analyze and design complex electrical and electronic devices, software, and systems containing hardware and software components

Required Texts/Readings

Readings

1. B. Razavi, "*Design of Analog CMOS Integrated Circuits*"
2. T.H. Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits*"
3. Vlach and Singhal, "*Computer Methods for Circuit Analysis and Design*"
4. Rudy van de Plassche, "*CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*"

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at <http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html>. Information about late drop is available at <http://www.sjsu.edu/sac/advising/latedrops/policy/>. Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

There will be three projects, one presentation and a final exam. Exams cover the assigned reading materials and class lecture notes. There will be no make-up exams (only in very special circumstances, both written excuse and official proofs are required for extraordinary exams). Exam solutions will be discussed in class after the exam dates and posted in the web site of the course. There will be one programming project on building a small circuit simulator. There will be two other projects, one each on design of PLL and ADC block. There will be one presentation assignment based on reading of a research paper.

Grades

Project 1	15%
Project 2	25%
Project 3	25%
Presentation	10%
Final exam	25%

Total 100%

Grading Percentage Breakdown

90% and above	A
89% - 85%	A-
84% - 82%	B+
81% - 79%	B
78% - 75%	B-
74% - 72%	C+
71% - 69%	C
68% - 65%	C-
64% - 62%	D+
61% - 59%	D
58% - 55%	D-
below 55%	F

University Policies

Academic integrity

Students should know that the University's [Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf). Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for [Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE 229 / Advanced Topics in Microelectronics, Fall 2009, Course Schedule

Course Schedule (Subject to change with fair notice as announced by instructor in class)

Week	Date	Topics, Readings, Assignments, Deadlines
1	8/29	Introduction/Overview
2	9/5	Circuit simulation basics (Project 1 out)
3	9/12	Oscillator design
4	9/19	Noise analysis
5	9/26	PLL design
6	10/3	PLL metrics (Project 2 out)
7	10/10	Circuit modeling – 1
8	10/17	Circuit modeling – 2
9	10/24	PLL modeling
10	10/31	ADC design - 1
11	11/7	ADC design – 2 (Project 3 out)
12	11/14	Variations (Presentation out)
13	11/21	Statistical Design
14	11/28	Thanksgiving
15	12/5	New trends in Analog / Mixed signal design
Final Exam	Check University Schedule	