

San José State University
Electrical Engineering Department
EE227, CMOS ASIC Design, Fall 2009

Instructor: Morris Jones
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Office Hours: T&TH 3:30-5:30pm Other days by appointment
Class Days/Time: T&TH 6:00-7:15PM
Classroom: E 343

Prerequisites: EE224

Web Page

[Http://www.engr.sjsu.edu/mjones](http://www.engr.sjsu.edu/mjones)
Blackboard <http://sjsu6.blackboard.com>

Course Description

EE227 is an introduction to large scale MOS design issues. It extends the digital concepts of EE224 to include mixed signal elements contained in all large scale integrated circuits. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by a design project. Team work will be stressed.

Course Goals and Student Learning Objectives

- Prepare students to be productive members of an industrial VLSI design team.
- Prepare students for graduate projects involving mixed signal circuits using design, analysis, layout, and verification.
- Provide an understanding of basic mixed signal design elements.
- Provide an opportunity developing teamwork skills.
- Provide an environment where students learn to think critically.
- Provide an environment where students learn to enjoy the design and learning processes.
- Have students internalize the culture of the design engineer.

Course Objectives (Outcomes):

To be productive members of an industrial mixed signal design team, students should be able to:

- Practice and demonstrate critical thinking
- Understand requirements and translate them to a system level building blocks.
- Understand capabilities and limitations of mixed signal CMOS elements and adjust designs to best use CMOS ASIC technologies.
- Demonstrate an ability to use industry tools to achieve desired project objectives.
- Modify designs to achieve performance objectives.
- Perform a mixed signal design from requirements through verification

- Demonstrate skills with a substantial project involving teamwork

Critical thinking has been described as:

A person who thinks critically can ask appropriate questions, gather relevant information, efficiently and creatively sort through this information, reason logically from this information, and come to reliable and trustworthy conclusions about the world that enable one to live and act successfully in it. ... critical thinking mimics the well-known method of scientific investigation: a question is identified, an hypothesis formulated, relevant data sought and gathered, the hypothesis is logically tested and evaluated ... [1]

Students who can think critically can:

- Determine what information is required to achieve an objective, find that information, and apply it
- Create designs from limited information
- design test benches that can prove that a design meet a specification
- identify design errors, and adjust a design to meet specifications

A course goal is students learn to enjoy the CMOS ASIC design team experience through a *hands on* approach.

Student Preparedness

Students should have previously had a class on CMOS design, and be familiar with the Cadence design, simulation, and layout tools. Circuit level debug skills are required. Logic design skills will be required for the homework and project, and will not be taught in the class. Students should be comfortable with undergraduate analog design concepts.

Students are expected to have previously taken a course where static CMOS design and analysis has been taught (EE224). EE227 picks up where static CMOS design leaves off, and explores the mixed signal and system level design concepts. Students should already know how to size transistors for a given CMOS logic function, and the basics of CMOS gate layout.

Outcome Assessment (Grading):

- Homework (10%): Homework will consist of a mix of analysis and design problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. In addition to homework, online assessments are included in the homework scores. Students are encouraged to work in groups on a number of group homeworks, but each student needs to try to solve the homework problems before group meetings. Each student in a group must submit individual homework assignments on the eCampus system until formal groups are set up on the system. After that, the group assignments will be presented to groups, and must be submitted as a group. When the group submission is made, only one submission is required for the entire group. Online assessments must be completed individually.
 - All homework shall be submitted individually or through eCampus groups using the eCampus system. (you can access the system at <http://sjsu6.blackboard.com>)
 - The eCampus document upload only works from a windows based machine. If you use another operating system, you can upload from the success center located in the Clark building
 - You can scan paper documents at the success center
 - Your user ID is your SJSU student number
 - Your password will be given in class
 - Please login and change your password
 - Developing professional discipline through on time homework submission is expected and required. Homework scores are modified according to the following schedule:
 - 100% Early or on time
 - 50% Late up to 1 week
 - 0% Late one week or more (Not accepted for grading)

- Group Project (15%): This project is a design problem. The specifications are found on eCampus. The project selection must be approved by the instructor to ensure students are working on different building blocks. Teams of 2-3 people are expected to work on the design project. You are expected to design, simulate, debug, layout, and prepare your project to be a cell in a larger chip. Analog test benches will be used to verify correct operation. To encourage original design, the process is changed every semester. Some projects seem to appear each semester, or students don't finish the project. To encourage better work, the following rules will be strictly enforced:
 - **Any project of a current mode DAC with X/Y decoding will receive a score of 0%**
 - **Any project of a Current mode DAC with a current reference in the cell will receive a score of 0%**
 - **Any project with a voltage dependent current reference will receive a score of 0%**
 - **Any project with an ideal voltage or current source anywhere except the test bench will receive a score of 0%**
 - **Any project that appears to be substantially the same as another will receive a score of 50%** The text Book is "CMOS Circuit Design, Layout, and Simulation" (revised second edition) by R. Jacob Baker
- Midterm (30%): Covers the first half of the semester. A study guide is available on the web site with typical questions. Several past midterms are also posted on the web. All EE227 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in the exam. The text Book is "CMOS Circuit Design, Layout, and Simulation" (revised second edition) by R. Jacob Baker
- Final Exam (45%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. All EE227 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in the exam.

Grading Scale

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.999%	varies for + and -
C+	78-79.99999%	No C or C- grades are given.
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at <http://info.sjsu.edu/web-dbgen/narr/socfall/rec-298.html>. Information about late drop is available at <http://www.sjsu.edu/sac/advising/latedrops/policy/>. Students should be aware of the current deadlines and penalties for adding and dropping classes.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Honor Code

Students should know that the University's Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work.

Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Adherence to the San Jose State Honor Code is required in EE287.

San Jose State University
Electrical Engineering Department
EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

A student's second offense in any course will result in a Department recommendation of suspension from the University.

Homework Due Dates

Date	Homework	Due
01-Sept	D 1.1,1.2	
03-Sept	P5.3	
08-Sept	K'n K'p homework due	D1
10-Sept	Lab Project Proposal	P5
15-Sept	P 23.9 23.11	
17-Sept	Capacitor Layout The text Book is "CMOS Circuit Design, Layout, and Simulation" (revised second edition) by R. Jacob Baker	Proposal
22-Sept	Current Ref Design	P23
24-Sept	Current Ref Layout	kn kp
01-Oct	Amplifier HW, D3.1 3.2	Cap layout
06-Oct	Amplifier Layout	
08-Oct	D 2.1 2.2 4.1 4.2	Cur Ref
13-Oct	P20.12 (except use figure 20.47 top) D 7.1 7.2	Cur Lay
20-Oct	Lab Project 1st schematic	Amp, D3
22-Oct	Balanced Switch	Amp Lay
27-Oct		D2

29-Oct	D 5.1 5.2	P20 D7
03-Nov	Current mode blocks	Bal sw
05-Nov	P18.1 18.3 18.7	1st schem
10-Nov		D5
12-Nov		P18
17-Nov		Cur blks
03-Dec		Project

Course plan

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews. The items labeled ACC are eCampus assessments (online quizzes) each students should perform online.

Date	Topic	Baker	De
25-Aug	Introduction, overview		
27-Aug	CMOS gate review/Low Power	Notes	CH 1
01-Sept	BSIM Spice Model	Chapter 6	
03-Sept	CMOS Passive Elements	Chapter 5	
08-Sept	Analog MOSFET models	Chapter 9	
10-Sept	Analog MOSFET models	Chapter 20	
15-Sept	References	Chapter 23	
17-Sept	References/Amplifiers	Chapter 21	
22-Sept	Amplifiers	Chapter 24	CH 2
24-Sept	Amplifiers	Chapter 25	CH 3
01-Oct	Amplifiers and SC functions	Chapter 26	CH 4
06-Oct	Current Sources and Sinks	Chapter 20	CH 7
08-Oct	Current Sources and Sinks	Chapter 20	

13-Oct	Midterm Review		
15-Oct	Midterm		
20-Oct	Data Converter Fundamentals	Chapter 28	CH 5
22-Oct	Data Converter SNR and ENOB		
27-Oct	Data Converter Architectures	Chapter 29	CH 8
29-Oct	Data Converter Architectures	Chapter 29	
03-Nov	Current Source D/A converters	Notes	
05-Nov	Special Purpose Digital Circuits	Chapter 18	
10-Nov	Digital PLLs	Chapter 19	
12-Nov	Digital PLLs		
17-Nov	Digital PLLs		
19-Nov	Delay Locked Loops	Notes	
24-Nov	Non Linear Circuits	Chapter 27	CH 6
26-Nov	No class -- Thanksgiving		
01-Dec	I/O Buffers	Notes	
03-Dec	I/O Buffers	Notes	
08-Dec	Float -- Review	study guide	

Text Book

The text Book is "CMOS Circuit Design, Layout, and Simulation" (revised second edition) by R. Jacob Baker