

San José State University
Electrical Engineering Department
EE224, CMOS ASIC Design, Fall 2009

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Office Hours: T&TH 3:30-5:30pm Other days by appointment
Class Days/Time: T&TH 7:30-8:45PM
Classroom: CL 117

Prerequisites:

Web Page

[Http://www.engr.sjsu.edu/mjones](http://www.engr.sjsu.edu/mjones)
Blackboard <http://sjsu6.blackboard.com>

Course Description

EE224 teaches high speed CMOS design concepts beyond traditional static CMOS. The course will focus on high speed transistor level logic design, with various modules used as design examples. Overall concepts will be tied together by a design project. Team work will be stressed.

Course Goals and Student Learning Objectives

- Prepare students to be productive members of an industrial CMOS design team
- Prepare students for graduate projects involving digital microelectronic design
- Provide an understanding of high speed CMOS design
- Provide an opportunity developing teamwork skills
- Provide an environment where students learn to think critically
- Provide an environment where students learn to enjoy the design and learning processes
- Have students internalize the culture of the design engineer

Course Objectives (Outcomes):

To be productive members of an industrial CMOS design team, students should be able to:

- Practice and demonstrate critical thinking
- Understand requirements and translate them to a high speed implementation
- Understand capabilities and limitations of CMOS logic and adjust designs to best use CMOS architectures
- Demonstrate common CMOS circuit design techniques
- Demonstrate an ability to use industry simulation and layout tools to achieve desired project objectives
- Demonstrate an understanding of module interfaces, pipe lining, and high speed clocking requirements
- Size transistors to achieve design performance goals
- Demonstrate skills with a substantial project involving teamwork

Critical thinking has been described as:

A person who thinks critically can ask appropriate questions, gather relevant information, efficiently and creatively sort through this information, reason logically from this information, and come to reliable and trustworthy conclusions about the world that enable one to live and act successfully in it. ... critical thinking mimics the well-known method of scientific investigation: a question is identified, an hypothesis formulated, relevant data sought and gathered, the hypothesis is logically tested and evaluated ... [1]

Students who can think critically can:

- Determine what information is required to achieve an objective, find that information, and apply it
- Create designs from limited information
- design test benches that can prove that a design meet a specification
- identify design errors, and adjust a design to meet specifications

A course goal is students learn to enjoy the CMOS ASIC design team experience through a *hands on* approach.

Student Preparedness

Students are expected to have previously taken a course a course using the Cadence design tools. (EE166). These tools are required for homework and project completion, and will not be taught in this class.

Students are expected to have previously taken a course where static CMOS design and analysis has been taught. EE224 picks up where static CMOS design leaves off. Students should already know how to size transistors for a given transfer curve, and the basics of CMOS gate layout.

Outcome Assessment (Grading):

- Homework (10%): Homework will consist of a mix of analysis and design problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. In addition to homework, online assessments are included in the homework scores. Students are encouraged to work in groups after homework 7-4, but each student needs to try to solve the homework problems, before group meetings. Each student in a group must submit individual homework assignments on the eCampus system until formal groups are set up on the system. After that, the assignments will be presented to groups, and must be submitted as a group. When the group submission is made, only one submission is required for the entire group. Online assessments must be completed individually.
 - All homework shall be submitted individually on the eCampus system. (you can access the system at <http://sjsu6.blackboard.com>)
 - The eCampus document upload only works from a windows based machine. If you use another operating system, you can upload from the success center located in the Clark building
 - You can scan paper documents at the success center
 - Your user ID is your SJSU student number
 - Your password will be given in class
 - Please login and change your password
 - Developing professional discipline through on time homework submission is expected and required. Homework scores are modified according to the following schedule:
 - 100% Early or on time
 - 50% Late up to 1 week
 - 0% Late one week or more (Not accepted for grading)
- Group Project (15%): This project is a design problem. Teams will propose a high speed block to meet design requirements. The block requirements will be provided. The block type will be selected from a theme which establishes function and bit lengths for each block. Teams of 2-3 people are expected to work on the design project
- Midterm (35%): Covers the first half of the semester. A study guide is available on the web site with typical questions. Several past midterms are also posted on the web. All EE224 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple

versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.

- Final Exam (40%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. All EE224 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (5-8 typically). You should bring a calculator and writing instruments to the exam. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.

Grading Scale

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.999%	varies for + and -
C+	78-79.99999%	No C or C- grades are given.
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available.

Honor Code

Students should know that the University's Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all

assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Adherence to the San Jose State Honor Code is required in EE287.

***San Jose State University
Electrical Engineering Department
EE Department Honor Code***

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*

A student's second offense in any course will result in a Department recommendation of suspension from the University.

Homework Due Dates

Date	Homework assigned	Due Dates
25-Aug		Get account
27-Aug	1-2, 1-6	Learn layout
01-Sept	5-7, 5-9, 5-14	do 166 example, ACC1
03-Sept	3-6 no spice, 3-8, 3-11	1-* due
08-Sept	An/Ap Homework	5-* due
10-Sept	<i>Write up Project Proposal</i>	3-* due, ACC2
15-Sept	7-1, 7-4	Proj Proposal Due
17-Sept	supp dynamic logic calcs	An/Ap due
21-Sept	CVSL HW	7-* due
28-Sept	<i>Design project block diagram</i>	Dynamic logic calcs, ACC3
01-Oct	Flip Flop assignment	CVSL HW due
06-Oct	<i>Pipeline project design</i>	Pipeline due
08-Oct	CPL Homework	Flip-flop due

13-Oct	Block diagram due
15-Oct	CPL due
29-Oct	ACC4
05-Nov	Block design due
19-Nov	1st Transistor due
03-Dec	Project Due

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at <http://info.sjsu.edu/web-dbgen/narr/socfall/rec-298.html>. Information about late drop is available at <http://www.sjsu.edu/sac/advising/latedrops/policy/>. Students should be aware of the current deadlines and penalties for adding and dropping classes.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Course plan

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews. The items labeled ACC are eCampus assessments (online quizzes) each students should perform online.

Date	Topic	Text	Other
25-Aug	Introduction/Review MOS Equations	1	intro2
27-Aug	MOS Transistor equations	2	most1
01-Sept	Switch Level circuit Design	4,5	Switch2
03-Sept	CMOS equations	3	cmos1, cmosdelay2
08-Sept	Latches		latch2
10-Sept	Other CMOS styles	9	Cmosstyle2
15-Sept	Dynamic CMOS	7	dynamic

17-Sept	Dynamic Logic device size calculations		dynsize
21-Sept	Dynamic And/Or Examples		In class on board
28-Sept	Xors and inversions with dynamic logic		In class on board
01-Oct	Adders		adder
06-Oct	CLA, Dynamic Examples	8	In class on board
08-Oct	Scaling in MOS processes		Scaling
13-Oct	Multipliers		Multipliers
15-Oct	Multiplier example		study guide
20-Oct	Midterm		
22-Oct	Sizing examples, and issues		
27-Oct	Floor Planning		Floor
29-Oct	Clock Generation		Clockgen
03-Nov	Clock Distribution examples		In class on board
05-Nov	PLAs		PLA
10-Nov	ROM/RAM common elements		
12-Nov	MOS RAMS		mosrams
17-Nov	MOS RAMS/ROMS		mosrams2
19-Nov	shifters and rotators		shiftrt
24-Nov	Characterizing for ASIC libraries		ASICchar
26-Nov	No Class – Thanksgiving		
01-Dec	I/O buffers		
03-Dec	I/O buffers		
08-Dec	Final Review		

Text Book

The text Book is "CMOS logic Circuit Design" by John P Uyemura