

**San José State University**  
**Department of Electrical Engineering**  
**EE223, Analog Integrated Circuits**  
**Number 40587, Section 01, Fall 2009**

<b>Instructor:</b>	Prof. Hamedi-Hagh
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<b>Office Hours:</b>	Wednesdays, 13:30 to 16:30 and Tuesdays, 17:45 to 18:45 or by appointment
<b>Class Schedule:</b>	Mondays/Wednesdays 16:30-17:45
<b>Classroom:</b>	ENGR401
<b>Prerequisites:</b>	EE221

**Course Description:**

This course studies nanoscale metal-oxide semiconductor field effect transistor (MOS-FET) modeling and circuit design techniques for analog integrated circuit applications. Course topics include short channel issues, layout techniques to improve design performance, noise modeling and transformation, wide-swing current mirrors, gain, bandwidth and voltage swing characteristics of single-stage and two-stage amplifiers. A variety of opamp architectures with their slew rate, settling time, phase margin, stability, gain, bandwidth, noise and distortion characteristics will be discussed in details. The course also discusses comparator design issues, sample and hold design issues and modern switched capacitor circuits to achieve high precision functionality.

**Required Textbook:**

- Analysis and Design of Analog Integrated Circuits, 4th Edition, by Paul R. Gray, P. J. Hurst, S. H. Lewis and Robert G. Meyer, Wiley, 2001

**Other Reference Materials:**

- Analog Integrated Circuit Design, by David A. Johns and Ken Martin, Wiley, 1997
- Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill, 2001

**Grading:**

assignments	30%
design project	30%
midterm exam	20%
final exam	20%

### **Grading Percentage Breakdown:**

90% and above	A
89% - 85%	A-
84% - 82%	B+
81% - 79%	B
78% - 75%	B-
74% - 72%	C+
71% - 69%	C
68% - 65%	C-
64% - 62%	D+
61% - 59%	D
58% - 55%	D-
below 55%	F

### **Exams:**

The date of the exams is shown on the course syllabus. Exams will be closed book. However, students are allowed to bring 1 page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

### **Projects:**

Assignments and projects closely relate to topics discussed in this course and change every semester. Each group (maximum 2 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up including all images and graphs as a single file by email within a week after the last lecture to be eligible to receive a credit. Students may be required to present their works similar to standard design reviews as conducted in industry. Non restricted MOSFET transistor models will be provided for assignments and projects. More details on design projects will be provided as the classes progress. **Please look under the EE223 course menu in <http://www.ics.sjsu.edu> to download the related materials.**

### **Academic Integrity Statement:**

Your own commitment to learning, as evidenced by your enrollment at San Jose State University, and the University's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty members are required to report all infraction to the Office of Student Conduct and Ethical Development. The policy on academic integrity can be found at [http://sa.sjsu.edu/student\\_conduct](http://sa.sjsu.edu/student_conduct)

Students in this course are expected to maintain high ethical standards in all matters pertaining to the course, including, but not limited to, examinations, homework, course assignments, presentations, writing, laboratory work, team work, treatment of class members, and behavior in class. Cheating and plagiarism are violations of the SJSU Policy on Academic Dishonesty (S98-1) and will not be tolerated in the class. Students are expected to have read the Policy, which is available at <http://www2.sjsu.edu/senate/S014-12.pdf>

## **Campus Policy in Compliance with the Americans with Disabilities Act:**

If you need course adaptations or accommodations because of a disability, if you have emergency medical information to share or if you need to make special arrangements in case the building must be evacuated, please make an appointment with your course instructor or see him/her during office hours as soon as possible.

### **Course Goals:**

1. Students will be able to design advanced biasing circuits, opamps, comparators and switch-capacitor circuits.
2. Students will be able to understand the concept of noise, distortion, stability, phase margin, voltage swing, slew-rate and gain-bandwidth product.
3. Students will be able to use modern engineering CAD tools for computations, simulations, analysis, and design.
4. Students will be able to verify the theory with hands-on lab simulations.

### **Course Learning Objectives:**

- The ability to design and analyze high speed opamp circuits
- The ability to understand and design the wide swing biasing circuits
- The ability to analyze common emitter amplifiers
- The ability to understand filtering theory and design of common drain amplifiers
- The ability to analyze frequency instability caused by circuit parasitics or architecture
- The ability to learn methods and simulation tools to characterize complex Analog integrated circuits
- The ability to design integrated comparators
- The ability to calculate the charge injection in switched capacitor amplifiers
- The ability to understand the Analog signal components and their impact on power and bandwidth
- The ability to determine the trade-off among linearity, efficiency and gain of amplifiers
- The ability to design multi-stage amplifiers
- The ability to understand various frequency compensation techniques for amplifiers
- The ability to perform team work and analyze the operation of low voltage and low power nanoscale integrated circuits

## Tentative Course Syllabus and Schedule

	Topics
Mon, Aug 24	Introduction
Wed, Aug 26	MOS Transistor Modeling
Mon, Aug 31	Short Channel Effects
Wed, Sep 2	Layout Techniques
Wed, Sep 9	Noise in Small-Signal Amplifiers
Mon, Sep 14	Noise Transformation
Wed, Sep 16	Current Mirrors
Mon, Sep 21	Wide Swing Current Mirrors
Wed, Sep 23	CS Single-Stage Amplifiers
Mon, Sep 28	CD Single-Stage Amplifiers
Wed, Sep 30	CG Single-Stage Amplifiers
Mon, Oct 5	Cascade Amplifiers
Wed, Oct 7	Cascode Amplifiers
Mon, Oct 12	Diff-pair Amplifiers
Wed, Oct 14	<b>MIDTERM EXAM (75 minutes)</b>
Wed, Oct 21	Two-Stage Opamps
Mon, Oct 26	Frequency Compensation
Wed, Oct 28	Folded Cascode Opamps
Mon, Nov 2	Current Mirror Opamps
Wed, Nov 4	Nested Miller Opamps
Mon, Nov 9	Low Voltage Opamps
Mon, Nov 16	Fully Differential Opamps
Wed, Nov 18	Common Mode Feedbacks
Mon, Nov 23	Comparator Offsets
Wed, Nov 25	Offset Cancellation
Mon, Nov 30	Latched Comparators
Wed, Dec 2	Sample and Hold Circuits
Mon, Nov 7	Charge Injection <i>(projects are due by the last Friday of the lectures)</i>
Tue, Dec 15	<b>FINAL EXAM (14:45 — 17:00)</b>

1. University and College Furlough programs might affect the class schedule. These changes, if any, will be announced in the classroom.
2. Monday, September 7<sup>th</sup> is Labor holiday.
3. Monday, October 19<sup>th</sup> is a Furlough day designated by the SJSU president.
4. Wednesday, November 11<sup>th</sup> is Veterans holiday.