

San José State University
College of Engineering/Electrical Engineering
EE221, Principle of Semiconductor Devices I,
Section-01 and 02, Fall, 2009

Instructor:	Lili He
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Office Hours:	TR 9:00am-10:20am, and 4:20-5:00pm
Class Days/Time:	TR 1:30 -2:45pm (section-01) TR 3:00-4:15pm (section-02)
Classroom:	ENG 345 (section-01) ENG232 (section-02)
Prerequisites:	EE128 or Consent of instructor

Course Description

This course is a prerequisite for all electronics area courses and reviews semiconductor device physics and technology. The students are expected to have some background in atomic physics and solid state physics for this course. The course is divided into four parts- semiconductor fundamentals, p-n junctions, bipolar junction transistors (BJT), and field effect transistors (FET).

Course Goals and Student Learning Objectives

Upon successful completion of this course, students will be able to:

LO1 **Describe** fundamental concepts of solid-state physics applied to the semiconductor devices by Silicon and compound semiconductor materials.

LO2 **Explain** general electrical behavior of semiconductor Si and GaAs, construct appropriate physical models.

LO3 **Illustrate** structural details and current-voltage characteristics of p-n junction diode, BJT, MOSFET, Metal/semiconductor diode, and MESFET.

LO4 **Apply** the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.

Required Texts/Readings

Textbook

Semiconductor Devices: Physics and Technology 2nd ed., by S.M.Sze, John Wiley, 2002, ISBN0471333727

Other Readings

1. Solid State Electronic Devices, 6th ed., Ben G. Streetman, S.K. Banerjee, Prentice Hall, 2000
2. Physics and Technology of Semiconductor Devices, A.S. Grove, John Wiley, 1967.
3. Semiconductor Devices, S.M. Sze, John Wiley, 1985.
4. Device Electronics for Integrated Circuits, RS. Muller and T.I. Kamins, John Wiley, 1977.
5. VLSI Fabrication Principles, Sorab K. Ghandi, John Wiley, 1983.
6. VLSI Technology, S.M. Sze, McGraw- Hill, 1985.
7. Microelectronic Processing- An Introduction to Manufacturing Integrated Circuits, W. Scott Ruska, McGraw- Hill, 1987.
8. Electronic Materials Science for Integrated Circuits in Si and GaAs, Shyam P. Murarka and Martin C. Peckerer, Academic Press, 1989.
9. Electronic materials Science and Technology, James W. Mayer and S.S. Lau, Macmillan, 1990.)

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Assignments and Grading Policy

a. Homework

Homework will be assigned during the semester (usually one per chapter). Homework will NOT be collected. The solution will be discussed in the class and/or posted in the web.

b. Exams.

There will be two mid-term examinations and one final examination.

c. Class Participation:

Class participation is required, and student attendance will be checked.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. [Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html](http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html). [Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/](http://www.sjsu.edu/sac/advising/latedrops/policy/). Students should be aware of the current deadlines and penalties for adding and dropping classes.

Grading Policy

Midterm (two)	25% each
Quiz and Class Participation	10 %
Final Exam	40 %
Total	100%

Final Grade Percentage Breakdown

90% and above	A
89% - 85%	A-
84% - 80%	B+
79% - 70%	B
69% - 65%	B-
64% - 60%	C+
59% - 55%	C
54% - 50%	C-
49% - 45%	D+
44% - 40%	D
below 40%	F

University Policies

Academic integrity

Students should know that the University's [Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf).

Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for [Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE221 / Principle of Semiconductor Devices, Section-02

Fall 2009, Course Schedule

Table 1 Tentative Course Schedule

The schedule is subject to change with fair notice to be announced in class.

Week	Topic	Reading
Week 1	Introduction to semiconductor device and technology	Chapter1
Week 2	Semiconductor materials	Chapter 2: 2.1-2.2, 2.4-2.7
Week 3	Carrier transport	Chapter 3: 3.1-3.7
Week 4	p-n Junctions fabrication; equilibrium conditions	Chapter4: 4.1-4.2
Week 5	p-n junction operation	Chapter 4: 4.3-4.6
Week 6	Reverse break down, transient behavior, Junction breakdown, hetero junctions	Chapter 4: 4.7-4.8
Week 7	First Mid-Exam	
Week 8	Bipolar Transistor Fundamentals: The transistor action, and static characteristics of BJT	Chapter 5: 5.1-5.2
Week 9	Frequency response and switching of BJT, Heterojunction BJT	Chapter 5: 5.3-5.4
Week 10	The MOS Diode	Chapter 6: 6.1
Week 11	MOSFET fundamentals	Chapter 6: 6.2
Week 12	MOS scaling , CMOS, BiCMOS, MOSFET on insulator	Chapter 6: 6.3-6.7
Week 13	Second Exams	
Week 14	Metal-Semiconductor contacts	Chapter 7:7.1
Week 15	MESFET and review for final	Chapter 7: 7.2-7.3
Final Examination:		

Fall 2009

**San Jose State University
Electrical Engineering Department**

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor.”*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student’s second offense in any course will result in a Department recommendation of suspension from the University.*