

Dr. Parent received his B.S.(1992) M.S.(1996) and PhD(1999) at the University of Connecticut and is an assistant professor in the San Jose State Electrical Engineering Department since the fall of 1999. This past year he has taught the undergraduate semiconductor device physics course, as well as the IC fabrication lab. He is currently teaching courses in digital/mixed signal IC design and fabrication. Dr. Parent has been active in the new Microelectronics Process Engineering Program providing expertise in process integration. In addition, he has received funding to develop the infrastructure required to bring an authentic IC Design experience to all EE Students.

Dr. Parent sees that his role as a teacher is to provide a challenging and interesting learning environment. He is also a firm believer in 'hands on learning' (Situating Cognition) and is introducing state of the art, UNIX based, IC design and silicon processing software to undergraduates.

Prior to joining us at San Jose State, he was a graduate student in the EE



department of the University of Connecticut, where he taught a silicon device fabrication laboratory as well as a digital IC design lab that used Cadence tools extensively.

At the University of Connecticut, Dr. Parent conducted studies (growth and device simulation) of

zinc selenide (a semiconductor) based lasers and photo detectors that operate in the blue-green light spectrum. He has also designed and simulated infrared light modulators to be used for wavelength division multiplexing.

Dr. Parent received his B.S.(1992) M.S.(1996) and PhD(1999) at the University of Connecticut.

Name: David W. Parent

Academic rank: Full time assistant professor

Years of Service: 3 years service at SJSU, Date of appointment: 16 August 1999

Grants:

AY 2001-2004, PI Cadence Design Systems Curriculum Development, with Belle Wei and Jim Freeman, \$499k in faculty release time, computer equipment, software, students assistants to develop integrated circuit courses in which students design, fabricate and test integrated circuits.

Summer 2001, PI California Workforce Initiative (CWI) \$28k grant, Title: Design of High Speed CMOS Circuits Using the TSMC .18 μ m MOSIS Fabrication Process

AY 1999-2003, Co PI NSF \$478k grant with Emily Allen(PI), S. Gleixner, Y. Dessouky and G. Young, Title: Development of a Microelectronics Process Engineering Curriculum.

AY 2000, Co PI SME \$70k grant with Emily Allen(PI), S. Gleixner, Y. Dessouky and G. Young, Title: San Jose state University Microelectronics Process Engineering Laboratory.

Fall 2000, PI \$2.5k CSU mini-grant, The Growth, Fabrication and Simulation of GaAs Based MOSFET Structures.

Summer 2001, PI \$7k CSU summer fellowship, The atmospheric MOVPE growth of SiGe on Si Substrates.

Experience:

EE Department San Jose State University, Fall 1999 to Present

Teaching Duties:

- Fall 2002 EE166 Design of CMOS Digital ICs, EE129-IC fabrication lab
- Spring 2002 EE167-Micro Electronic Manufacturing Methods, EE166 Design of CMOS Digital ICs.
- Fall 2001 EE166 Design of CMOS Digital ICs, EE129-IC fabrication lab
- Spring 2001 EE167-Micro Electronic Manufacturing Methods, EE128-Physics of Transistors.
- Fall 2000: EE224-CMOS Digital Circuit Design, EE128-Physics of Transistors.
- Spring 2000 EE128- Physics of Transistors, EE129-IC fabrication lab
- Fall 1999: EE128-Physics of Transistors

Transwitch Corporation, Summer 1994:

- VHDL Test Bench Engineer, Developed input vectors for a Constant Bit Rate ATM Chip. Tested a Better than eight zeros and HDB3 encoders and decoders. Developed on chip self test for ATM Chip as well as a clock with simulated jitter. Developed a UNIX Makefile to convert Synopsis VHDL to MENTOR GRAPHICS VHDL.

EE Department University of CT, Fall 1993 to Spring 1999:

- *Research Assistant, II-VI Blue Green Lasers/Detectors Project:* Designed and carried out experiments for the MOVPE fabrication of II-VI HBT Photo-transistors, Heterojunction solar cells, ZnMgSSe cladding layers, and ZnCdSe/ZnSSe quantum well active regions for II-VI lasers. Material was grown with an EMCORE vertical chamber MOCVD reactor. Modified EMCORE reactor to add nitrogen, HCl, and Mg sources. Converted Room Temperature PL setup to 10K. Modeled ZnSe/GaAs, AlGaAs/GaAs and SiGe HBT's using Silvaco's ATLAS device simulator.
- *Research Assistant, II-VI Nano-Particle Displays:* Designed three alkyl channels for Nano-Particle reactor, designed flow rates for alkyl sources, developed and implemented helium leak test plan for reactor, and assisted with assembly of reactor.
- *Instructor, Silicon Device Processing Laboratory:* Supervised and developed a senior and graduate laboratory course introducing standard silicon processing techniques for design, fabrication, and characterization of devices such as BJTs, MOS Inverters, SCRs, LEDs. Improved laboratory manual, standardized experiments and wrote detailed instruction in html. Improved MOS Qss to $1.2 \times 10^{10} \text{ cm}^{-2}$. Introduced the use of Silvaco's virtual wafer fab to students. Improved metalization process. Played an advisory role to faculty laboratory committee.
- *Research Assistant, OLIN MQUAD Project:* Assisted in the simulation of OLIN's MQUAD package for 100MHz dies, using ANSOFT's MAXWELL. Set up and maintained Apollo 9000 used for the project.
- *Instructor, Young Scholars:* Designed and implemented electronics instruction and silicon solar cell fabrication for high school senior out reach program. Supervised two junior lab mentors.
- *Research Assistant, Automated Solar Cell Test Station:* Supervised two undergraduates who constructed a computer controlled IV tester for Si and ZnSe/GaAs solar cells.

Military (CT Army National Guard) 1985-1996:

- Platoon Leader: Responsible for the training and welfare of a 30 soldier Combat Engineer Platoon including 10 Non-Commissioned officers. Accountable for 400,000 dollars worth of Engineer equipment.
- Company Commander: Responsible for the training, welfare and overall readiness of a 150 soldier (including 4 officers and 20 NCO's) Combat Heavy Engineer Company. Accountable for over three million dollars worth of engineer equipment.

Honors:

Eagle Scout.

Dean's List Spring 1992.

Winner 1996 Brundage Family Scholarship for Leadership and Academics.

CAD Tutorials:

- Getting Started with UNIX and CDE
- Bottom Up Design Tutorial Using Cadence Tools
- FAQ 1 on Cadence Tools
- Module 2: Using NC-verilog to verify logic in complex AOI circuits.
- Silvaco Tutorial

IC Fabrication Lab Documentation:

- Oxidation/Diffusion Furnace Documentation
- Photolithography Documentation

Journal Articles:

- 1) D. W. Parent, A. Rodriguez, J. E. Ayers and F. C. Jain, "The Photoassisted MOVPE Growth of ZnSe(n)/GaAs(p+) Solar Cells", To be published in the Journal of Solid State Communications 2003.
- 2) Emily Allen, Stacy Gleixner, David Parent, Greg Young, Yasser Dessouky and Linda Vanasupa, "Microelectronics Process Engineering at San Jose State University: A Manufacturing-Oriented Interdisciplinary Degree Program" accepted for publication in the International Journal of Engineering Education (March 2002).
- 3) D. W. Parent, A. Rodriguez, J. E. Ayers and F. C. Jain, "The Photoassisted MOVPE Growth of ZnMgSSe", *Journal of Crystal Growth*, Vol. 224, pp. 212-217 (2001).
- 4) D. W. Parent, A. Rodriguez, X. G. Zhang, G. Zhao, P. Li, J. E. Ayers and F. C. Jain, "The Photoassisted MOVPE Growth of ZnSSe using

- Tertiaributylmercaptan”, *Journal of Electronic Materials*, Vol. 29, No. 6, pp. 713-717 (2000).
- 5) X.G. Zhang, P. Li, G. Zhao, D.W. Parent, F. C. Jain, and J. E. Ayers, “Removal of Threading Dislocations from Patterned Heteroepitaxial Semiconductors”, *Journal of Electronic Materials*, Vol. 27 pp. 1248-1253 (1998).
 - 6) F. Jain, E. Heller, D. Parent, H. Wang, W. Zappone, S. Srinivasan, S. Cheung, W. Huang, R. Bansal, J. Preiss, L. Green, A. Arinilli, and M. Russel, “Multiple Quantum Well In-Line Optical Modulators Using Tunable Distributed Bragg Grating Photonically Controlled Active Array”, *IEEE Antennas and Propagation Society International Symposium*, Vol. 2, pp. 755-758 (1997).
 - 7) X.G. Zhang, S. Kalisetty, J. Robinson, G. Zhao, D.W. Parent, J. E. Ayers, and F. C. Jain, “Structural properties of $ZnS_ySe_{1-y}/ZnSe/GaAs(001)$ grown by photoassisted metalorganic vapor phase epitaxy”, *Journal of Crystal Growth*, Vol. 174 pp 726-732 (1997).
 - 8) D. W. Parent, S. Kalisetty, X. G. Zhang, G. Zhao, W. Zappone, J. Robinson, Evan Heller, J. E. Ayers and F. C. Jain, “A Comparison of Ethyl Iodide and Hydrogen Chloride for doping ZnSe Grown by Photoassisted MOVPE”, *Journal of Electronic Materials*, Vol. 26 pp. 710-714 (1997).

CONFERENCE PROCEEDINGS:

- 1) S.H. Gleixner, G.L. Young, L.S. Vanasupa, Y. Dessouky, D.W. Parent and E.L. Allen, “Teaching Design of Experiments and Statistical Analysis of Data Through Laboratory Experiments,” accepted for publication in Procs. 2002 Frontiers in Education Conference (November 2002).
- 2) Emily Allen, Huong Vu and David Parent, “The Spartan Solar Cell Freshman Experience,” Abstract submitted for presentation at the National Educators Workshop, San Jose, CA (October 2002).
- 3) Gregory Young, David Parent, Yasser Dessouky, Stacy Gleixner, Emily Allen, and Linda Vanasupa, “Course Assessment of the Microelectronics Process Engineering Program at SJSU,” Procs. 2002 American Society for Engineering Education (2002).
- 4) David Parent, Yasser Dessouky, Stacy Gleixner, Gregory Young and Emily Allen, “The Microelectronics Process Engineering Program at SJSU,” Proceedings of the 14th Biennial IEEE University/Government/Industry Microelectronics Symposium,” Richmond, VA, pp. 128-134, (June 2001).
- 5) Emily Allen, Stacy Gleixner, David Parent, Greg Young, Yasser Dessouky and Linda Vanasupa, “Microelectronics Process Engineering: a non-traditional approach to MS&E,” Materials Research Society Procs. 684E, GG5.1 (April 2001).

CONFERENCES:

The UGIM Conference, Presented Paper, "Microelectronics Process Engineering Program at SJSU", Virginia Commonwealth University, Richmond VA, June 2001

The Connecticut Microelectronics and Optoelectronics Conference (CMOC), Presented Poster, "The Photoassisted MOVPE Growth of ZnMgS", Yale University, March 2000.

SME Grant Meeting, Presented Talk, "Microelectronics Process Engineering Program at SJSU", Dearborn MI, June 2000.

U.S. Workshop on the Physics and Chemistry of II-VI materials, Las Vegas NE, Paper presented, "The Photoassisted MOVPE Growth of ZnSSe using Tertiabutylmercaptan", Las Vegas NE, 1999.

The Connecticut Microelectronics and Optoelectronics Conference (CMOC), Presented Poster, "The Photoassisted MOVPE Growth of ZnSSe using Tertiabutylmercaptan", Yale University, March 1999.

The Connecticut Microelectronics and Optoelectronics Conference (CMOC), Presented Poster, "A Comparison of Various Methods for Microstrip Line Analysis", Yale University, March 1998.

The Connecticut Microelectronics and Optoelectronics Conference (CMOC), Presented the paper, "ZnSe on GaAs HBT for use as a Photo Transistor", Yale University, March 1997.

Invited Talk, Gave the presentation, "ASIC Design Cycles Using VHDL" Trinity College, Hartford CT, 10 October 1996.

The U.S. II-VI Workshop, Presented the paper "A Comparison of Ethyl Iodine and Hydrogen Chloride in ZnSe grown by Photoassisted MOVPE" Las Vegas, Nevada (OCT 22-24 1996.)

The 1995 IECP, Presented a paper "Three Dimensional Modeling of MQUAD Packages at 100 MHz", San Diego October 1995.

Scientific and professional society memberships:

- IEEE Member (Solid State Circuits Society, EDS)
- IEEE SJSU Branch Counselor

INSTITUTIONAL AND PROFESSIONAL SERVICE

- UCONN Engineering Enrollment Committee (1995-1997)
- Academic Affairs Committee (2000-Present)
- EE Graduate Program Task Force (Spring 2000)
- EE Honors Program Task Force (Spring 1999)
- micro-ProE Committee (1999-Present)
- The Solid-State Committee (1999-Present)
- IEEE Faculty Advisor. (2000-Present)
- E10/ MatE153 Solar Cell Project advisor (2000-Present)
- EE Graduate student Survey (Spring 2002)
- College Scholarship Judge (Synopsys Science Fair) (Spring 2002)
- I am the course coordinator for, EE129, EE167, and EE166 (2000-Present)
- Developed and ran a short Course for TA's and students using the IC Fabrication lab (SP02 and FALL02).
- Developed and ran an IC design short course attended by senior and junior faculty as well as undergraduate and graduate students (FALL02).
- Director VLSI CAD LAB: In charge of developing curriculum for TCAD, digital circuit, and analog circuit simulation using state of the art CAD packages. Current CAD packages are Cadence design tools, Synopsys, and Silvaco. In charge of one system administrator. (F00 to Present)
- Reviewed one CMOS circuit textbook for McGraw Hill (Kang & Leblebici, CMOS Digital Integrated Circuits) Fall 2000
- Evaluated grant proposals for San Diego State University (Fall 2000).
- Process Integration Engineer: Designed a 4-layer NMOS process and a seven layer CMOS process as part of an NSF grant. Supervised five students verifying the two new processes.

PROFESSIONAL DEVELOPMENT ACTIVITIES

- Attended the 1998 CADENCE user's group meeting in TX
- Enrolled in the Peer Teaching Program (IRC SJSU FALL 1999)
- Attended Cadence's meeting on developing Digital and Analog SOC curriculum.

Current Projects:

Cadence Curriculum Development Grant:

- Develop self-paced instruction that teaches the design of CMOS circuits along with an industrial strength CAD tool.
- Develop the infrastructure needed to offer an authentic IC design, fabrication and test experience to undergraduate and graduate EE students.
- Develop a well-documented “front to back” IC design that students can use as a vicarious learning experience. The project includes having IC designs fabricated by the MOSIS service.

Senior Projects in the area of IC design, Fabrication and Test:

- 4 BIT ALU for SOC IP Library
- 4 BIT ALU suitable for operation in space
- 8 BIT DSP Filter

Graduate Projects in the area of IC design, Fabrication and Test:

- Low Power CMOS Multipliers
- Low Voltage CMOS OPAMPS
- Low Power CMOS Adders
- SRAM for IP library
- Design and Fabrication of LDMOS Structures
- Frequency Synthesizer Based on PLL Structure

Graduate Projects in the area of IC Processing:

- Isopropyl Alcohol as a PR Stripper (Project leader is Grey Young of CME)
- Electrical Characterization of Cu/ Nanoglass- E Damascene Structures (Project with Honeywell)

Table 1: Past Projects

Project	Student	Student	Student	Student
Inexpensive CMOS inverter process design and fabrication (BSEE-SP00)	J. Ramos	S. Lising	M.Quiazon	E. Caluya
Design and verification of a 4 MASK NMOS process (MSE-SP01)	D. Folkes			
Development of a .5micron Cadence ASIC design environment (MSEE-SP01)	B. Swamy			
Modeling of silicon germanium HBTs (MSEE-SP01)	P. Singe			
Design, Fabrication and Testing of Single Crystal Silicon Solar Cells (BSEE-SP01)	T. Pham	M. Thu	C. Nguyen	
Solar Cell Process Optimization (BSEE-F01)	Appleton, Mack	Park, Sungmin	Milano, Angel	Tsegaye, Yemane
MEMS Resonator (BSEE-F01)	Seone, Maria	Pingue, Michael	West, Ericson	McConnell, Tim
The Beowulf Cluster (BSEE-F01)	Bui, Tom	Nguyen, Khoa		
GaAs MOSFET (MSEE-F01)	Kondapalli, Goutham			
Design of a High Speed PLL Frequency Synthesizer(MSEE-F01)	Jiang, Sherman	Yoe, LayQuan		
An 8 Bit Full Adder IC(BSEE-S02)	Tieu, Dong	Ho, Liem	Do, Hau	
A 4 Bit ALU for an SOC Library(BSEE-S02)	Gonzalez, Juan	Lal, Prakriti		
2 Ghz Frequency Synthesizer(MSEE-S02)	Gauri Kulkarni			