PROCESS HANDBOOK

Gate Oxidation

I. Overview

Previously, we have selectively doped portions of our p-type silicon with phosphorus (an n-type dopant), forming the source and drain areas of our transistors. The purpose of this section will to form a region of thin, dense, pure silicon dioxide, lying across the gap between the source and the drain. This thin SiO_2 will be the gate oxide of the transistors.

This is the next step, following the Source/Drain doping procedure, in a series of lab processing sessions, which will be performed in order to fabricate and test MOS transistors and other integrated circuit elements.

The purpose of the first part of this lab will be to define the gate oxide regions using photolithography and etch. The second portion will involve re-cleaning the wafers and growing the gate oxide in a dry environment. In the process of performing this lab, students will have the opportunity to study mask alignment procedures and dry oxidation.

II. Background

II.A. The MOS system

The gate oxide will be part of the important metal-oxide-semiconductor stack, which is central to the operation of MOS transistors. The oxide between the metal and the semiconductor insulates them, and allows a voltage applied at the metal to create an electric field in the semiconductor with no current flow. If the metal is positively charged, the electric field lines will point from the metal into the semiconductor, resulting in the attraction of negative charges in the semiconductor. If the metal is negatively charged, the electric field will be oppositely directed, and positive charges will be attracted in the semiconductor. It is important for the oxide to be a good insulator to prevent current flow between the semiconductor and the metal.

If the semiconductor substrate is p-type, with majority carrier being holes, and a negative voltage is applied to the metal of an MOS stack, the result will be an *accumulation* of majority carriers in the semiconductor material just below the metal and oxide layers. If a positive voltage is applied to the metal over a p-type semiconductor, the majority carriers are *depleted,* as they are repelled away from the area just below the metal and oxide layers. Minority carriers (holes) are attracted, which result in an *inversion* of the material type, making it n-type. When the semiconductor is inverted, an electrical path (channel) is established between the n-type doped source and drain regions immediately adjacent to the MOS stack.

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II.B. Threshold voltage

Some of the factors that determine how much voltage must be applied to the metal, which will result in an inversion of the semiconductor include: oxide thickness (which determines the strength of the electric field for a given voltage), substrate doping (which determines how many minority carriers must be attracted to invert the material), Metal-Semiconductor work function difference (which determines how much the semiconductor is perturbed simply by the presence of the metal), and charge present in the oxide (which will result in a mirrored charge in the semiconductor). The oxide charge will be the most significant factor in our process. Obtaining a positive threshold voltage will be severely effected by contaminates in the oxide and is why great care will be taken in the gate oxide process steps to keep things clean. nMOS is much more susceptible to contaminants than is pMOS. Sodium, which comes from people and tap water is a major problem.

A good explanation of the simplified theory can be found in Solid State Electronic Devices, by B.G. Streetman, which is available in the Reserve Book Room of Wahlquist Library. A few points to keep in mind are that heavier doping will make the turn-on voltage of nMOS more positive, a thicker oxide will make the turn on voltage more positive, and negative charge trapped in the oxide will also make the turn on voltage more positive. The combination of all of the factors determining the threshold voltage will ideally give your transistors a turn-on voltage between 0 and 5 Volts, but can be as low as -20 or -30V, depending upon the oxide charge. If the V_T is negative then the transistor will be in the normally on state, which is not wanted.

III. Report

Only one team performs the processing steps on the lot of wafers in any given week. It is therefore critical for the other group to find out exactly what happened with the wafers. This status report must make it possible for the other group to know exactly what needs to happen to the wafers next. You are to describe the procedures you have followed in the lab, and any measurements or observations you have made during the processing. You should include the reasons for the procedures you have performed. If any unexpected results occurred, be sure to examine them, their implications, and possible solutions (if solutions are necessary).

The following questions may help you to think about some ideas to present in the status report. By no means is it an exhaustive list, it is only provided to help your group enter a discussion about what to include in the report.

1. For the Lithography step, what dose was determined, what exposure time, what development time?
2. How well aligned were the “Alignment Check” features after develop?
3. For the Etch step, how long did the oxide etch take?

4. What were the starting oxide thicknesses before etch?
5. How did the resolution lines and boxes look after etch?
6. For the oxidation step, why the pre-clean?
7. What was the oven temperature?
8. What were the Gate oxide thicknesses?
9. What was your measured values for sheet resistance on the test wafer?
10. What was your junction depth after Oxidation?

IV. References

B.G. Streetman, Solid State Electronic Devices, 2nd Ed., Prentice-Hall.

R.F. Pierret, Field Effect Devices, Modular Series on Solid State Devices, Volume 4, Addison-Wesley.